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Citation: Journal of Applied Physics **118**, 205502 (2015); doi: 10.1063/1.4936197 View online: http://dx.doi.org/10.1063/1.4936197 View Table of Contents: http://scitation.aip.org/content/aip/journal/jap/118/20?ver=pdfcov Published by the AIP Publishing

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Noise spectroscopy of polymer transistors

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(Received 8 August 2015; accepted 27 October 2015; published online 24 November 2015)

Noise studies constitute an important approach to study polymer based field effect transistors (FETs) from the perspective of disorder physics as well as device application. The current fluctuations in an all organic solution-processable FET in different regimes of operation (I-V) are measured and analyzed. The intrinsic transport noise is sizable and readily observed in the current time series measurements. The ensuing current spectrum ($S_I(f)$) exhibits a typical 1/f characteristics. It is observed that this noise amplitude scales with respect to current bias and indicative of mobility as well as number fluctuations at dielectric-semiconductor interface. FETs with leakage (lossy) dielectric layer indicate characteristic noise spectrum features which can serve as a diagnostic tool to monitor device stability. © 2015 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4936197]

I. INTRODUCTION

Solution processed, polymer based field effect transistors (FETs) have shown considerable progress over the last decade as a key component for printed electronics.¹ The device characteristics such as field effect mobility (μ_{FET}) and on-off ratio of these devices are controlled by the degree of structural order and defect densities which play a decisive role in charge transport of organic semiconductors.² The general mechanisms of transport, in case of semiconducting polymers, has been largely dealt in the framework of hopping between disordered-localized states.³ A direct manifestation of disorder in transport appears in the current fluctuations measured at time scales covering the trapping, releasing, and transit time duration.⁴ Time dependent fluctuations in current (noise) give insight into the energetic landscape traversed by charge carriers and can be analyzed in frequency domain as power spectrum density (PSD) plot. These variations, picked up by random arrival time of carriers at the electrode, can be classified to originate from number fluctuation (change in carrier density) or mobility fluctuations⁵ (trap-defects, lattice, grain-boundaries) or a combination of the two factors.^{6–8} The magnitude of the fluctuations also poses a fundamental device limit for operation. Noise studies of these devices are expected to be quite informative both at a fundamental level and for designing applications.

The semiconducting polymer, poly-3-hexyl-thiophene (P3HT) served as a model system to demonstrate various aspects of p-channel accumulation mode organic FETs (OFETs). There have been noise studies in small-molecule⁹⁻¹⁶ based thin film transistors (TFTs) as well as polymer based TFTs^{17–24} using SiO_x/HfO_x substrates as dielectrics. In the present case we focus on all polymer FETs (PFETs), and examine the effects of polymer dielectric-polymer semiconductor interfaces. In these PFETs, gate bias modulates charge carrier density at interface and a certain threshold voltage (V_{th}) marks the onset of channel formation by filling the deep trap states in the semiconductor (P3HT).²⁵ Thermally activated hopping mechanisms have been shown to dominate the transport process in P3HT with mobility increasing with temperature (T).²⁶ This trap mediated transport in P3HT-FETs is expected to have a sizable presence in the overall noise contribution.

Besides the intrinsic channel noise arising from semiconductor-dielectric interfacial states, the PFET architecture is susceptible to have noise contributions from the electrodes in the form of Schottky-type barriers and/or rough contacts (contact resistance), oxygen and moisture induced traps, and dielectric impurities that may result from device processing.^{15,16,19,23} Each contribution for these noise sources is expected to have a distinct noise signature (for example, white noise, generation-recombination noise) and there is a need for systematic studies to identify and possibly minimize these non-intrinsic contributions.

The current noise in PFETs is measured in different operating regimes (linear and saturation) and the observed noise spectrum shows 1/f type behavior in the low frequency range (4 Hz–1.6 kHz). PSD plots are correlated with carrier number and mobility fluctuations at the interface, as the dominant noise source in different regimes. The device performance of PFET, otherwise free from external impurities, is known to degrade gradually due to the factors which include bias stress and/or physiochemical changes of the materials.²⁷ The present studies also reveal correlation between leakage current magnitude and the noise exponent, which can thereby serve as monitor to probe degradation.

II. EXPERIMENTAL DETAILS

P3HT and the dielectric poly-vinylidene fluoride (PVDF) were commercially procured.²⁸ Devices were fabricated in bottom-gate top-contact (BGTC) architecture on the RCA cleaned glass substrates following standard procedure by coating aluminium as gate electrode using shadow mask technique.² Thin films of P3HT (\sim 50–100 nm) and PVDF

0021-8979/2015/118(20)/205502/5/\$30.00

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(~300–400 nm) were obtained by spin coating (800 rpm for 1 min) from their respective solutions (10 mg/ml in anhydrous chlorobenzene and 40 mg/ml in dimethyl formamide, respectively) followed by thermal annealing at 110 °C for 1 h inside glove box (N₂ atmosphere). The source-drain (SD) electrodes were deposited by coating gold (thickness 40 nm) using shadow mask. Fabricated devices were encapsulated before testing. The encapsulation process is detailed in the supplementary material.²⁹ The fabricated devices have long channel lengths ($L \sim 20-150 \,\mu$ m) with gold as SD electrodes which ensures that the contact resistance is lower than channel resistance.

The DC characteristics were measured by Keithley 4200 SCS. Noise measurements were carried out in electrically shielded and grounded environment. Rechargeable batteries were used for DC biasing of device under test (DUT). The output of the amplified current (from low-noise trans-impedance preamplifier, Femto DLPCA-200) was sampled by a dynamic signal analyzer (Agilent 35670A). The time series data is sampled above the Nyquist rate corresponding to upper frequency limit in the measurement range. The lower frequency limit is determined by the total time span of one sampled data set (or frame). Each frame is normalized by the gain at preamplifier before its Fourier transform, modulus square of which gives the PSD. The PSD is averaged by the total number of captured frames (50) for each set of results. The data processing and analysis were verified with waveforms captured in the signal analyzer, for periodic as well as aperiodic waveform. Control measurements verified the effectiveness of the electrical shielding with the background noise ($\sim 10^{-26}$ A²/Hz) largely limited by the preamplifier noise.

III. RESULTS AND DISCUSSION

The well-established BGTC based FETs in our laboratory which results in high performance, stable FETs were used for the present studies. Sizable number (>100) of devices were studied to arrive at a reliable and reproducible trend. Contact resistance of the devices was estimated by compact modeling procedure proposed by Tejada *et al.*^{29–32} and was found to be less than 2% of the channel resistance. The extracted parameters for the different set of devices used in noise studies are detailed in Table I.

The representative set of typical output and transfer curves of a transistor is depicted in Fig. 1.

Noise studies were specifically carried out on devices which exhibited stable response and relatively low hysteresis in DC characteristics. We examine the channel current fluctuations in two regimes (linear and saturation) of transistor



FIG. 1. (a) Output characteristics of an OFET chosen for noise studies (D2). (b) Transfer characteristics of the same device.

operation to evaluate the device processes, at different drainsource voltage (V_{ds}) and gate-source voltage (V_{gs}) . Data from SD current (I_{ds}) time series measurements were acquired in a systematic manner and initially analyzed using generalized Hooge's equation⁵ for conductivity fluctuations

$$S_I(f) = \alpha_H I^\beta / N f^\gamma, \tag{1}$$

 $S_I(f)$ represents the current PSD (A²/Hz), N is the total number of free charge carriers, β and γ are the exponents on I and f, respectively, while α_H represents Hooge's constant. The fundamental assumption here is that total noise results from random fluctuations of N independent charge carriers. It is observed that noise in I_{ds} results from carrier number fluctuation (Δ N or McWhorter model) and/or mobility fluctuation ($\Delta\mu$ or Hooge model). In PFETs, the number of free charge carriers, N at interface is controlled by V_{gs} ($\sim C_i WLV_{gs}^{eff}/q$) where V_{gs}^{eff} is the effective gate voltage and equals ($V_{gs} - V_{th}$) and is a device variable responsible for the carrier density modulation at the interface. The modified Hooge's framework for a-Si TFTs³³ can be adapted for the present case where PSD takes the following dependence with V_{gs}^{eff} , in linear regime:

$$S_I(f) \propto I_{ds}^2 / (V_{gs}^{eff})(1/f), \qquad (2a)$$

$$S_I(f) \propto I_{ds}^2 / (V_{gs}^{eff})^2 (1/f).$$
 (2b)

Equations (2a) and (2b) correspond to $\Delta \mu$ and ΔN models, respectively, and can be modified for saturation regime $(I_{ds} \propto (V_{gs}^{eff})^2)$ to obtain

$$S_I(f) \propto (V_{gs}^{eff})^3 (1/f), \tag{3a}$$

TABLE I. Extracted DC parameters of PFETs.

Device ID	Channel length, $L(\mu m)$	Channel width, W (mm)	Insulator capacitance, C_i (nF/cm ²)	Threshold voltage, V_{th} (V)	Saturation mobility, μ (cm ² /V s)	Reference figure(s)
D1	55	1.13	20	-15	2.02×10^{-3}	Fig. 2
D2	30	0.84	29	-15	1.06×10^{-3}	Figs. 1 and 3
D3	70	0.93	11	-10	$6.5 imes 10^{-3}$	Figs. 4 and S3
D4	68	1.74	15	+18	1.18×10^{-3}	Fig. S3

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$$S_I(f) \propto (V_{gs}^{eff})^2 (1/f). \tag{3b}$$

The validity of $\Delta \mu$ or ΔN model can be verified by estimating the exponent (*p*) on V_{gs}^{eff} , in different regimes.

In linear regime, noise is studied at different V_{ds} and V_{gs} (D1). The obtained spectrum (at different V_{gs}) (Fig. 2) shows a *l*/*f* type behavior as excess noise above thermal white noise background in the range 4 Hz-1.6 kHz. The γ value is close to 1 (1 \pm 0.1) and nearly independent of V_{gs} . In this case, it is seen that p value, in the relation $S_I/I^2 \propto (V_{gs}^{eff})^{-p}$, lies close to 2 (2 ± 0.2) (Fig. S2 in the supplementary material)²⁹ which suggests number fluctuation (Eq. (2b)) originating from the interfacial trap states as the dominant factor. For a constant V_{gs} (D2), the PSD increases as a function of V_{ds} (or I_{ds}) in the linear regime. Here, the exact nature of $S_{I}(f)$ is determined by the current exponent, β defining the slope of log-log plot (Fig. S3 in supplementary material).²⁹ The noise magnitude, in this case, varies linearly with current bias $(\beta \sim 0.9 \pm 0.1)$, and is largely independent of V_{gs} (inset Fig. S3 in the supplementary material).²⁹

For the transistor operated in saturation regime (D2) where V_{ds} is held constant (and is $>V_{gs}^{eff}$), the observed PSD response at different V_{gs} (Fig. 3) indicates that the noise form continues to exhibit 1/f type behavior with $\gamma \sim 1$ (1.1 ± 0.1). The $S_I(f)$ dependence on V_{gs}^{eff} which takes the form $S_I(f)$ $\propto (V_{os}^{eff})^p$ in saturation regime (inset Fig. 3 and Fig. S4 in the supplementary material),²⁹ reveals an exponent $p \sim 3$ (3.1 ± 0.1) which in this framework is representative of $\Delta \mu$ model (Eq. (3a)) and is suggestive of larger contributions from the bulk-disorder. From transistor equations²⁵ in saturation regime, $I_{ds} \propto (V_{gs}^{eff})^2$ hence expected value for $\beta \sim 1.5$ $(\beta = p/2)$ which is obtained by a log-log plot of PSD with respect to I_{ds} (Fig. S5 in the supplementary material).²⁹ Unlike the linear regime, the higher β value in saturation can be attributed to mixing of noise sources from the channel and the depleted region formed between pinch-off point and drain terminal. At a microscopic level, the magnitude of β (~1–2) can be interpreted to be a measure of mixing of various noise sources in the device or of the volume versus surface nature of the noise mechanism.^{11,34} It has been observed that for surface



FIG. 2. Relative noise spectra (RPSD) in linear regime of a PFET (D1) at different V_{gs} with V_{ds} at -10 V. Inset shows RPSD dependence on effective gate voltage, at frequency 20 Hz.



FIG. 3. Noise spectra (PSD) in saturation regime of a PFET (D2) at different V_{gs} with V_{ds} at -50 V. Inset shows PSD dependence on effective gate voltage, at 20 Hz.

trapping dominated events $\beta \sim 1$ and for bulk trapping events β is typically 1.5–2.³⁵

The α_H value can be understood as relative noise present in the system at 1 Hz and is used as a figure of merit to evaluate device performance. From earlier studies in homogenous samples, it was assumed to be a constant (~0.002) for all materials⁵ but has been observed to reduce drastically for ultrapure crystals (~10⁻⁷) whereas disordered materials show typically higher values (~1–1000).^{7,36} Present studies show α_H in the range of 4–50, consistent with earlier noise studies on OFETs but slightly higher as compared to oxide (dielectric) based OFETs.¹⁴ In saturation regime α_H is less (~5) and typically remains constant with V_{gs} while it decreases from 50 to 12 with V_{gs} , in the linear regime.

We clearly observe scaling down of relative noise with V_{gs}^{eff} (Fig. 2 inset) which essentially indicates the contribution of interfacial processes to the conductivity fluctuations. The mechanism of the trapping-detrapping at the interface appears to be predominant in linear regime, resulting in number-density fluctuations²⁰ as indicated by the fitting exponent, $p(\sim 2 \pm 0.2)$. On the contrary, noise in the saturation regime is dominated by the mobility fluctuation of charge carriers, based on the fitting parameters $(p \sim 3)$.³³

However, it is reasonable to expect that both mobility and number fluctuations are correlated in this system, since mobility is field dependent, and can contribute comparably to the total noise.¹² The trap distribution and energetics in the polymer dielectric may not be equivalent to oxide based dielectrics in the framework of McWhorter model.³⁷ It is likely that for disordered polymer semiconductors number fluctuations are a dominant noise source since the interface trap states are comparable to carrier density. Light as a source for increasing charge carrier density in a controlled selective way can in principle sort out the different contributions. Ongoing efforts in our laboratory are in this direction. Apart from the intrinsic transport mechanisms, the other aspect of sizable noise arising from intrinsic and external factors is in setting up the device performance limits. The external factors which are source for degradation and stability can overwhelm intrinsic features.

To demonstrate the efficacy of this approach in identifying different processes, we study PFETs (D2, D3, and D4) with different levels of gate dielectric leakage (I_{gs}) contributions. This was achieved by observing the magnitude of I_{gs} , in gate-source circuit while V_{ds} is open circuit (or float). In PFETs, it is observed to increase with the operation duration due to the factors such as bias stress, ionic transport, and electrode migration. The gradual increase in the leakage current is not readily observed in the FET characteristics, but is quite obvious in the PSD evolvement. The consequence is a lossy dielectric (reduced capacitance and higher conductance) which draws more power affecting the functioning of otherwise working transistors in an integrated environment. We systematically study the noise levels in these PFETs, at different biasing conditions, where I_{gs} values are comparable to I_{ds} (within one or two orders of magnitude) (Fig. 4). The DC characteristics of D3 and D4 show well defined linear and saturation regimes (Figs. S6 and S7 in the supplementary material)²⁹ similar to D2 in Fig. 1.

The features of these gate current contributions are the following: (i) PFETs with low leakage current are associated with $\gamma \sim 1$ and are stable over long period of time with the γ values maintained for a sustained period. (ii) Once degradation is ensued, γ takes up values >1 and gradually increases. (iii) γ and leakage current magnitude are directly correlated as indicated by V_{gs} dependent studies in the degraded PFETs (Figs. S8 and S9 in the supplementary material)²⁹ (iv) The *f*-range over the $1/f^{\gamma}$ also is observed with the sizable noise magnitude shifting to the lower side (<100 Hz).

These characteristic features, primarily, has its origin to the contribution from both I_{gs} and I_{ds} . Noise from dielectric has a spatially different origin from the channel and can be assumed to be uncorrelated implying that the charge carrier fluctuations are independent of each other in the two regions. The total spectrum, resulting from two uncorrelated noise sources, can be approximated as the sum of individual PSDs. The superposition of noise in I_{gs} ($S_{Igs}(f)$) and I_{ds} ($S_{Ids}(f)$) can give rise to the cross-over (~100 Hz). We associate the higher exponent to be a signature of particularly high I_{gs} ($\approx I_{ds}$) and the lower exponent value to fluctuations in I_{ds} .



IV. CONCLUSIONS

In summary, the noise output characteristics of OFETs exhibit the universal 1/f type behavior. The microscopic origin of the noise has contributions from both mobility and carrier number fluctuations in the channel originating from the interfacial trap states. The contributions from the gate leakage current to the output I_{ds} appears, with unique signature in the noise spectrum, in the form of higher exponent values in the low f range (<100 Hz). It is observed that for leakage-free devices $\gamma \approx 1$, and this magnitude of γ increases with an increase in the relative leakage component. Leakage-free devices clearly are more stable and exhibit 1/f noise ($\gamma \sim 1$) for prolonged period. These studies in the PFETs points out that low frequency noise analysis can be used to study the charge transport in disordered materials (dielectric and semiconductor) and monitor reliability and degradation.

ACKNOWLEDGMENTS

We acknowledge the financial support from DST and SERI project, Government of India.

- ¹H. Sirringhaus, Adv. Mater. **26**(9), 1319–1335 (2014).
- ²S. P. Senanayak, A. Z. Ashar, C. Kanimozhi, S. Patil, and K. S. Narayan, Phys. Rev. B **91**, 115302 (2015).
- ³S. D. Baranovskii, Phys. Status Solidi B 251(3), 487–525 (2014).
- ⁴M. Bag, N. S. Vidhyadhiraja, and K. S. Narayan, Appl. Phys. Lett. **101**(4), 043903 (2012).
- ⁵F. N. Hooge, IEEE Trans. Electron Devices **41**(11), 1926–1935 (1994).
- ⁶M. Weissman, Rev. Mod. Phys. 60, 537–571 (1988).
- ⁷A. K. Raychaudhuri, Curr. Opin. Solid State Mater. Sci. **6**(1), 67–85 (2002).
- ⁸L. K. J. Vandamme, IEEE Trans. Electron Devices **41**(11), 2176–2187 (1994).
- ⁹C. Bonavolontã, C. Albonetti, M. Barra, and M. Valentino, J. Appl. Phys. 110(9), 093716 (2011).
- ¹⁰C. Y. Han, L. X. Qian, C. H. Leung, C. M. Che, and P. T. Lai, J. Appl. Phys. **114**(4), 044503 (2013).
- ¹¹Z. Jia, I. Meric, K. L. Shepard, and I. Kymissis, IEEE Electron Device Lett. **31**(9), 1050–1052 (2010).
- ¹²H. Kang, L. Jagannathan, and V. Subramanian, Appl. Phys. Lett. **99**(6), 153702 (2011).
- ¹³L. Ke, S. Bin Dolmanan, C. Vijila, S. J. Chua, Y. H. Han, and T. Mei, IEEE Trans. Electron Devices 57(2), 385–390 (2010).
- ¹⁴P. V. Necliudov, S. L. Rumyantsev, M. S. Shur, D. J. Gundlach, and T. N. Jackson, J. Appl. Phys. 88(9), 5395–5399 (2000).
- ¹⁵Y. Xu, F. Balestra, J. A. Chroboczek, G. Ghibaudo, T. Minari, K. Tsukagoshi, R. Gwoziecki, and R. Coppard, in *International Conference on Noise and Fluctuations (ICNF)* (2011), pp. 57–60.
- ¹⁶Y. Xu, C. Liu, W. Scheideler, S. Li, W. Li, Y.-F. Lin, F. Balestra, G. Ghibaudo, and K. Tsukagoshi, IEEE Electron Device Lett. **34**(10), 1298–1300 (2013).
- ¹⁷K. Y. Choo, S. V. Muniandy, C. L. Chua, and K. L. Woon, Org. Electron. 13(8), 1370–1376 (2012).
- ¹⁸M. J. Deen, O. Marinov, S. Holdcroft, and W. Woods, IEEE Trans. Electron Devices **48**(8), 1688–1695 (2001).
- ¹⁹O. D. Jurchescu, B. H. Hamadani, H. D. Xiong, S. K. Park, S. Subramanian, N. M. Zimmerman, J. E. Anthony, T. N. Jackson, and D. J. Gundlach, Appl. Phys. Lett. **92**(13), 132103 (2008).
- ²⁰H. Kang and V. Subramanian, Appl. Phys. Lett. **104**(2), 023301 (2014).
- ²¹L. Ke, S. B. Dolmanan, L. Shen, C. Vijila, S. J. Chua, R.-Q. Png, P.-J. Chia, L.-L. Chua, and P. K. H. Ho, J. Appl. Phys. **104**(12), 124502 (2008).
- ²²L. Ke, S. B. Dolmanan, L. Shen, C. Vijila, S. J. Chua, R.-Q. Png, P.-J. Chia, L.-L. Chua, and P. K. H. Ho, Appl. Phys. Lett. **93**(15), 153507 (2008).
- ²³O. Marinov, M. J. Deen, J. Yu, G. Vamvounis, S. Holdcroft, and W. Woods, Circuits, IEE Proc. Devices Syst. 151(5), 466–472 (2004).
- ²⁴L. K. J. Vandamme, R. Feyaerts, G. Trefan, and C. Detcheverry, J. Appl. Phys. 91(2), 719–723 (2002).

- ²⁵J. Zaumseil and H. Sirringhaus, Chem. Rev. **107**(4), 1296–1323 (2007).
- ²⁶J.-L. Bredas, D. Beljonne, V. Coropceanu, and J. Cornil, Chem. Rev. **104**(11), 4971–5004 (2004).
- ²⁷H. Sirringhaus, Adv. Mater. **21**(38–39), 3859–3873 (2009).
- ²⁸S. P. Senanayak, S. Guha, and K. S. Narayan, Phys. Rev. B **85**(11), 115311 (2012).
- ²⁹See supplementary material at http://dx.doi.org/10.1063/1.4936197 for device encapsulation process, contact resistance estimation, power spectrum dependence with gate voltage, transistor DC curves, and gate leakge current spectrum.
- ³⁰O. Marinov, M. J. Deen, U. Zschieschang, and H. Klauk, IEEE Trans. Electron Devices **56**(12), 2952–2961 (2009).
- ³¹J. A. J. Tejada, J. A. L. Villanueva, P. L. Varo, K. M. Awawdeh, and M. J. Deen, IEEE Trans. Electron Devices 61(2), 266–277 (2014).
- ³²M. J. Deen, O. Marinov, U. Zschieschang, and H. Klauk, IEEE Trans. Electron Devices 56(12), 2962–2968 (2009).
- ³³D. Rigaud and M. Valenza, J. Rhayem, IEE Proc. Circuits, Devices Syst. 149(1), 75–82 (2002).
- ³⁴A. van der Ziel, Proc. IEEE **76**(3), 233–258 (1988).
- ³⁵S. Martin, A. Dodabalapur, Z. Bao, B. Crone, H. E. Katz, W. Li, A. Passner, and J. A. Rogers, J. Appl. Phys. **87**(7), 3381–3385 (2000).
- ³⁶F. N. Hooge, T. G. M. Kleinpenning, and L. K. J. Vandamme, Rep. Prog. Phys. 44(5), 479–479 (1981).
- ³⁷L. K. J. Vandamme and F. N. Hooge, Phys. B **357**(3–4), 507–524 (2005).