Dielectric and Interface Engineering Strategies for Polymer Field Effect Transistors

A Thesis Submitted in Partial Fulfillment for the Requirements of the Degree of

Doctor of Philosophy

by

Satyaprasad P. Senanayak

Chemistry and Physics of Materials Unit,
Jawaharlal Nehru Centre for Advanced Scientific Research
(Deemed University)
Bangalore - 560 064,
India.

JULY 2014

Dedicated to my Family...

Declaration

I hereby declare that the matter embodied in the thesis entitled "***Dielectric and Interface Engineering Strategies for Polymer Field Effect Transistors***" is the result of investigations carried out by me at the Chemistry and Physics of Materials Unit, Jawaharlal Nehru Centre for Advanced Scientific Research, Bangalore, India under the supervision of Prof. K. S. Narayan and that it has not been submitted elsewhere for the award of any degree or diploma. In keeping with the general practice in reporting scientific observations, due acknowledgment has been made whenever the work described is based on the findings of other investigators.

Satyaprasad P. Senanayak

JAWAHARLAL NEHRU CENTRE FOR ADVANCED SCIENTIFIC RESEARCH
Jakkur, Bangalore 560064, India

K. S. NARAYAN
Professor and Dean (R&D)
PHONE: 91 80 22082822
FAX: 91 80 22082766
e-mail: narayan@jncasr.ac.in URL: www.jncasr.ac.in/narayan

July 28th, 2014

Certificate

I hereby certify that the matter embodied in this thesis entitled "***Dielectric and Interface Engineering Strategies for Polymer Field Effect Transistors***" has been carried out by Mr. Satyaprasad P. Senanayak at the Chemistry and Physics of Materials Unit, Jawaharlal Nehru Centre for Advanced Scientific Research, Bangalore, India under my supervision and that it has not been submitted elsewhere for the award of any degree or diploma.

Prof. K. S. Narayan
(Research Supervisor)

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Satyaprasad P. Senanayak

JNCASR, Bangalore

Synopsis

Low-cost, large-area, solution-processability and roll-to-roll printing are the salient features of polymeric devices which are emerging as a powerful technology option for embedding electronic functionality onto flexible substrates. Polymer field effect transistors (PFETs) form the basic building block of flexible electronics. The performance parameter of a PFET is mainly governed by the field effect mobility (μ_{FET}) of charge carriers, switching speed (t_{switch}), operating voltage and power consumption. For PFETs to complement conventional electronics its performance should be comparable with conventional inorganic electronics. This thesis addresses two major themes of PFET research, namely the transport interface tuning and dielectric engineering. A combination of optimized device architecture and the strategy of modifying the interface from the semiconductor as well as dielectric side are utilized to obtain PFETs with performance comparable to a-Si based field effect transistor devices.

The first part of the thesis deals with obtaining a general guideline for band-like transport in PFETs. With the advent of new class of DPP based materials it is possible to obtain $\mu_{FET} > 1$ $cm^2V^{-1}s^{-1}$ for polymer devices. According to the classical theory for van der Waals solid it is expected that band-like transport would be feasible for polymeric disordered materials at such high μ_{FET}. Noting this prediction, studies were carried to understand the molecular origin of high μ_{FET} in one such amphiphillic DPP (2DPP-TEG) based polymeric material. The amphiphillic design of the polymer results in microscopic structures with interconnected aggregates and co-planar conjugate core with low re-organization energy. Transport studies performed on PFETs fabricated with 2DPP-TEG molecule and low-*k* dielectric material indicates a negative coefficient of μ_{FET}. This negative coefficient of μ_{FET} originates from the inherent transport of the system and not from external factors like water related traps, bias stress or any structural and glass transition of the dielectric/semiconductor layer. In addition, the observed equivalence of μ_{Hall} and μ_{FET} as well as the evidence pointing to delocalized charge carriers indicate a clear band-like transport mechanism in this polymer. Comprehensive studies on a range of dielectric materials lead us to the unifying the requirements for band transport, which

includes: rationale molecular design, optimum transport interface, interconnected aggregates and co-planar conjugated core of the polymer.

The next part discusses, the origin of disorder in high-*k* dielectric based PFETs. Presence of high-*k* dielectric material in the PFET device structure results in broadening of the density of states and increase in the effective mass of charge carriers of the semiconductor. However, it is not clear whether the disorder at the interface is related to the dielectric constant or the nature of dielectric material. To answer this question, PFETs were fabricated with PVDF based dielectric materials which fall in different class of ferroelectric (FE), paraelectric (PE) and random paraelectric (r-PE) dielectric material which have similar *k*. Temperature dependent study exhibits a weak activation behavior of 15 meV for FE-FETs which increases to 0.1 – 0.2 eV for PE dielectric based PFETs. This weak activation behavior in FE-FETs is attributed to the collective domain fluctuation of the FE dielectric. Thus, the electrostatic disorder at the transport interface of a PFET is dependent on the nature of dielectric material and not the dielectric constant.

In the subsequent section, the ordered interface obtained from FE material is employed for enhancing the transient response of PFETs. However, the high polarization in FE can result in slow relaxation which gets reflected in the slow switching behavior of FE-FETs. This dielectric limited response is circumvented by a combination of dipole and device engineering. The procedure involves pre-poling the FE dielectric to initiate the domain nucleation which is the slowest step in the switching dynamics of polymer FE material. Parasitic capacitance is minimized by fabricating devices with aligned patterned electrodes which further increases the operating frequency of PFETs. These modified device structures and the corresponding all-polymer logic circuits demonstrate switching frequency of 4 MHz at printable channel lengths. A range of dielectrics and semiconducting materials are studied to obtain the limiting factors for the switching mechanism of PFETs. These studies indicate that the requisites for fast switching polymer circuits as: ordered dielectric dipole, semiconductors with high μ_{FET} and isolated conjugated core.

In general, PFETs have a high operating voltage which limits its usability in portable applications. The final section of the thesis deals with a strategy for obtaining high performing PFETs with low-operating voltage. A strategy based on multilayered self-assembled nano-dielectric (SAND) structure with precise control on thickness, leakage current (0.1 pA) and capacitance (0.4 – 0.8 $\mu F/cm^2$) is utilized to obtain PFETs operating at 1 V with typical μ_{FET} ~ 2.4 $cm^2V^{-1}s^{-1}$. Furthermore, these structures are utilized to obtain large area polymer logic circuits with switching frequency of ~ 5 MHz. The origin of the high

performance low operating voltage PFETs can be attributed to the combination of optimum transport interface, densely packed ordered dipoles and effective combination of atomic, molecular and ionic polarization. In addition, the SAND structure provides a functional interface to modulate the polarization by optical and electrical control. Azo-group based photo-isomerization procedure is explored to follow the variation of the transport interface with UV and visible illumination. This functionality of the interface is then utilized to design optoelectronic memory with digitally commutable electrical and optical response.

In summary, the thesis reports a combination of strategies to obtain PFETs with performance comparable to a-Si based FETs.

List of Publications

- **Satyaprasad P. Senanayak**, Ashar A.Z **,** K. Kanimozhi, Satish K. Patil and K.S.Narayan; "*Low disorder and observation of band like transport in high mobility ambipolar polymer"*; **Nature Communication (under review)** (2014) .

- **Satyaprasad P. Senanayak** and K.S.Narayan; "*Strategy for fast switching in all polymer field effect transistors*" **Advanced Functional Materials,** 24 (22), 3324-3331, (2014).

- **Satyaprasad P. Senanayak**, S. Guha and K.S.Narayan; "*Polarization fluctuation dominated electrical transport processes of polymer-based ferroelectric field effect transistors"*; **Physical Review B**, 85 , 115311, (2012).

- **Satyaprasad P. Senanayak**, Vinod K.Sangwan, Julian J McMorrow, Zhihua Chen, Antonio Fachetti, Mark Hersam, Tobin J Marks and K. S. Narayan; "*Self-assembled Nanodielectrics for Fast-Switching Low-Voltage Polymer Logic circuits"* (2014) **(Nanoletters submitted)**.

- **Satyaprasad P. Senanayak**, Vinod K.Sangwan, Julian J McMorrow, Zhihua Chen, Antonio Fachetti, Mark Hersam, Tobin J Marks and K. S. Narayan; "*Origin of polarization in Self-assembled Nanodielectrics: Impact on charge transport*" (2014) (manuscript under preparation).

- Suresh Vasimalla, **Satyaprasad P. Senanayak**, Meenakshi Sharma, K. S. Narayan and Parameswar Krishnan Iyer; *"Improved Performance of Solution-Processed n-Type Organic Field-Effect Transistors by Regulating the Intermolecular Interactions and Crystalline Domains on Macroscopic Scale";* **Chemistry of Materials**, (In Press) (2014).

- Ashish Kumar Asatkar, **Satyaprasad P. Senanayak**, Anjan Bedi, Snigdha Panda, K S Narayan and Sanjio S Zade; "*Zn(II) and Cu(II) Complexes of Thiophene-Based Salphen-Type New Ligand: Solution-Processable High-Performance Field-*

Effect Transistor Materials"; **Chemical Communication**, 50 (53), 7036-7039 (2014).

- B Narayan, **Satyaprasad P. Senanayak**, Ankit J, K.S.Narayan and S.J.George; **"***Self-assembly of π-Conjugated Amphiphiles: Free Standing, Ordered Sheets with Enhanced Mobility*"; **Advanced Functional Materials**, 24, 3053-3060 (2013).

- Palas Baran Pati, **Satyaprasad P. Senanayak**, G. Ramakrishna, C. M. Reddy, K. S. Narayan and Sanjio S. Zade ; "*Solution Processable Benzooxadiazole and Benzothiadiazole Based D-A-D Co-oligomer Field Effect Transistors: a Structure Property Relationship"*; **ACS applied materials & interfaces** 5 (23), 12460-12468 (2013).

- Anjan Bedi, **Satyaprasad P. Senanayak**, G. Ramakrishna, C. M. Reddy, K.S. Narayan, Sanjio S. Zade; "*Synthesis of solution-processable alternate polymer of cyclopenta[c]selenophene and ethylene and its thiophene analogue: their charge transport properties and comparative study"*; **Macromolecules**, 46 (15), 5943-5950 (2013).

- Anjan Bedi, **Satyprasad P. Senanayak**, K.S. Narayan, Sanjio S. Zade; "*Synthesis and characterization of copolymers based on cyclopent [c]thiophene and bithiazole and their transistor properties*"; **Journal of Polymer Science Part A: Polymer Chemistry**, 51 (20), 4481-4488 (2013).

- N. B. Ukah, **Satyaprasad P. Senanayak**, D. Adil, G. Knotts, J. Granstrom, K. S. Narayan, and S. Guha ; "*Enhanced mobility and environmental stability in all organic field-effect transistors : the role of high dipole moment*"; **Journal of Polymer Science Part B: Polymer Physics** 51 (21), 1533-1542 (2013).

- K.S.Narayan, Madhushankar, Vini G, **Satyaprasad P. Senanayak** and Ravichandran S; "*Water gated Phospholipid - Monolayer Organic field effect*

transistor through modified Mueller-Montal method"; **IEEE Electron Device Letters**, 99, 1-3 (2013).

- Nagesh B. Kolhe, R. Nandini Devi, **Satyaprasad P. Senanayak**, B. Jancy, K. S. Narayan and S. K. Asha; *"Structure Engineering of Naphthalenediimides for improved Charge Carrier Mobility: Self-assembly by Hydrogen Bonding, Good or Bad?'"*; **Journal of Materials Chemistry**, 22, 15235 - 15246 (2012).

- Anjan Bedi, **Satyaprasad P. Senanayak**, Soumyajit Das, K. S. Narayan and Sanjio S. Zade; *"Cyclopenta[c]thiophene oligomers based solution processable D–A copolymers and their application as FET materials"*; **Polymer Chemistry**, 3(6), 1453 - 1460 (2012).

- Soumyajit Das, **Satyaprasad P. Senanayak**, Anjan Bedi, K.S. Narayan and Sanjio S. Zade; *"Synthesis and charge carrier mobility of a solution-processable conjugated copolymer based on cyclopenta[c]thiophene"*; **Polymer**, 52, 5780 - 5787 (2011).

- Nagesh Kolhe**, Satyaprasad P. Senanayak**, K. S. Narayan and S. K. Asha; *"n-Type Field Effect Transistors Based on Rigid Rod and Liquid-Crystalline Alternating Copoly(benzobisoxazole) Imides Containing Perylene and/or Naphthalene"*; **J. Phys. Chem. B**, 114, 16694 - 16704 (2010).

- Geeta Saini, **Satyaprasad P. Senanayak**, Josemon Jacob and K. S. Narayan; "*Synthesis, characterization and OFET characteristics of 3,4-diaryl substituted poly(thienylene vinylene) derivatives*"; **Polymer Bulletin**, 1007, 1 - 9 (2010).

List of Patents

- Metal Organic Complex, Devices and Method.
  Inventor : Prof. Sanjio Shankarrao Zade, Prof. Kavassery Sureswaran Narayan, Dr. Ashish Kumar Asatkar, **Satyaprasad Premswarup Senanayak**

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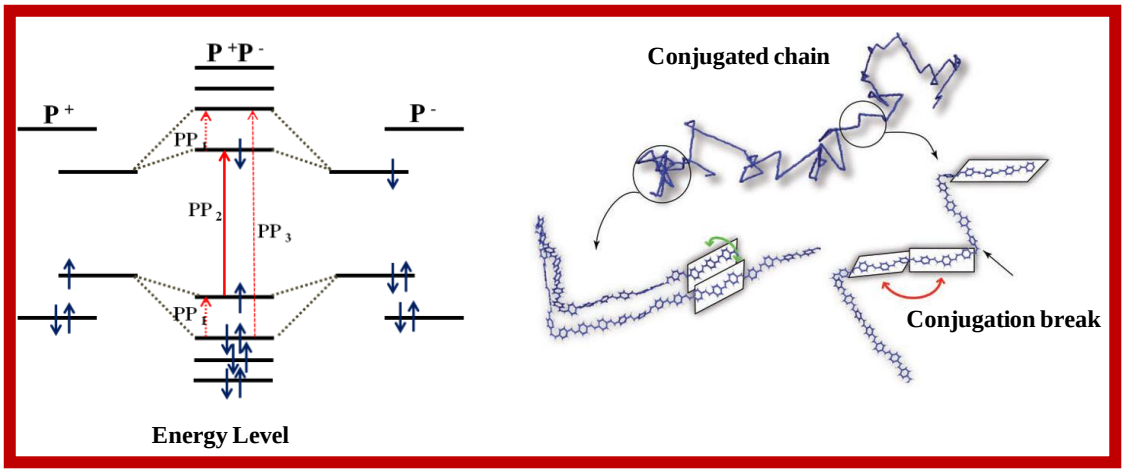
Notations/Abbreviations

FET	Field Effect Transistor
TFT	Thin Film Transistor
PFET	Polymer Field Effect Transistors
a-Si, p-Si	Amorphous Silicon, Polycrystalline Silicon
VRH	Variable Range Hopping
ME	Mobility Edge
MTR	Multiple Trap Release
HOMO	Highest Occupied Molecular Orbital
LUMO	Lowest Un-occupied Molecular Orbital
GIXRD	Grazing Incidence X-ray Diffraction
FE	Ferroelectric
PE, r-PE	Paraelectric, random-Paraelectric
SCLC	Space Charge Limited Current
DSC	Differential Scanning Calorimetry
FTIR	Fourier Transform Infra-Red Spectroscopy
ALD	Atomic Layer Deposition
NLS	Nucleation Limited Switching
MIM	Metal-Insulator-Metal
MFSM	Metal-Ferroelectric-Semiconductor-Metal
DOOS	Density of Occupied States
PLC	Polymer Logic Circuit
SAM	Self Assembled Monolayer
SAND	Self Assembled Nano Dielectric
SAP	Self Assembled Photochromic

Chapter 1

Introduction



Chapter 1

Introduction

1.1 Field Effect Transistors

Conventional microelectronics has been the driving force for modern electronic devices, sensors, displays and energy sources. Semiconductors such as inorganic silicon and gallium arsenide, insulators like silicon dioxide, and metals such as aluminum, copper and gold have been the backbone of the semiconductor industry. The level of device fabrication has grown from small-scale integrated circuits to very large-scale integrated circuits which have resulted in efficient circuitry, faster switches and better color rendering in displays. The fundamental building block of microelectronics is the field effect transistor (FET).

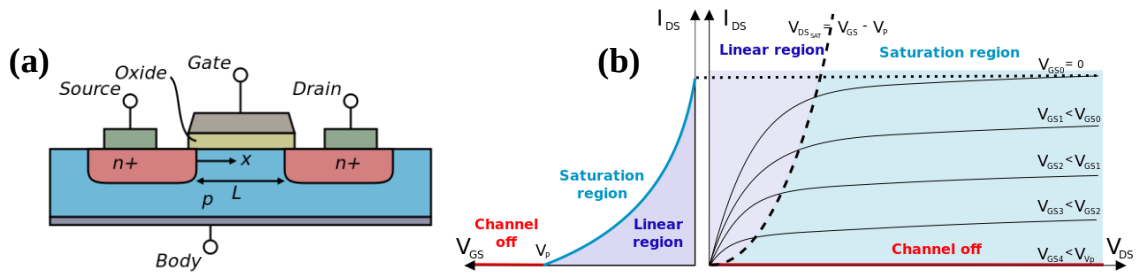


Figure 1.1: (a) *Schematic of a typical FET;* ***(b)*** *operation of conventional inorganic FETs (reproduced from Reference 1).*

FETs are a revolutionary invention which is considered a landmark for the growth of modern microelectronics. The FET device structure consists of three electrodes (gate, source and drain), semiconducting layer and the insulating layer[1]. The source-drain electrodes are used for charge-injection, and charge-transport occurs through the semiconductor upon applying voltage (**Figure: 1.1a**). The gate electrode is isolated from the active semiconductor by a thin dielectric layer, which is utilized to induce charges at the semiconductor-dielectric interface under the influence of the applied gate bias. Thus, the

operation of metal-insulator-semiconductor FET (MISFET) is based on the control of charge density at the transport layer by capacitive coupling with external voltage.

High electric field at the interface results in the bending of the energy levels of the semiconductor (**Figure: 1.2**). This bending of bands results in accumulation of majority charge carriers at the interface that provides a highly conducting (on) state, called the accumulation or enhancement mode. On the other hand, upon applying the opposite gate bias, the majority carriers are pushed away from the interface due to opposite band bending, and carriers are depleted from the interface. This corresponds to the depletion mode of operation which has low conduction (**Figure: 1.2b**). Similarly, inversion regime of operation is also observed by generating minority carriers at the interface.

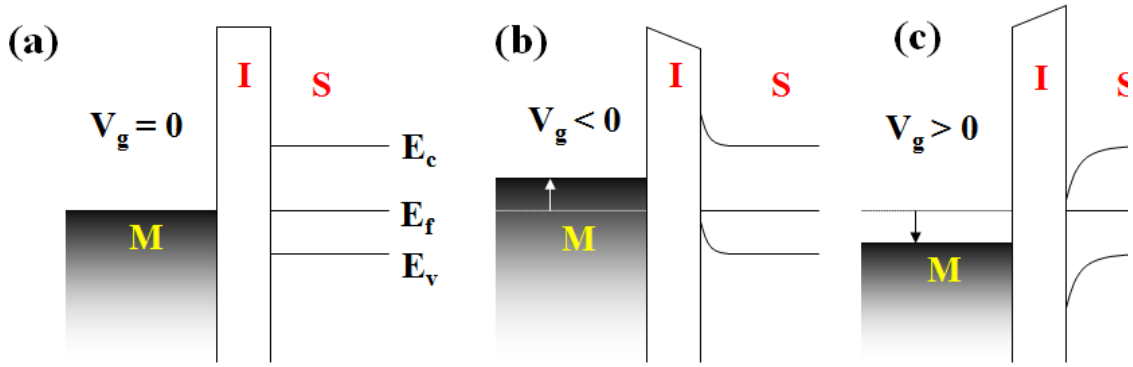


Figure 1.2: *Schematic of band-bending at the semiconductor-dielectric interface for n-FETs under the influence of (a) no gate bias (b) depletion bias (c) accumulation bias.*

A MISFET is mainly characterized by the charge carrier mobility (μ_{FET}), the switching speed (t_{switch}), sub-threshold swing (SS) and on/off ratio[1]. Each of these parameters is dependent on the device structure, the semiconducting layer, the insulating layer and the electrodes. The active material used in conventional inorganic FETs is predominantly crystalline-Si or III-V semiconductors. These devices have a typical μ_{FET} ~ 10^3 – 10^5 $cm^2V^{-1}s^{-1}$, t_{switch} ~ 0.27 ns, SS ~ 70 mV/dec and on/off ratio ~ 10^8. Expensive fabrication process of the active material and scarcity of large wafers deterred the advancement of the technology. This lead to the next generation of the microelectronic devices referred as the thin film transistor (TFT) technology, which is based on hydrogenated amorphous Si (*a*-Si) and polycrystalline Si (*p*-Si)[2]. With the development of these devices it was possible to have a scalable production of FET. However, the inherent disorder in these TFT's reduced the maximum mobility to the order of 1 cm^2 V^{-1} s^{-1}. In spite of these developments, the inherent limitations of obtaining flat semiconducting

wafers prevented the usage of inorganic microelectronics for applications involving large area and flexible substrates. Moreover, the fabrication process requires extensive clean room and lithographic facilities, which is expensive and time consuming. Furthermore, downscaling and improving the performance of inorganic electronics is reaching an end due to limits from lithographic techniques, hence different avenues have to be explored to complement this technology. A range of new materials like carbon nanotubes, metal-dichalcogenides, graphene, amorphous oxides and organic materials have been explored for making electronic devices. Alongside, novel device fabrication techniques like vertical field effect transistors have also been tried in this regard. These new generation materials now demonstrate electrical performance comparable to inorganic devices. The studies in this thesis focus on the understanding of the charge transport in one such new generation material the organic polymers.

1.2 Polymer Devices

Polymer electronics has garnered significant interest as a key active component in developing embedded circuits on flexible substrates. Over the last few decades, organic and polymer electronics has evolved as a complement to inorganic circuitry, since these materials cannot surpass the performance parameters of conventional crystalline semiconductors[3]. Despite the issue of low performance, organic electronics provides additional advantages of embedding molecular functionalities in a controlled manner by new synthesis techniques which adds novel properties to the materials.

Polymer diodes demonstrated by Heeger et.al was one of the early efforts in the direction of fabricating electronic components[4]. This was followed by the demonstration of polymer light emitting diodes[5], organic photovoltaics[6], and field effect transistors[7]. Polymer devices have the advantage of cheap and ambient fabrication procedure without any need of extensive clean room based technologies as well as easy tuning of the optical and electronic properties. The main hindrance in the development of polymer electronics is the stability of the polymer devices. This issue has been mitigated to a large extent by the synthesis of new materials which demonstrate reliable performance under ambient condition[8]. With consistent efforts, the performance of polymer devices has reached a level which clearly exceeds the performance parameters of the benchmark *a*-silicon based devices[9]. This impeccable development of polymer electronics is attributed to a combination of novel device architecture and new materials design which is driven by the understanding of the

transport physics of these materials[10]. The subsequent sections provide a brief overview of the growth of polymer electronics in the last few decades.

1.2.1 Charge Transport in Polymers

Conjugated polymers are organic macromolecules which consist of at least one backbone chain of alternating double and single bonds. In these materials, the C atoms are three-fold coordinated (e.g. polyacetylene) leading to sp^2 hybridization. Three equivalent orbitals, $2s^1$ $2p_x^1$ $2p_y^1$ bind with nearest neighbors creating three co-planar strong σ-bonds, directed at 120° to each other. The remaining orbital $2p_z^1$ of each C atom overlaps with the other by a weaker π-bond, in the direction perpendicular to the sp^2 hybridized plane. These polymer chains behave as quasi 1-D metal with half-filled band. However, the instability of a 1-D metal against periodic lattice distortion as predicted by the Peierl's instability leads to dimerization or interchain interactions in these materials[11]. The interaction between the polymeric chains occurs via weak van der Waal's forces which is different from the strong covalent bonding seen in inorganic semiconductors[12]. Molecular orbital theory predicts when two atoms bond to form a molecule, the atomic orbitals overlap forming bonding (lower energy) and antibonding (higher energy) orbitals also referred as the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO). These energy levels resemble the valence and conduction band of a semiconductor. The band gap in a polymer depends upon factors like aggregation, microstructure and crystallinity of the polymer. A schematic illustration of this is shown in **Figure: 1.3**.

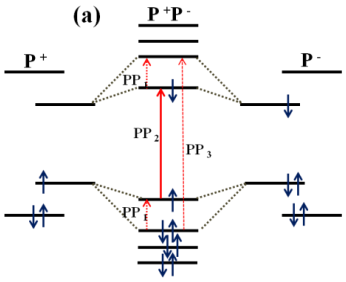


Figure 1.3: *(a) Schematic of the molecular orbitals in a polymer. Reproduced from Science 2009, 323, (5912), 369-373 with the permission from AAAS.*

Various approaches have been suggested to explain the charge transport in polymeric materials. The transport models for these materials are derived from the observed behavior in disordered or amorphous inorganic materials[13]. These transport models can be classified as microscopic transport models which require atomic levels with first principle

modeling and the macroscopic transport models where the device parameters can be directly mapped.

A) Microscopic Transport models

Polymer based soft materials, which are weakly bonded by van der Waals interaction are expected to have transport properties intermediate to hopping based amorphous glasses and covalently bonded crystalline systems[3b, 14]. The most acceptable theory for transport in polymers is based on the hopping of charges through trap sites. Disorder in polymer chains, leads to localization of the states and transport takes place via hopping between the localized states with the assistance of molecular distortion. The charge transport then occurs through quasi particles called polaron which is a combination of electron and phonons.

Polarons which originate due to the inherent self localized excitations involved in the charge transport are called the Holstein polarons[15,16] and the polarons which originate due to extrinsic factors like the existence of polarization cloud are called the Froehlich polarons[13]. These polarons can be positively or negatively charge with a ½ spin state. The existence of strong electron-phonon coupling in the polymer semiconductors is responsible for the existence of polarons. The strength of the electron-phonon coupling decides the radius of the polaron. Due to polarons in the semiconducting layer, additional levels are created symmetrical to the Fermi level. Typical energy level and types of polarons are shown in **Figure: 1.4**. The location of the energy levels is dependent on the length of the polymer chain. The transition between the polaronic levels is governed by selection rules which require parity transformation. The presence of polarons is evident from experiments involving electron spin resonance and transient absorption[17].

The hopping mechanism of a polaron from one site to another is generally thermally activated and is given by:

$$\mu = \frac{ea^2}{k_b T} \frac{\sqrt{\pi}\, J^2}{h\sqrt{2E_b k_b T}} \exp\left(\frac{-E_b}{k_B T}\right) \qquad \text{..... (1.1)}$$

where, T is the temperature, J is the nearest-neighbor interaction energy, and E_b is the polaron binding energy.

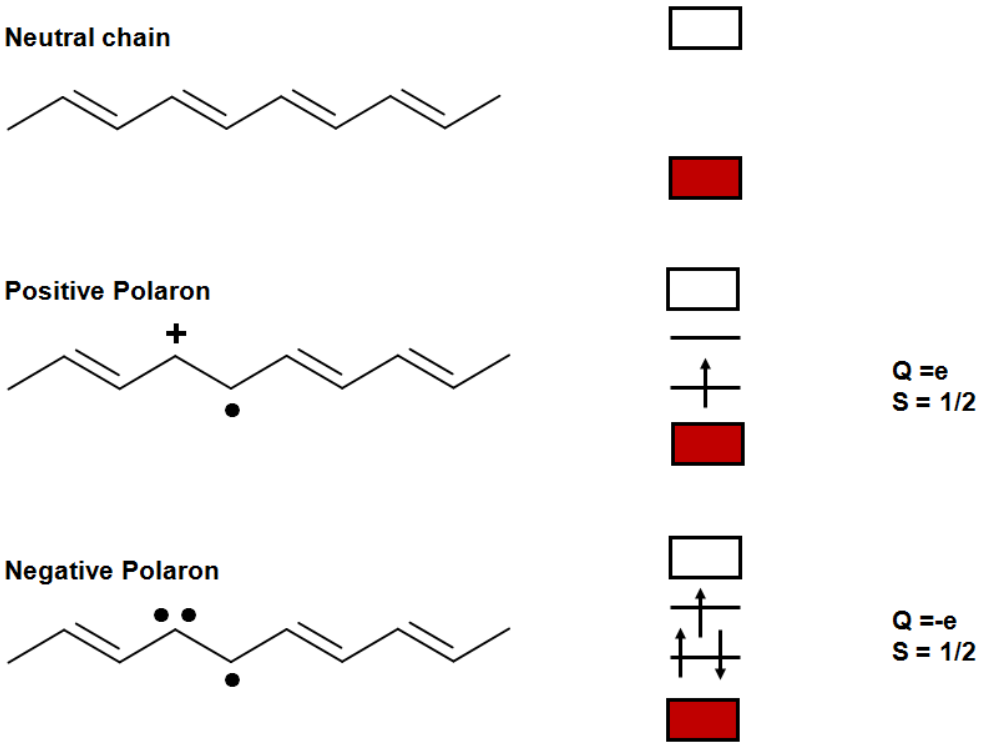


Figure 1.4: *Various types of polarons with their spin and charge state.*

Two types of hopping processes are observed from polymer transport namely fixed range hopping or the Miller-Abraham hopping and variable range hopping.

a) Miller-Abraham Hopping

In the case of fixed range hopping, proposed by Miller and Abraham[18] (M-A) for lightly doped semiconductors at a low temperature, the hopping rate is given by:

$$\Gamma_{ij} = \vartheta_o \, exp\left(\frac{-2\,R_{ij}}{a}\right) exp\left(-\frac{(E_i - E_j)}{k_B T}\right) \qquad \text{……..(1.2)}$$

where, υ_0 is a constant related to phonon density of states, a is the localization length and R_{ij} is the distance between sites i and j with energy E_i and E_j. The first exponential term expresses the tunneling probability, indicating that at low doping levels of the semiconductors, the probability for an electron to jump from one site to another decrease exponentially. The second exponential term accounts for the temperature dependence of the hopping rate. Typical transport in hopping mechanism is thermally activated with an activation energy given by the difference in energy between the hopping sites. This treatment of fixed range hopping is useful for describing transport in 1-D fibrillar structures

obtained for P3HT based systems and systems which obey 1 D transport models like Luttinger-Liquid[19].

b) Mott's Variable Range Hopping

If the hopping process between the nearest neighbors is not energetically favorable, charge carriers tend to hop to a larger distance than the nearest neighbor and occupy an energetically more favorable state. This process is referred as the variable range hopping (VRH). VRH is generally preferred for homogeneous systems with 2D or 3D transport. In order to have conductance in these solids the spatial distance between the two states has to be optimized. From the Mott's approach[20], the average energy spacing between states near Fermi energy level is given by:

$$W = \frac{3}{4\pi R^3 N(E_F)} \qquad \text{…….. (1.3)}$$

The average hopping distance can be estimated as

$$R_{avg} = \left[\frac{9}{8\pi\alpha N(E_F) k_B T}\right]^{\frac{1}{4}} \qquad \text{…….. (1.4)}$$

And the conductivity is obtained as

$$\sigma = \sigma_0(T) \exp\left[\left(\frac{T_o}{T}\right)^{\frac{1}{4}}\right] \qquad \text{…….. (1.5)}$$

This expression is the Mott's law for hopping transport in 3D system. T_o is related to the broadening of DOS, α is the inverse delocalization radius and $N(E_F)$ is the density of localized states at the Fermi level E_F.

In general, the conductivity for any *d*-dimensional system the can be expressed as:

$$\sigma = \sigma_0(T) \exp\left[\left(\frac{T_o}{T}\right)^{\frac{1}{d+1}}\right] \qquad \text{…….. (1.6)}$$

It should be noted that Mott's VRH model is based on several simplified assumptions that the DOS is independent of energy at E_F and no correlation exists between the tunneling process and electron-electron interactions. When the Coulomb interaction between the electrons is strong, a linear gap opens up in the DOS at E_F. In the regime of strong Columbic interaction, the conductivity is given as

$$\sigma = \sigma_0(T) \exp\left[\left(\frac{T_o}{T}\right)^{\frac{1}{2}}\right] \qquad \text{…….. (1.7)}$$

and the broadening of the Gaussian DOS is expressed as:

$$T_o = 6.2\ \frac{e^2}{k_B \varepsilon \xi} \qquad \text{…….. (1.8)}$$

where ε and ξ are the dielectric constant and the localization length respectively. It has been reported that when VRH is assisted by electron-electron interaction, a universal conductivity factor $\sigma_0 \approx e^2/h$ is obtained which is independent of temperature[21].

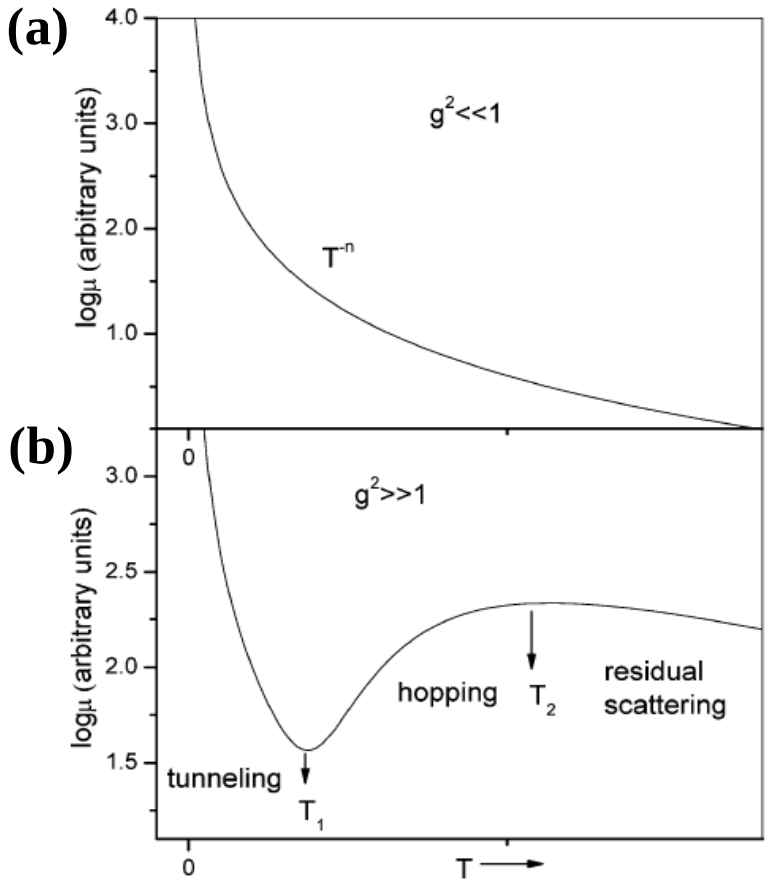


Figure 1.5: *Temperature dependence of the mobility predicted from the polaron model for the limiting case of (a) weak and (b) strong coupling regime. g represents the electron-phonon coupling strength. (Reproduced with permission from reference 23)*

The hopping theory predicts the existence of band-like delocalized transport in a molecular system if the time between the electron hops is much less than the scattering time[14c]. This leads to the minimum condition of mobility $(\mu_{min}) > \frac{er^2}{2\hbar}$, where r is the intermolecular distance, e is the electronic charge and $\hbar$ is the reduced Plank's constant[22]. Depending on the coupling between the electron-phonon (g), the condition for band-like temperature dependence is observed in different T regimes. In the weak coupling regime (g << 1), the transport is dominated by tunneling and displays a band-like power law

dependence of μ_{FET} (~ T^{-n}) in the complete T range. For intermediate coupling, the μ_{FET} is band-like at low T and as the hopping contribution increases, a weaker T dependence is observed. However, in the strong-coupling regime (g >> 1), three regimes of transport are obtained. At low T, μ_{FET} is band-like. As T increases hopping term dominates and μ_{FET} undergoes transition from adiabatic to non-adiabatic state and at very high T the thermal energy can cause dissociation of polarons and the residual electron is scattered causing negative coefficient of $\mu_{FET.}$ The variation of μ_{FET} with T under different coupling regimes is illustrated in **Figure: 1.5**.

A clear indication of band-like transport in semiconducting materials is the observation of Hall Voltage in the FET devices. Ideal, free-electron like Hall signature requires that the electron wave function is delocalized over neighboring molecules. This would then give rise to mesoscopically extended Bloch electrons with a well defined wave-vector which can couple with the external magnetic field to result in hall voltage as shown in **Figure: 1.6**.

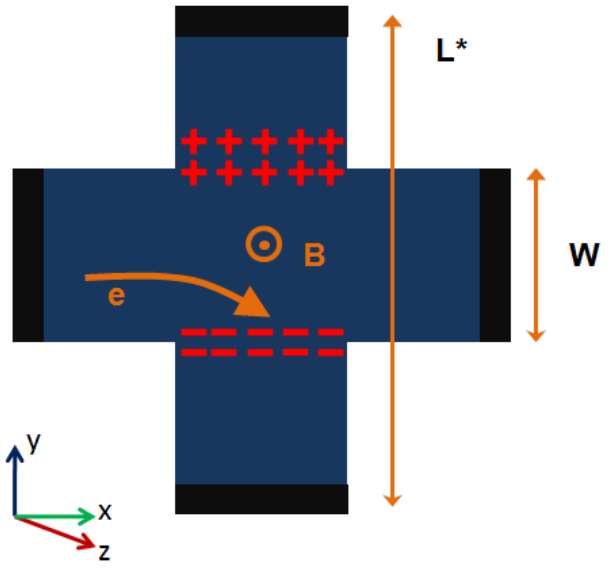


Figure 1.6: *Schematic representation of the Hall measurement setup.*

Hall measurement involves measuring the potential developed across the Hall probes due to the Lorentz force of the **B**. For a current I flowing through a semiconductor and a magnetic field **B** applied perpendicular to the semiconductor following parameters can be estimated from the Hall measurement:

$$R_H = \frac{1}{\boldsymbol{B}}\frac{V_H}{I} \qquad \text{..... (1.9)}$$

$$n_H = \boldsymbol{B}\frac{I}{eV_H} = \frac{1}{eR_H} \qquad \text{…….. (1.10)}$$

$$\mu_H = R_H\sigma_H \qquad \text{…….. (1.11)}$$

Here, R_H is the Hall coefficient, n_H is the number of delocalized carriers contributing to the Hall signal (V_H), σ_H is the four-probe conductivity, L^* is the channel length between the Hall probes and W is the width of the electrodes through which I flows. The sign of the Hall coefficient is the indication of the type of charge carrier involved in the transport.

Hall measurements have been performed on both crystalline as well as amorphous inorganic materials to estimate the number of delocalized charge carriers. For materials with diffusive transport V_H originates from classical Lorentz forces. However, in amorphous materials the origin of V_H is attributed to the quantum interference between different hopping transports which results in small magnitude and anomalous sign of Hall coefficient. Similarly, Hall measurements are also performed on single crystals such as ruberene as well as polycrystalline films of dinaphtho[2,3-b:2,3-f]thieno[3,2-b]thiophene. Despite μ_{FET} magnitudes of 10 $cm^2V^{-1}s^{-1}$, the observation of a clear Hall signal in the case of polymeric semiconductor has been rare. This could be related to the dynamic disorder originating from the polymer microstructure. Hence, a clear understanding of the relation between Hall measurement and the molecular structure will be a useful tool to design high performing polymer semiconductors.

c) Marcus theory

With the development of the new materials and novel device structures, it was possible to achieve transport regime with high charge density for polymer devices. The M-A approach for hopping fails in the regime of high charge density. In these cases, the activation energy originates from the dynamic disorder due to the local polarization fluctuations which are similar to the observed charge transfer phenomenon[23]. Hence, a treatment based on Marcus electron transfer theory is utilized for understanding the hopping processes in these systems. The Marcus expression for semi-classical electron transfer rates is given by:

$$k_{it} = \frac{t^2}{\hbar}\left[\frac{\pi}{k_BT}\right]^{\frac{1}{2}} exp\left[\frac{\left(\lambda_{reorg} + \varepsilon_i - \varepsilon_j\right)^2}{4\lambda_{reorg}k_BT}\right] \qquad \text{…….. (1.12)}$$

where, k_{it} is the charge transfer rate, ε_i and ε_j are the respective energy of the hopping levels, and λ_{reorg} is the reorganization energy. The polarization contribution is included in the transition rate between the initial and final state and the re-organization energy. Both the Marcus theory and M-A predicts zero conductivity at 0 K which is contrary to many experimental observations where a finite conductivity is expected upon extrapolating the $\sigma(T)$ data to 0 K. In order to explain this finite conductivity, the vibrational degrees of freedom is invoked which can drive the tunneling of charge carriers. In such polymeric systems, two regimes of transport exist depending on the carrier potential energy (V_{hop}). In the regime where $eV_{hop} << k_BT$, the transport is T dependent and in the regime where $eV_{hop} >> k_BT$, the transport is superlinear with electric field and is T independent. Such a transition in the transport phenomenon is observed in electrolyte gated devices or ferroelectric FETs, where charge density of 10^{13} cm^{-2} can be attained.

B) Macroscopic Transport models

a) Trap models

Trapping models were initially developed to understand charge transport in amorphous silicon[24]. The charge transport process involves, multiple trapping and de-trapping mechanism through localized defect states as illustrated in **Figure: 1.7**[25]. This type of transport process is referred as the multiple trap release (MTR) transport. The motion of charge carriers through the localized states is attributed to the available thermal energy and is governed by an Arrhenius type dependence given by the expression:

$$\mu = \mu_0 \exp\left(\frac{-E_A}{k_B T}\right) \qquad \text{…….. (1.13)}$$

where μ_0 is the mobility at 0 K and E_A is the activation energy for the charge transport.

As evident from the above expression, at high T the transport is thermally activated and as the T decreases the transport becomes independent of T, which is referred as the apparent band-like transport in organic systems. Such a phenomenon is generally observed in electrolyte based FETs where at low T, μ_{FET} and σ becomes weakly dependent on T[26].

Although the MTR model predicts observation of apparent band-like delocalized transport, the order-disorder transition predicted from this model is not a continuous transition. Hence, a new model for charge transport involving a continuous transition is developed called the mobility edge (ME) model. According to this model, conduction occurs when the charges are excited to the extended transport level referred as E_t. The DOS

is assumed to have an exponential distribution of localized states and the transport occurs with E_A which is given by the difference in energy between the apparent Fermi level of the system (E_F) and the transport level. In the framework of ME model, E_A decreases with the increase in V_g. This can be explained by the fact that as V_g increases, the induced charges increase and E_F shifts close to E_t which results in lower magnitude of E_A for charge transport[27]. Based, on this mechanism a transition from localized trap-limited transport to delocalized extended transport is expected in molecular solids with very low degree of disorder. Typical mobility is then given as:

$$\mu = \mu_0 \exp\left[\frac{-(E_t - E_F)}{k_B T}\right] \qquad \ldots\ldots\ldots\ldots (1.14)$$

This model is extensively used for understanding the temperature dependent charge transport in amorphous silicon based devices and the new generation of high mobility polymer semiconductors.

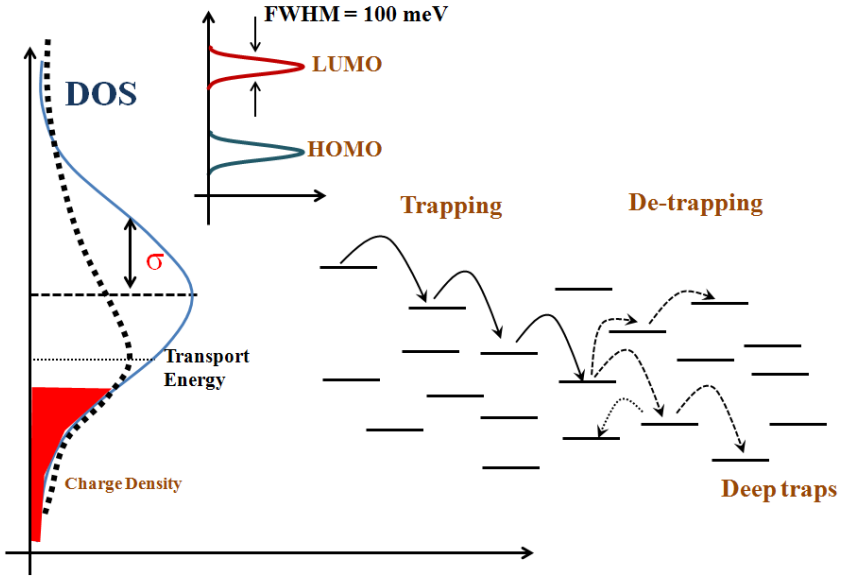


Figure 1.7 : *Schematic of charge transport in the framework of Multiple Trap Release model for transport*

1.2.2 Polymer Field Effect Transistors

Polymer field effect transistors (PFET) are TFTs where the active layer is the polymer semiconductor. The first approach to fabricate FETs using polymers was demonstrated from the Bell Laboratories in the year 2000 with a relatively low performance defined by μ_{FET} of 10^{-5} cm^2 V^{-1} s^{-1} [28]. Starting from these low performing devices, PFETs

have now grown to have μ_{FET} of 10 cm^2 V^{-1} s^{-1} [9d]. These devices now find application in disposable sensors, medico-diagnostic tools and as drivers for flexible displays. In addition to these applications, PFETs have allowed the fundamental studies of charge transport, for example, the degree of wave function delocalization achievable in van der Waals bonded materials[26a], the correlation between charge transport and structural dynamics[14a, 29], studies of transport at two-dimensional charge transfer interfaces[10b, 30] and the role of nuclear tunneling in electron transfer[23a]. Improved understanding of the charge transport and the structure-property correlation in these materials has in-turn led the chemists to develop better semiconducting material which can enhance the device performance[3b].

1.2.3 Operation of PFETs

PFETs differ from the conventional inorganic metal oxide based FETs in the device operation. In contrast to traditional FETs, the operation of PFETs is restricted only to the accumulation regime. The observation of inversion regime in these devices is rare and can be related to the large time constant involved in the transport of minority carriers of the semiconductor[31]. Nevertheless, weak inversion type behavior has been demonstrated in pentacene by extrinsic doping of the molecule with donors like F_6TCNNQ or acceptors like $W_2(hpp)_4$ [32] which is not extendable to other organic materials.

Figure: 1.8 illustrates the accumulation and the depletion mode of operation of a PFET[1]. These operating conditions are similar to inorganic FETs. When $V_g = 0$, no band-bending takes place and is referred as the flat-band condition. As V_g increases ($V_g > 0$ for *n*-type and $V_g < 0$ for *p*-type), band-bending occurs for the semiconductors at the interface which increases the charge density of the majority carriers and hence, the conductivity of the channel increases. In a FET, maximum accumulation of charges occurs at the semiconductor-dielectric interface. Therefore, the effect of bias, on the band structure is limited to the interface and is not present in the bulk of the material. It should be noted that uniform charge distribution is maintained at the channel until V_{ds} is applied[33]. With increase in $|V_{ds}|$, a gradient of charge density from the source to the drain appears along the channel due to position dependent voltage difference between the gate and the different position of the channel. Under these conditions, the channel current (I_{ds}) continues to increase linearly with V_d ($0 < |V_d| < |V_g|$) which is referred to as the linear regime of PFET operation. In general, $V_{ds} > 0$ is applied for n-type transport and $V_{ds} < 0$ is applied for p-type transport. As V_{ds} increases, to a point where $V_{ds} \approx V_g$, the channel depth at the drain reduces to zero due to the absence of effective voltage difference between the gate and the drain[33]. This

magnitude of V_{ds} is known as the pinch-off or saturation voltage. At the pinch-off point the carriers that arrive are injected to the depleted zone around the drain. Hence, the number of charge carriers effectively contributing to the charge transport is essentially invariant with respect to V_{ds} and the current saturates to a constant value. This region is referred as the saturation region.

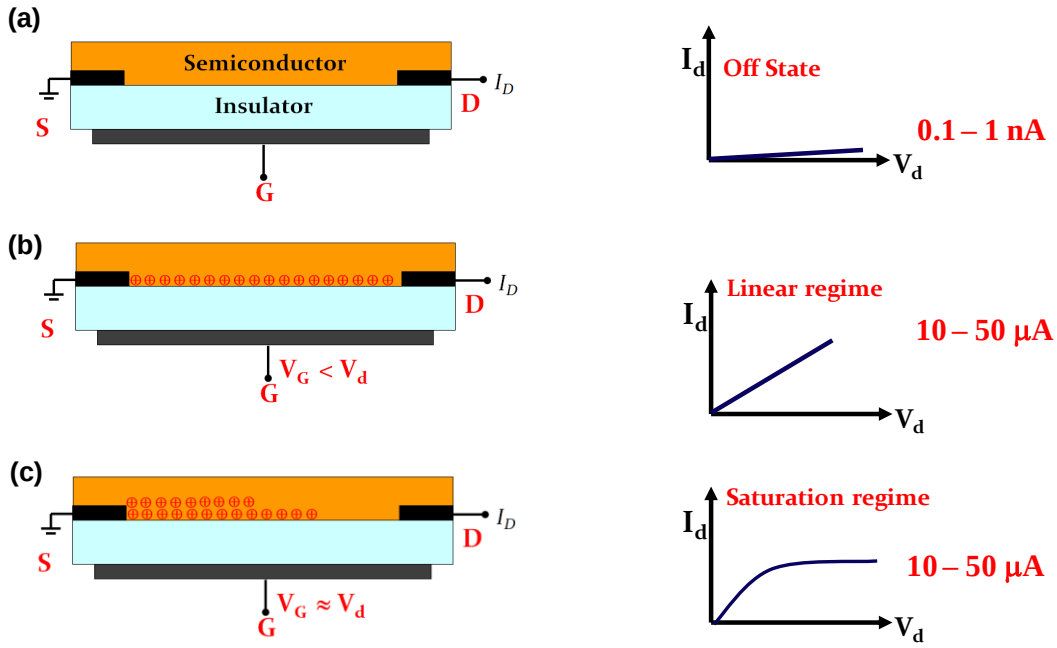


Figure 1.8: *Typical operation of a PFET representing (a) off state; (b) linear regime and (c) saturation regime.*

On reversal of V_g to the other polarity ($V_g < 0$ for n-type and $V_g > 0$ for p-type), the energy bands bend downward at the interface to compensate the corresponding electric field. This causes the charge depletion at the interface, resulting in low conductivity. Under this circumstance, even if the drain-source voltage (V_d) is maintained, the channel current drastically reduces. A quantitative analysis of the PFET performance parameters is arrived at by making the following assumptions which are similar to the treatment used for Si-TFTs: (i) the transverse field directed perpendicular to the channel is larger than the longitudinal field along the channel, (ii) there is no barrier between the energy level of the semiconductor and the Fermi level of the gate electrode, (iii) carrier mobility is constant throughout the channel, and (iv) reverse leakage current is negligibly small[14b]. The first assumption means that the field due to the gate electrode is higher than the drain-source bias or the charges induced by the transverse field are dominant than the longitudinal field[14b, 22]. This eventually requires channel length being much larger compared to the

insulator thickness which is referred as gradual channel approximation. Typical channel length should be about four times the dielectric thickness for observation of proper saturation behavior[34]. The other assumptions are basically to ensure uniform charge transport across the FET channel[14b] and proper operation of the PFET. In addition, due to the presence of interfacial trap states, all the charges induced by the gate dielectric structure are not mobile. This results in an effective V_g given by $V_g - V_{th}$. At a given V_g higher than the threshold voltage V_{th}, the induced mobile charges Q_{mob} per unit area at the source contacts are related to V_g as

$$Q_{mob} = C_i(V_g - V_{th}), \qquad \text{..... (1.15)}$$

where, C_i is the capacitance per unit area of the gate dielectric. If the channel potential is assumed to be zero and the induced charge density varies along the channel, then

$$Q_{mob} = C_i[V_g - V_{th} - V(x)] \qquad \text{..... (1.16)}$$

Neglecting diffusion, I_{ds} induced by carriers is:

$$I_{ds} = W\mu_{FET}Q_{mob}E_x\,, \qquad \text{..... (1.17)}$$

where, W is the channel width, μ_{FET} is the charge mobility and E_x is the electric field at x. Substituting for Q_{mob} and E_x:

$$I_{ds}dx = W\mu_{FET}C_i\big[V_g - V_{th} - V(x)\big]dV \qquad \text{..... (1.18)}$$

The gradual channel expression for the drain current can then be obtained by integration of the current increment from x= 0 to L, that is of the form $V(x)$ = 0 to V_{ds}. Assuming mobility is independent of carrier density the channel current is given as:

$$I_{ds} = WL\mu_{FET}C_i\left[(V_g - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2\right] \qquad \text{..... (1.19)}$$

In the linear regime with $V_{ds} \leq V_g$ this can be simplified to

$$I_{ds} = WL\mu_{FET}^{lin}C_i\big[(V_g - V_{th})V_{ds}\big] \qquad \text{..... (1.20)}$$

From the above expression, it is evident that $I_{ds}(t)$ is directly proportional to V_g, and the μ_{FET}^{lin} can be extracted from the gradient of I_d versus V_g

$$\mu_{FET}^{lin} = \frac{\partial I_{ds}}{\partial V_g}\frac{L}{WC_iV_{ds}} \qquad \text{..... (1.21)}$$

In the pinch off region, when $V_{ds} = V_g - V_{th}$, the current cannot increase substantially anymore and saturates. The saturation current (I_{ds}^{sat}) can be obtained as:

$$I_{ds}^{sat} = \frac{W}{2L}\mu_{FET}^{sat}C_i(V_g - V_{th})^2 \qquad \text{..... (1.22)}$$

and μ_{FET}^{sat} can then be estimated as:

$$\mu_{FET}^{sat} = \frac{\partial I_{ds}}{\partial V_g} \frac{L}{W C_i (V_g - V_{th})} \qquad \text{…….. (1.23)}$$

From the expression, it is evident that μ_{FET}^{sat} is independent of V_g, however in polymer based FETs, mobility is dependent on the gate bias. It should be noted that the expression for I_{ds} gets modified to $I_{ds} = \frac{W}{2L}\mu_{FET}^{sat} C_i (V_g - V_{th} - V_o)^2$ in the presence of an external potential at the interface, which can originate from the charge retention in a ferroelectric dielectric. A detailed derivation of this is given in **Appendix 1**.

Another parameter of importance in the PFET device performance is the ON/OFF ratio. It is defined as the ratio of the channel current in off-state and accumulation mode of the PFET. This ratio is given by:

$$\frac{I_{ds,on}}{I_{ds,off}} = \frac{\mu_{FET}}{\sigma} \frac{C_i^2}{N e d_s^2} V_{ds}^2 \qquad \text{…….. (1.24)}$$

where, N is the charge density induced, σ is the conductivity and d_s is the semiconductor thickness. As evident from the expression, the ON/OFF ratio can be increased by high ratio of mobility and conductivity, higher capacitance dielectric layer and thinner semiconducting layer for the device structure. Moreover, the magnitude of off-current is also determined by the gate leakage current and the existence of bulk conductivity due to un-patterned electrodes.

As evident from the characterization of a PFET charge transport occurs at the semiconductor dielectric interface, charges are injected or collected at the metal-semiconductor interface and the gate-dielectric interface controls the threshold properties of the PFET. Hence, in the pursuit for developing high performance PFETs it is essential to optimize these interfaces as well as develop novel high performance materials by an understanding of the charge transport in polymers. The next sections deal with these facets of PFET operation.

1.3 Device fabrication

A PFET constitute of multiple layers of materials which include: metal electrodes for source, drain and gate; semiconducting layer for charge transport and dielectric layer for inducing charges. These layers form different interfaces namely: metal-semiconductor, semiconductor-dielectric and dielectric-metal. This section discusses the ideal choice of materials for PFET devices and the approach to obtain optimum interface required for high performing devices.

1.3.1 Device Geometry

The solution processable nature of the dielectric and semiconductor requires design and innovation in terms of device geometry to make each of the layers compatible on top of another. Commonly used structures are bottom contact/bottom gate (BC-BG), bottom contact/top gate (BC-TG) and top contact/bottom gate (TC-BG) structures as shown in the **Figure: 1.9**. The latter two geometries are also referred as the staggered geometry. FETs with same components but different geometries show different behavior.

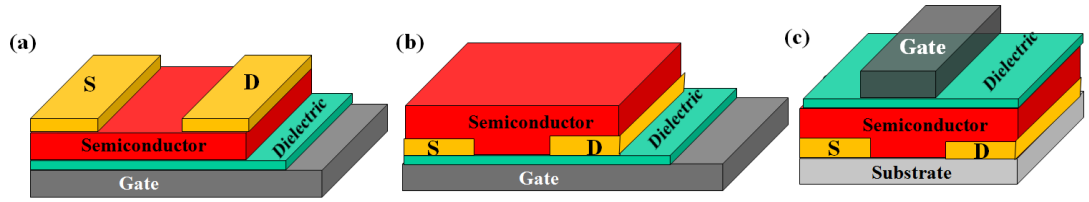


Figure 1.9: *Schematic of different device geometries used for fabricating FETs: (a) top contact bottom gate (TC-BG); (b) bottom contact bottom gate (BC-BG); (c) bottom contact top gate (BC-TG).*

Major reason for the dissimilarity arises due to the way charge transport occurs at the semiconductor-dielectric interface. In BC/BG structure charges are directly injected into the dielectric-semiconductor interface. However, in TC/BG and TG/BC structures, source drain electrodes and the channel are separated by the semiconducting layer. Hence, charge transport in these devices occurs through the un-doped semiconductor before reaching the interface. Also in the staggered configuration the effect of parasitic capacitance and bulk conductivity is comparatively higher than the other geometry. Differences in the transport properties of the transistors fabricated with different geometries also arise from the different morphologies of the semiconductor on the dielectric film. For example, in case of PVDF dielectric based FETs lower μ_{FET} is obtained in the BG structures compared to top gate structures. This can be attributed to the rougher surface of PVDF based dielectric layers. Hence, it is essential to have proper device architecture depending on the materials choice, application required and fabrication procedure to obtain optimum performance.

1.3.2 Source-Drain electrodes

Metallic electrodes in the device structure are generally deposited by vacuum deposition technique (~ 10^{-6} mbar) and typical film thickness is in the range of 40 – 50 nm. The choice of the metal electrodes for source and drain electrodes is dependent on the metal work function (ϕ_m), such that it facilitates efficient electrical injection and transport.

Typical metal electrodes which are used in PFETs are gold (Au, ϕ_m = 5.1 eV), aluminum (Al, ϕ_m = 4.2 eV), magnesium (Mg, ϕ_m = 3.7 eV), calcium (Ca, ϕ_m = 2.8 eV) and silver (Ag, ϕ_m = 4.6 eV). Since most of the *p*-type semiconductors based on thiophene molecules have HOMO level in the range of 5 eV, Au electrodes with ϕ_m ~ 5.1 eV, is the preferred choice of electrode for the drain-source contacts in these materials. In case of *n*-type semiconducting materials, LUMO level is the transport level. The LUMO level of typical *n*-type semiconductors fall in the range of 3.6 – 3.8 eV, hence Al with ϕ_m = 4.2 eV is a preferred choice for source-drain contacts. It is observed that the devices fabricated with Al electrodes are prone to oxide formation which affects the conductivity of the electrodes. This issue is more dominant in bottom-contact top-gated devices. Hence, in some case Au electrodes are also used for *n*-type transport. Apart from these metals, inorganic alloy and water-soluble conducting polymer like poly(3,4-ethylenedioxythiophene)/poly(4-styrenesulfonate) (PEDOT/PSS) are also widely used for PFETs[35].

1.3.3 Metal-Semiconductor Interface

The main purpose of the metal/semiconductor interface is to facilitate efficient carrier injection to the semiconductor. The efficiency of injection of charge carriers depend on the energy barrier prevalent at the metal-semiconductor interface. The origin of this barrier can be related to the difference in the HOMO (LUMO) levels and the Fermi level of the metal electrodes. So in case of holes the barrier for injection (ϕ_{Bh}) is the difference between the ionization potential (E_I) and the work function of the metal, similarly barrier for electron injection (ϕ_{Be}) is the difference between the electron affinity, denoted by χ, and Fermi level of the metal (ϕ_m)[14b]. In addition to this, a finite shift in the energy levels of the semiconductor is observed at the interface due to the metal electrodes reaction with semiconductor[36]. For example, in case of N, N′-diphenyl-1,4,5,8-naphthyl-tetracarboxylimide (DP-NTCDI), the vacuum level in the semiconductor side of the interface with Al shifts upwards by - 0.2 eV, whereas for Au contact it shifts downward by 0.9 eV[37]. As a result, the electron injection barrier is higher for the Al contact than that for the Au contact. An illustration of various barriers and energy levels at the metal-semiconductor interface is given in **Figure: 1.10**.

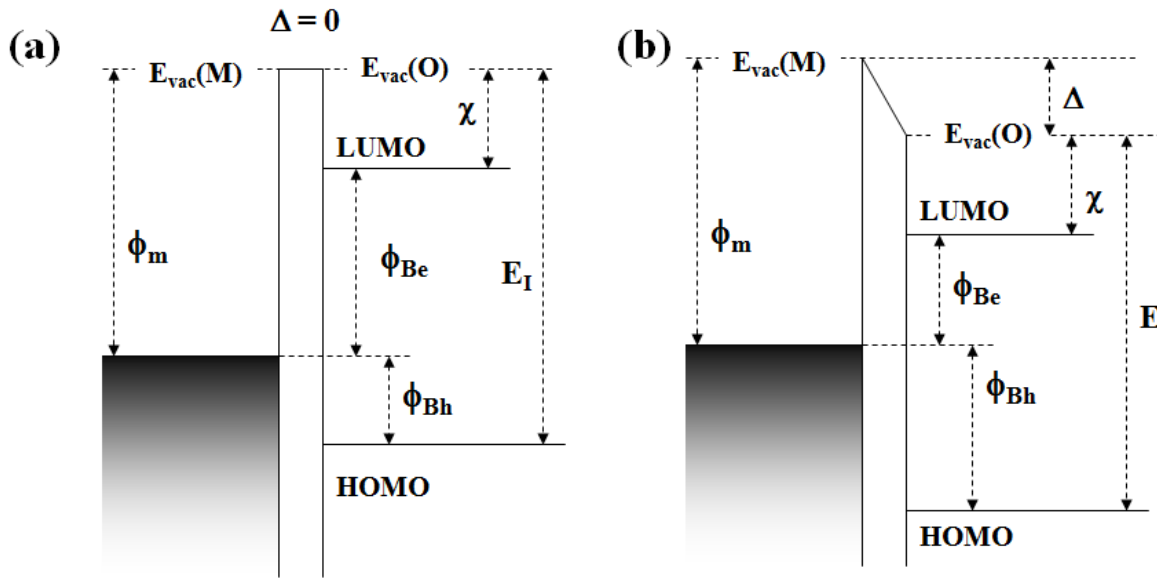


Figure 1.10: *Schematic diagram of the metal-semiconductor interface (a) without and (b) with the interfacial shift. Δ represents the interfacial shift.*

The barriers originating from energy-offset at the interface contribute to the contact resistance for the charge transport. This contact resistance can be estimated by different electrical methods (like transmission line method)[38] and optical methods[39]. Hence, enhancement in the performance of a PFET would involve obtaining low contact resistance for the PFETs. One of the strategies utilized for decreasing contact resistance is deposition of self-assembled thiol molecules on Au electrodes[14b]. These self-assembled layers form optimum contact linking the metal with the thiol end and the semiconductor with the organic end[14b]. Other methods implemented to obtain ohmic contacts include introduction of titanium suboxide[40] interfacial layer which decreases the barrier. In addition, materials like charge transfer salts[41], solution processed carbon nanotubes[42], graphene[43] and metal nano-particles are also explored for usage as source-drain electrodes. It should be noted that the contact resistance is observed to vary with the device geometry of the PFET. In general, top contact geometry results in low contact resistance due to atomic level growth of metal electrode on the semiconducting layer[14b].

1.3.4 Semiconductor Layer

Polymer semiconducting layer in the PFET structure is generally introduced by solution processable techniques like spin coating, drop-casting, dip-coating, printing technology or Langmuir-Blodgett technique. A basic requirement for fabricating

semiconducting layer using these techniques is good solubility of the polymer in common organic solvents. Hence, appropriate design of the polymeric structure is essential to improve the solubility of the polymers. One of the approaches followed to improve the solubility of the polymers is to introduce solubilizing groups like alkyl chains or amphiphillic substitution to the polymer backbone[10a, 44]. Thus the requirement for a good polymer semiconductor is that it should be easily solution processable and form optical quality films. In addition, it would be advantageous to have polymer layers with enhanced crystallinity, interconnected domains and inherent propensity to form π-π stacking which will be reflected in high μ_{FET}.

1.3.5 Dielectric Layer

The purpose of the dielectric layer is to introduce charges at the transport interface by capacitive coupling. Hence, the dielectric layer should be such that it introduces high charge density, has low leakage current (10^{-8} A/mm^2), high breakdown voltage (> 1 MV/cm) and easy downscaling process[45]. Moreover, the fabrication procedure should be such that it does not cause the dissolution or swelling of the subsequent semiconducting layer[45b]. It should be also ensured that the dielectric layer should not hinder the transport, like the presence of hydroxyl group in SiO_2 surface hinders electron transport[46]. A number of materials satisfy these conditions for the choice of dielectric materials. These materials can be broadly classified as inorganic oxides, organic polymer dielectrics and hybrid dielectrics[45a]. Inorganic dielectric mainly constitute metal-oxide layers like HfO_x, CeO_x, Ta_xO_y, ZrO_x etc which are processed by sol-gel method, ALD deposition or vacuum deposition technique[47]. Commonly used polymer dielectric layers include poly-methyl-methacrylate (PMMA), poly-styrene (PS) and benzocyclobutene based BCB which are generally introduced by solution deposition techniques. Details of the dielectric properties are provided in the next chapter. The hybrid dielectrics which consist of both organic and inorganic layers are obtained by a combination of techniques used for organic and inorganic dielectric layers[48].

1.3.6 Semiconductor-Dielectric Interface

Obtaining an optimum interface between the dielectric and the semiconductor is a major challenge. This interface is mainly based on van der Waal interaction between the two layers. It has been observed that the polarity of dielectric layer affects the DOS in the semiconductor[49]. Polar dielectric at the semiconducting interface results in broadening of

the DOS, which hinders the charge transport and it is observed that $\mu_{FET} \propto 1/\varepsilon$, where ε is the dielectric constant of the dielectric layer[13]. It was also observed that this dipolar induced broadening of DOS is related to the nature of the dielectric material and not on the dielectric constant alone[50]. Moreover, the dipolar induced disorder is a columbic interaction which is dependent on the distance between the conjugated core and the dielectric layer[51]. Hence, one of the ways to overcome this limitation is to increase the distance between the polar dielectric layer and the conjugated core of the semiconductor[51-52]. This led to the development of new generation of semiconducting polymers with long-alkyl chains which adopt lamellar structure with edge-on stacking at the dielectric interface. This includes molecules like: Poly(2,5-bis(3-hexadecylthiophen-2-yl)thieno[3,2-b]thiophene): PBTTT[51] and [poly{[*N*,*N*′-bis(2-octyldodecyl)-1,4,5,8-naphthalenedicarboximide-2,6-diyl]-*alt*-5,5′-(2,2′bithiophene): N2200 [52]. Another approach to isolate the conjugated core of the semiconductor from the dielectric layer is by introducing self-assembled interface layers at the interface. In addition, to the isolation of the semiconducting core, these interfacial layer also modify the charge density at the interface due to its electron-donating or accepting properties[53]. A combination of these strategies to obtain optimum transport interface has resulted in obtaining high performing PFETs.

1.3.7 Gate Electrode

Gate electrodes in PFETs are generally obtained by vacuum deposition technique (~ 10^{-6} mbar) with typical metal films of thickness in the range of 40 – 50 nm. The essential pre-requisite for an ideal gate electrode is that it should provide an appropriate surface for the growth of the dielectric layer in the bottom gate geometry. Similarly, in the top gate geometry, the growth of gate electrode should be compatible with the dielectric layer.

1.3.8 Dielectric-metal Interface

This metal-dielectric interface plays a minimal role in PFETs fabricated with polymer dielectrics. Most of the low-*k* polymer dielectric layers are unaffected by the nature of the metal electrode used. However, in the case of high-*k* polymer dielectric layers like PVDF, it is observed that the FE phase of the dielectric is achieved when Au gate electrodes are used[54]. If the FE polymer dielectrics are grown on Al electrode the native oxide layer creates a depolarizing field which opposes the effect of the FE polarization. Similarly, in electrolyte-gated PFETs where the gate electrode participates in an electrochemical reaction with the electrolyte it is possible to tune the V_{th} of the PFETs by

varying the electrodes. It has been observed that low work function metals as gate electrode results in easy switching of the PFET[55]. This trend of tuning V_{th} with different metals is useful to optimize the gain and the operating condition of logic circuits. Hence, proper choice of the gate electrode is essential to obtain desired functionalities from the dielectric layer.

These device fabrication and interface optimization procedures have been the driving force behind the growth of polymer electronics.

1.4 Progress in materials design for PFETs

Major efforts on novel materials design have been towards developing new semiconducting materials and dielectric layers and relatively less towards the development of new materials for electrodes. This section summarizes the various strategies implemented for obtaining novel materials for high performance PFETs.

1.4.1 Electrodes

Typically the electrodes in PFET devices are thermally deposited. Au electrodes are preferred for p-type injection and Al for n-type injection. Photolithography is implemented for Au electrodes to obtain short channel bottom contact device structures. In addition, printed self-aligned electrodes from inkjet printed gold nanoparticles were also obtained by using a block structure to separate electrodes or using a hydrophobic self-assembled monolayer (SAM) such as 1H,1H,2H,2H-perfluorodecanethiol (PFDT). These procedures allow fabrication of devices with channel dimensions of 100 – 400 nm by printing. In addition to these techniques other materials like charge transfer salts[41], solution processed graphene[43],CNT electrodes[42] and conducting polymers like PEDOT:PSS[56] are explored as substitute for metal electrodes.

1.4.2 Dielectric Layer

SiO_2 based dielectric layers are widely employed for traditional PFETs. However, this class of oxide based dielectric layers have limited applicability in *n*-type polymers due to the presence of OH^- group at the surface which results in electron trapping. Hence new generation of polymer dielectric materials like PMMA and BCB were utilized to obtain *n*-channel operation in PFETs[46, 57]. Several other polymer dielectrics were then synthesized and utilized to obtain working PFETs.

In addition, to the organic and inorganic dielectric layers, electrolytes[21a] and ionic liquids[27] are also explored as an alternative for developing PFETs with low operating

voltage. However, these devices suffer from a limitation related to the electrochemical doping, where the ions of the electrolyte dope the semiconductor[26b]. This severely limits the high frequency behavior of the PFETs. Hence, in order to avoid doping of the semiconductors, interlayers are introduced for example: lipid based interlayer. Typical response of a PFET fabricated with P3HT semiconductor and water electrolyte with lipid-bilayer at the interface is shown in **Figure: 1.11** [58]. In addition, new electrolyte molecules based on covalently attached ions have also been synthesized. The covalent attachment of the anions prevents unwanted doping of the semiconductor[59]. These strategies have minimized the electrochemical doping and enhanced the static and dynamic performance of polymer transistors.

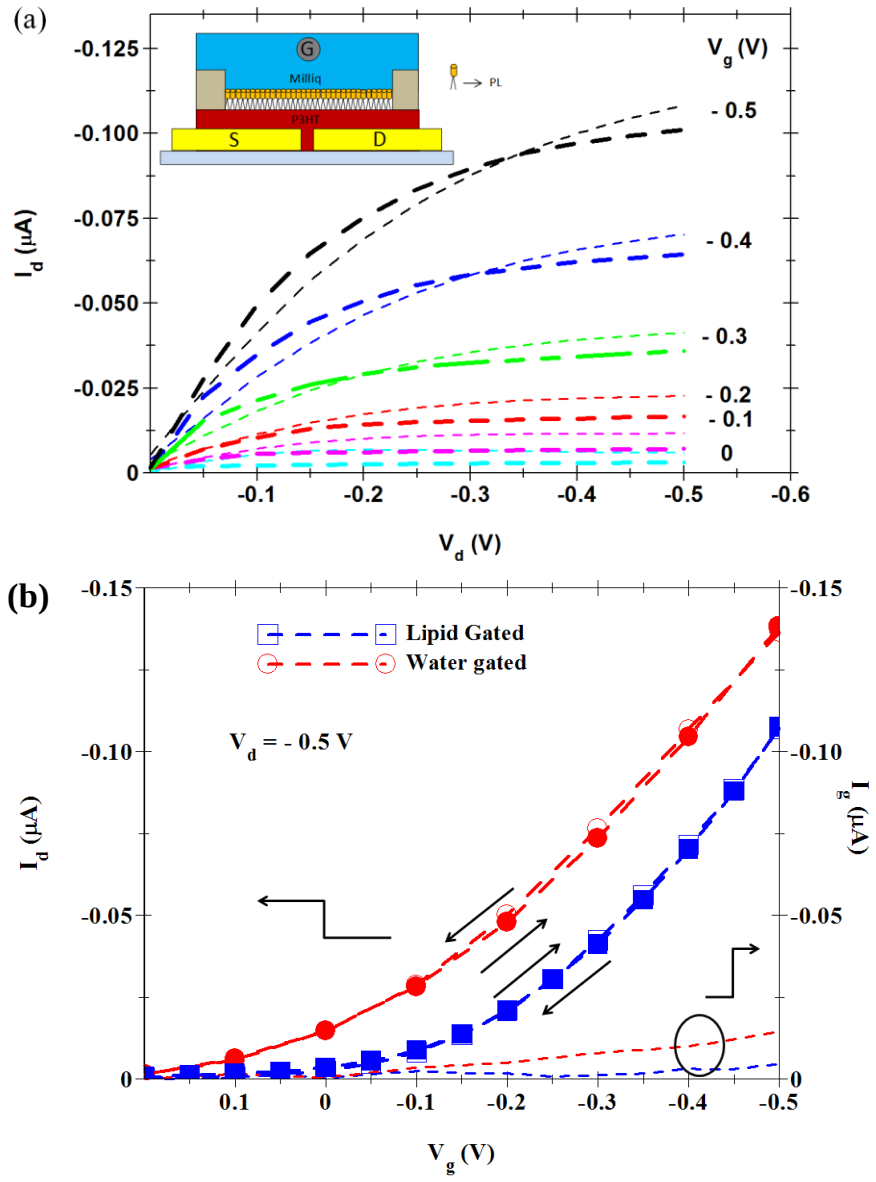


Figure 1.11: *(a) Output and (b) transconductance plots of water gated PFET with and without the phospholipid layer. Reproduced with permission from reference 56.*

Another strategy implemented to obtain high performing dielectric material is the usage of hybrid dielectric layers[60]. These dielectric materials combine the advantages of both organic and inorganic materials. Typically, the hybrid dielectric layers are restricted to bi-layer structures which are fabricated with processes involving T > 400 °C and constitute of a low-k dielectric layer at the interface[47]. These properties limit the control of capacitance, leakage current and compatibility with the solution processable procedure of PFET fabrication[61]. In order to overcome these drawbacks, self assembled dielectric layers based on hydrophilic-hydrophobic interaction and constituting of high polar group have been synthesized[62]. The presence of polar groups in the self-assembled dielectric layer increases the overall capacitance of the assembly, and the novel self-assembly technique is compatible with solution processable and ambient fabrication procedures of PFETs. These developments have resulted in obtaining PFETs with low operating voltage and high frequency response (as shown in chapter 6).

1.4.3 Semiconducting Polymer

Major efforts to improve the performance of PFETs have been on developing new semiconducting polymer materials with enhanced performance parameters[9c]. Basic criteria for the choice of polymeric layer are: good solubility, reasonable degree of long-range order and crystallinity, enhanced π-π stacking, interconnected domains which can support inter-chain hopping and co-planar conjugated core to enhance delocalization[14a, 63].

The most studied polymer in the community are the thiophene based polymers which include poly3-hexylthipohene (P3HT)[10b] and PBTTT [64]. In these molecules, the origin of enhanced performance is ascribed to the inherent structural order induced by head-to-tail chain coupling[10a, 45b]. Moreover, the microstructures of these polymers are dependent on the deposition technique[9b, 65] and the molecular weight of the polymer[66]. It is also observed that higher μ_{FET} is obtained for films when the polymer sample has high molecular weight and when it is deposited with the drop casting technique. However, the best μ_{FET} value achieved for P3HT is limited to 0.1 $cm^2V^{-1}s^{-1}$ [10b] and for PBTTT polymer maximum μ_{FET} of 1 $cm^2V^{-1}s^{-1}$ is achieved[64]. The next step to further improve the performance of PFETs is to design new materials with enhanced crystallinity. In the quest of such materials, polymers such as flourene[67], bithiophene[29] or cyclopenta-thiophene[68] based conjugated cores were explored. Although these molecules have higher crystallinity compared to thiophene based molecules, the μ_{FET} magnitude was limited to 10^{-3} - 10^{-2}

$cm^2V^{-1}s^{-1}$. These classes of polymeric materials also include PCPDTBT based low band gap polymers which were found to be very promising for photovoltaic application. Moreover, the low lying HOMO level of these polymers increases its stability for operation under ambient condition[69]. The best in this class of co-planar polymer is the indacenodithiophene–benzothiadiazole[63] which has a μ_{FET} magnitude of 3.6 $cm^2V^{-1}s^{-1}$. Furthermore, it was demonstrated that shearing these polymers results in macroscopically aligned and inter-connected domains which increases the μ_{FET} to 23 $cm^2V^{-1}s^{-1}$ [9b].

This leads to the next important parameter to be considered for obtaining high performance polymeric materials that is interconnection between the domains[14a]. DPP based polymers are notable for this property. Although these polymers lack long range order, they demonstrate μ_{FET} ~ 10 $cm^2V^{-1}s^{-1}$, which is intriguing[9d]. The high μ_{FET} values obtained from these polymers are attributed to the inter-connected domains which support interchain hopping. This gets reflected in the low degree of disorder and low activation energy for the transport. In addition, several strategies like amphiphillic substitution and inter-digitated alkyl chains are also used to enhance the π-π stacking of the polymer and obtain high degree of transport[9c, 70]. Another method to improve the π-π stacking in the polymer is the usage of donor-acceptor (D-A) type molecules[9d]. The D-A interaction increases the orbital overlap and decreases the distance of π-π stacking. In addition to the enhancement in transport for developing complementary circuits[71].

Consistent efforts have led to large scale improvement in *p*-type polymers, however the observation of electron transport in polymers has lagged behind due to the limited options based on the conjugated cores. In addition, *n*-type polymers have limited stability under ambient conditions[72]. The most promising conjugated core utilized for electron transport is the rylene based naphthalene or perylene core[73]. Naphthalene and perylene conjugated cores have extremely planar structure which supports enhanced charge transport[8, 74]. In addition, the functionalization at the diimide position of the conjugated core, with aliphatic alkyl chain, either branched or long chain, provides good solubility in common organic solvents enhancing their processability[73]. The possibility to obtain interdigitated structures limits the percolation of moisture to the conjugated core, thereby, making it stable for ambient performance. Alkyl substitution also prevents the static disorder the dielectric induces at the conjugated core, as in the case of NDIOD-T2[52] (**Figure: 1.12**).

Based on these strategies, it has been possible to design NDI and PDI based small molecules and oligomers with self-assembling properties and good charge transporting ability[75]. High electron μ_{FET} of up to 0.45–0.85 $cm^2V^{-1}s^{-1}$ has been reported with NDI based bi-thiophene copolymers[52] which increased to 1.8 $cm^2V^{-1}s^{-1}$ for vinylene-thiophene copolymers [76]. In PDI based copolymers, μ_{FET} of up to 0.075 $cm^2V^{-1}s^{-1}$ has been possible with di-thienothiophene unit[77] and with liquid crystalline copolymers[78]. Similarly, Poly(benzimidazobenzophenanthroline) based ladder type polymers are also explored which have limited solution processability in methyl sulfonic acid and exhibit μ_{FET} ~ 0.03 $cm^2V^{-1}s^{-1}$[79]. Thus, the major class of high electron mobility molecules developed includes: ladder type naphthalenediimide[78a, 79], perylene diimide[78a, 80], and D-A type copolymers of NDI, PDI with thiophene, bithiophene dithienothiophene, phenothiazine, dithienopyrrole and phenylene[81] substitution. These developments have significantly enhanced the *n*-type transport in polymers.

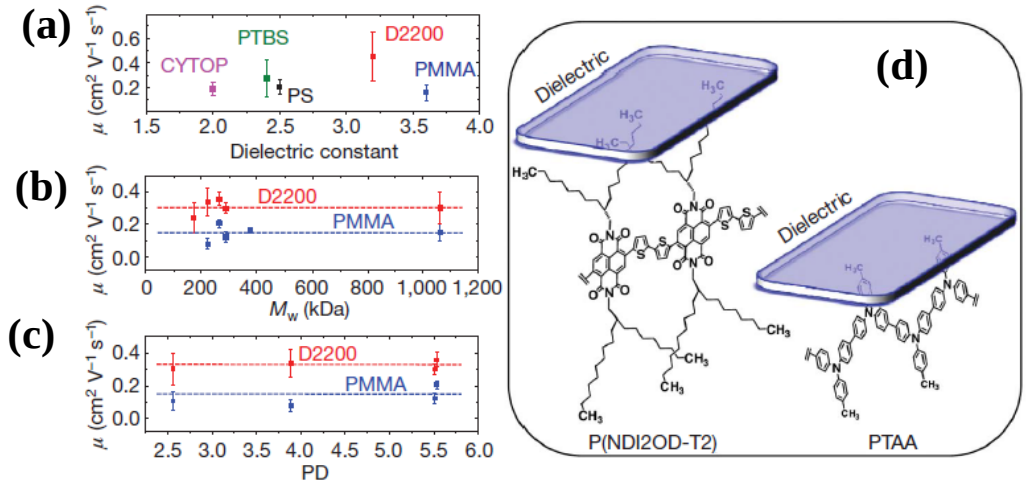


Figure 1.12: *Mobility variation of NDIOD-T2 based PFETs with: (a) different dielectric layers of PFET, (b) molecular weight of the polymer and (c) PDI of the semiconductor. Also shown is the stacking of NDIOD-T2 on the dielectric layer and comparison with the stacking of PTAA polymer.Reproduced with permission from reference 50b.*

These material engineering strategies have resulted in making PFETs with performance comparable to conventional microelectronic devices and opened up the possibility of using them devices for practical applications.

1.5 Outlook and Thesis Outline

PFET devices have demonstrated considerable performance enhancement. These high values are unexpected for disorder prone conjugated polymer systems. The applicability of traditional transport physics would then be questionable. Hence a set of systematic and comprehensive studies are needed to understand the complex microstructure, structure–property relationships and the origin of the μ_{FET}. It is desirable that disorder does not dominate the transport parameters and the electrical transport is controlled by the intrinsic aspects of the material. This should then open up the field to design novel materials and observe various fascinating phenomenon that have hitherto not been accessible in these systems.

This thesis is a step towards the direction of understanding the transport physics of high mobility polymers and developing novel strategies for device fabrication to obtain performance comparable to amorphous silicon. Studies were carried out to understand the molecular origin of high μ_{FET} in one such amphiphillic DPP (2DPP-TEG) based polymeric material. Transport studies performed on PFETs fabricated with 2DPP-TEG molecule and low-*k* dielectric material indicates a negative coefficient of μ_{FET}. In addition, the observed equivalence of μ_{Hall} and μ_{FET} points to delocalized charge carriers indicating a clear band-like transport mechanism in this polymer. These studies lead us to the general guideline for band-like transport in polymers which involve : amphiphillic design of the polymer resulting in microscopic structures with interconnected aggregates, co-planar conjugated core with low re-organization energy and optimum interface for charge transport.

Chapter four deals with the origin of disorder in high-*k* dielectric based PFETs. Presence of high-*k* dielectric material in the PFET device structure is expected to induce broadening of the density of states of the semiconductor. However, it is not clear whether the disorder at the interface is related to the dielectric constant (*k*) or the nature of dielectric material. A comprehensive study relating a number of dielectric and semiconducting materials points to the fact that the electrostatic disorder at the transport interface of a PFET is related to the nature of dielectric material and not the dielectric constant. After the optimization of the static response of the PFET, the next study in chapter five focuses on the dynamic performance of the PFETs. A combination of dipole and device engineering procedure is utilized to obtain PFETs with switching speeds three orders of magnitude higher than the conventional PFETs. Furthermore, all-polymer logic circuits are fabricated

with switching frequency of 4 MHz for printable channel length. A detailed investigation is then performed using different dielectric and semiconducting materials to obtain the limiting factors for the switching in PFETs. The general requirement for fast switching polymer circuits are: ordered dipoles of the dielectric, semiconductors with high μ_{FET} and isolated conjugated core.

In chapter six, issues related to the high operating voltage of PFETs are addressed. Hybrid self-assembled nano-dielectrics are utilized as the dielectric layer to fabricate PFETs. These multilayered self-assembled nano-dielectric (SAND) structures have leakage properties of 0.1 pA, capacitance of 0.4 – 0.8 μF/cm^2 and breakdown voltage of 10^9 V/m. PFETs fabricated with these dielectric layer operate at 1 V with typical μ_{FET} ~ 2.4 cm^{2}V^{-1}s^{-1} and a switching frequency of ~ 5 MHz. The origin of the high performance in these low operating voltage PFETs can be attributed to the combination of optimum transport interface, densely packed ordered dipoles and effective combination of atomic, molecular and ionic polarization. The SAND structure provides a functional interface to modulate the polarization by optical and electrical control. This functionality of the interface is then utilized to design optoelectronic memory with digitally commutable electrical and optical response.

In summary, this thesis reports a combination of strategies to obtain PFETs with performance comparable to *a*-Si based FETs which would pave the way for utilizing printable polymer devices for real applications. The performance parameters of the PFETs as it stands now are μ_{FET} ~ 3 cm^{2}V^{-1}s^{-1}, switching time of 150 ns, operating voltage ~ 1 V, power dissipation of ~ 1 – 10 nW. All these parameters are considerably higher than the commercially available *a*-Si based TFTs.

References

1. Sze, S. M., Physics of Semiconductor devices.
2. Weimer, P. K., Proc. of IRE. *50* (1462).
3. (a) Sirringhaus, H., 25th Anniversary Article: Organic Field-Effect Transistors: The Path Beyond Amorphous Silicon. *Advanced Materials* **2014,** *26* (9), 1319-1335; (b) Allard, S.; Forster, M.; Souharce, B.; Thiem, H.; Scherf, U., Organic Semiconductors for Solution-Processable Field-Effect Transistors (OFETs). *Angew. Chem.* **2008,** *47* (22), 4070-4098.
4. (a) Gustafsson, G.; Cao, Y.; Treacy, G. M.; Klavetter, F.; Colaneri, N.; Heeger, A. J., Flexible light-emitting diodes made from soluble conducting polymers. *Nature* **1992,**

357 (6378), 477-479; (b) Patil, A. O.; Heeger, A. J.; Wudl, F., Optical properties of conducting polymers. *Chemical Reviews* **1988,** *88* (1), 183-200.

5. Burroughes, J. H.; Bradley, D. D. C.; Brown, A. R.; Marks, R. N.; Mackay, K.; Friend, R. H.; Burns, P. L.; Holmes, A. B., Light-emitting diodes based on conjugated polymers. *Nature* **1990,** *347* (6293), 539-541.

6. Sariciftci, N. S.; Smilowitz, L.; Heeger, A. J.; Wudl, F., Photoinduced Electron Transfer from a Conducting Polymer to Buckminsterfullerene. *Science* **1992,** *258* (5087), 1474-1476.

7. Sirringhaus, H.; Kawase, T.; Friend, R. H.; Shimoda, T.; Inbasekaran, M.; Wu, W.; Woo, E. P., High-Resolution Inkjet Printing of All-Polymer Transistor Circuits. *Science* **2000,** *290* (5499), 2123-2126.

8. Chen, Z.; Zheng, Y.; Yan, H.; Facchetti, A., Naphthalenedicarboximide- vs Perylenedicarboximide-Based Copolymers. Synthesis and Semiconducting Properties in Bottom-Gate N-Channel Organic Transistors. *Journal of the American Chemical Society* **2008,** *131* (1), 8-9.

9. (a) Senanayak, S. P.; Narayan, K. S., Strategies for Fast-Switching in All-Polymer Field Effect Transistors. *Advanced Functional Materials* **2014,** *24* (22), 3324-3331; (b) Tseng, H.-R.; Phan, H.; Luo, C.; Wang, M.; Perez, L. A.; Patel, S. N.; Ying, L.; Kramer, E. J.; Nguyen, T.-Q.; Bazan, G. C.; Heeger, A. J., High-Mobility Field-Effect Transistors Fabricated with Macroscopic Aligned Semiconducting Polymers. *Advanced Materials* **2014,** *26* (19), 2993-2998; (c) Li, Y.; Sonar, P.; Murphy, L.; Hong, W., High mobility diketopyrrolopyrrole (DPP)-based organic semiconductor materials for organic thin film transistors and photovoltaics. *Energy & Environmental Science* **2013,** *6* (6), 1684-1710; (d) Li, J.; Zhao, Y.; Tan, H. S.; Guo, Y.; Di, C.-A.; Yu, G.; Liu, Y.; Lin, M.; Lim, S. H.; Zhou, Y.; Su, H.; Ong, B. S., A stable solution-processed polymer semiconductor with record high-mobility for printed transistors. *Sci. Rep.* **2012,** *2*.

10. (a) Facchetti, A., Organic semiconductors: Made to order. *Nat Mater* **2013,** *12* (7), 598-600; (b) Sirringhaus, H.; Brown, P. J.; Friend, R. H.; Nielsen, M. M.; Bechgaard, K.; Langeveld-Voss, B. M. W.; Spiering, A. J. H.; Janssen, R. A. J.; Meijer, E. W.; Herwig, P.; de Leeuw, D. M., Two-dimensional charge transport in self-organized, high-mobility conjugated polymers. *Nature* **1999,** *401* (6754), 685-688.

11. (a) Peierls, R., Quantum Theory of Solids; (b) Kivelson, S.; Heim, D. E., Hubbard versus Peierls and the Su-Schrieffer-Heeger model of polyacetylene. *Physical Review B* **1982,** *26* (8), 4278-4292.

12. Austin, I. G.; Mott, N. F., Polarons in crystalline and non-crystalline materials. *Advances in Physics* **2001,** *50* (7), 757 - 812.

13. Hulea, I. N.; Fratini, S.; Xie, H.; Mulder, C. L.; Iossad, N. N.; Rastelli, G.; Ciuchi, S.; Morpurgo, A. F., Tunable Frohlich polarons in organic single-crystal transistors. *Nat Mater* **2006,** *5* (12), 982-986.

14. (a) Noriega, R.; Rivnay, J.; Vandewal, K.; Koch, F. P. V.; Stingelin, N.; Smith, P.; Toney, M. F.; Salleo, A., A general relationship between disorder, aggregation and charge transport in conjugated polymers. *Nat Mater* **2013,** *12* (11), 1038-1044; (b) Horowitz, G., Organic Field-Effect Transistors. *Adv. Mater.* **1998,** *10* (5), 365-377; (c) Troisi, A., Charge transport in high mobility molecular semiconductors: classical models and new theories. *Chemical Society Reviews* **2011,** *40* (5), 2347-2358.

15. Tessler, N.; Preezant, Y.; Rappaport, N.; Roichman, Y., Charge Transport in Disordered Organic Materials and Its Relevance to Thin-Film Devices: A Tutorial Review. *Advanced Materials* **2009,** *21* (27), 2741-2761.

16. Bredas, J. L.; Street, G. B., Polarons, bipolarons, and solitons in conducting polymers. *Accounts of Chemical Research* **1985,** *18* (10), 309-315.

17. Capone, M.; Stephan, W.; Grilli, M., Small-polaron formation and optical absorption in Su-Schrieffer-Heeger and Holstein models. *Physical Review B* **1997,** *56* (8), 4484-4493.

18. Miller, A.; Abrahams, E., Impurity Conduction at Low Concentrations. *Physical Review* **1960,** *120* (3), 745-755.

19. Yuen, J. D.; Menon, R.; Coates, N. E.; Namdas, E. B.; Cho, S.; Hannahs, S. T.; Moses, D.; Heeger, A. J., Nonlinear transport in semiconducting polymers at high carrier densities. *Nat Mater* **2009,** *8* (7), 572-575.

20. Davis, N. F. M. a. E. A., Electronic Processes in Non-Crystalline Materials. *2nd Edition*.

21. (a) Dhoot, A. S.; Wang, G. M.; Moses, D.; Heeger, A. J., Voltage-Induced Metal-Insulator Transition in Polythiophene Field-Effect Transistors. *Phys. Rev. Lett.* **2006,** *96* (24), 246403; (b) Pérez-Garrido, A.; Ortuño, M.; Cuevas, E.; Ruiz, J.; Pollak, M., Conductivity of the two-dimensional Coulomb glass. *Physical Review B* **1997,** *55* (14), R8630.

22. Klauk, H., Organic thin-film transistors. *Chem. Soc. Rev.* **2010,** *39* (7), 2643-2666.

23. (a) Asadi, K.; Kronemeijer, A. J.; Cramer, T.; Jan Anton Koster, L.; Blom, P. W. M.; de Leeuw, D. M., Polaron hopping mediated by nuclear tunnelling in semiconducting polymers at high carrier density. *Nat Commun* **2013,** *4*, 1710; (b) Coropceanu, V.; Cornil, J.; da Silva Filho, D. A.; Olivier, Y.; Silbey, R.; Brédas, J.-L., Charge Transport in Organic Semiconductors. *Chemical Reviews* **2007,** *107* (4), 926-952.

24. Le Comber, P. G.; Spear, W. E., Electronic Transport in Amorphous Silicon Films. *Physical Review Letters* **1970,** *25* (8), 509-511.

25. Letizia, J. A.; Rivnay, J.; Facchetti, A.; Ratner, M. A.; Marks, T. J., Variable Temperature Mobility Analysis of n-Channel, p-Channel, and Ambipolar Organic Field-Effect Transistors. *Advanced Functional Materials* **2010,** *20* (1), 50-58.

26. (a) Dhoot, A. S.; Yuen, J. D.; Heeney, M.; McCulloch, I.; Moses, D.; Heeger, A. J., Beyond the metal-insulator transition in polymer electrolyte gated polymer field-effect

transistors. *Proceedings of the National Academy of Sciences* **2006,** *103* (32), 11834-11837; (b) Panzer, M. J.; Frisbie, C. D., High Carrier Density and Metallic Conductivity in Poly(3-hexylthiophene) Achieved by Electrostatic Charge Injection. *Advanced Functional Materials* **2006,** *16* (8), 1051-1056.

27. Xia, Y.; Cho, J. H.; Lee, J.; Ruden, P. P.; Frisbie, C. D., Comparison of the Mobility–Carrier Density Relation in Polymer and Single-Crystal Organic Transistors Employing Vacuum and Liquid Gate Dielectrics. *Advanced Materials* **2009,** *21* (21), 2174-2179.

28. Barbe, D. F.; Westgate, C. R., Surface state parameters of metal-free phthalocyanine single crystals. *Journal of Physics and Chemistry of Solids* **1970,** *31* (12), 2679-2687.

29. Guo, X.; Ortiz, R. P.; Zheng, Y.; Hu, Y.; Noh, Y.-Y.; Baeg, K.-J.; Facchetti, A.; Marks, T. J., Bithiophene-Imide-Based Polymeric Semiconductors for Field-Effect Transistors: Synthesis, Structure−Property Correlations, Charge Carrier Polarity, and Device Stability. *Journal of the American Chemical Society* **2011,** *133* (5), 1405-1418.

30. Alves, H.; Molinari, A. S.; Xie, H.; Morpurgo, A. F., Metallic conduction at organic charge-transfer interfaces. *Nat Mater* **2008,** *7* (7), 574-580.

31. (a) Lindner, T.; Paasch, G., Inversion layer formation in organic field-effect devices. *Journal of Applied Physics* **2007,** *102* (5), -; (b) Brondijk, J. J.; Spijkman, M.; van Seijen, F.; Blom, P. W. M.; de Leeuw, D. M., Formation of inversion layers in organic field-effect transistors. *Physical Review B* **2012,** *85* (16), 165310.

32. Lüssem, B.; Tietze, M. L.; Kleemann, H.; Hoßbach, C.; Bartha, J. W.; Zakhidov, A.; Leo, K., Doped organic transistors operating in the inversion and depletion regime. *Nat Commun* **2013,** *4*.

33. Zaumseil, J.; Sirringhaus, H., Electron and Ambipolar Transport in Organic Field-Effect Transistors. *Chemical Reviews* **2007,** *107* (4), 1296-1323.

34. Noh, Y.-Y.; Zhao, N.; Caironi, M.; Sirringhaus, H., Downscaling of self-aligned, all-printed polymer thin-film transistors. *Nat Nano* **2007,** *2* (12), 784-789.

35. Sirringhaus, H.; Tessler, N.; Friend, R. H., Integrated Optoelectronic Devices Based on Conjugated Polymers. *Science* **1998,** *280* (5370), 1741-1744.

36. (a) Hill, I. G.; Rajagopal, A.; Kahn, A.; Hu, Y., Molecular level alignment at organic semiconductor-metal interfaces. *Applied Physics Letters* **1998,** *73* (5), 662-664; (b) Hung, L. S.; Tang, C. W., Interface engineering in preparation of organic surface-emitting diodes. *Applied Physics Letters* **1999,** *74* (21), 3209-3211.

37. Ishii, H.; Seki, K., Energy level alignment at organic/metal interfaces studied by UV photoemission: breakdown of traditional assumption of a common vacuum level at the interface. *Electron Devices, IEEE Transactions on* **1997,** *44* (8), 1295-1301.

38. Baeg, K.-J.; Khim, D.; Jung, S.-W.; Kang, M.; You, I.-K.; Kim, D.-Y.; Facchetti, A.; Noh, Y.-Y., Remarkable Enhancement of Hole Transport in Top-Gated N-Type

Polymer Field-Effect Transistors by a High-k Dielectric for Ambipolar Electronic Circuits. *Advanced Materials* **2012,** *24* (40), 5433-5439.

39. Rao, M.; Narayan, K. S., Evaluation of electrode-semiconductor barrier in transparent top-contact polymer field effect transistors. *Applied Physics Letters* **2008,** *92* (22), -.

40. Cho, S.; Seo, J. H.; Lee, K.; Heeger, A. J., Enhanced Performance of Fullerene n-Channel Field-Effect Transistors with Titanium Sub-Oxide Injection Layer. *Advanced Functional Materials* **2009,** *19* (9), 1459-1464.

41. Wada, H.; Shibata, K.; Bando, Y.; Mori, T., Contact resistance and electrode material dependence of air-stable n-channel organic field-effect transistors using dimethyldicyanoquinonediimine (DMDCNQI). *Journal of Materials Chemistry* **2008,** *18* (35), 4165-4171.

42. Wada, H.; Mori, T., Solution-processed carbon electrodes for organic field-effect transistors. *Applied Physics Letters* **2008,** *93* (21), -.

43. Di, C.-a.; Wei, D.; Yu, G.; Liu, Y.; Guo, Y.; Zhu, D., Patterned Graphene as Source/Drain Electrodes for Bottom-Contact Organic Field-Effect Transistors. *Advanced Materials* **2008,** *20* (17), 3289-3293.

44. Guo, X.; Quinn, J.; Chen, Z.; Usta, H.; Zheng, Y.; Xia, Y.; Hennek, J. W.; Ortiz, R. P.; Marks, T. J.; Facchetti, A., Dialkoxybithiazole: A New Building Block for Head-to-Head Polymer Semiconductors. *Journal of the American Chemical Society* **2013,** *135* (5), 1986-1996.

45. (a) Facchetti, A.; Yoon, M. H.; Marks, T. J., Gate Dielectrics for Organic Field-Effect Transistors: New Opportunities for Organic Electronics. *Advanced Materials* **2005,** *17* (14), 1705-1725; (b) Sirringhaus, H.; Bird, M.; Zhao, N., Charge Transport Physics of Conjugated Polymer Field-Effect Transistors. *Adv. Mater.* **2010,** *22* (34), 3893-3898.

46. Chua, L.-L.; Zaumseil, J.; Chang, J.-F.; Ou, E. C. W.; Ho, P. K. H.; Sirringhaus, H.; Friend, R. H., General observation of n-type field-effect behaviour in organic semiconductors. *Nature* **2005,** *434* (7030), 194-199.

47. Ortiz, R. P.; Facchetti, A.; Marks, T. J., High-k Organic, Inorganic, and Hybrid Dielectrics for Low-Voltage Organic Field-Effect Transistors. *Chemical Reviews* **2009,** *110* (1), 205-239.

48. Yoon, M.-H.; Facchetti, A.; Marks, T. J., σ-π molecular dielectric multilayers for low-voltage organic thin-film transistors. *Proc. Natl. Acad. Sci. USA* **2005,** *102* (13), 4678-4682.

49. Veres, J.; Ogier, S. D.; Leeming, S. W.; Cupertino, D. C.; Mohialdin Khaffaf, S., Low-k Insulators as the Choice of Dielectrics in Organic Field-Effect Transistors. *Adv. Funct. Mater.* **2003,** *13* (3), 199-204.

50. Senanayak, S. P.; Guha, S.; Narayan, K. S., Polarization fluctuation dominated electrical transport processes of polymer-based ferroelectric field effect transistors. *Phys. Rev. B* **2012,** *85* (11), 115311.

51. Zhao, N.; Noh, Y. Y.; Chang, J. F.; Heeney, M.; McCulloch, I.; Sirringhaus, H., Polaron Localization at Interfaces in High-Mobility Microcrystalline Conjugated Polymers. *Adv. Mater.* **2009,** *21* (37), 3759-3763.

52. Yan, H.; Chen, Z.; Zheng, Y.; Newman, C.; Quinn, J. R.; Dotz, F.; Kastler, M.; Facchetti, A., A high-mobility electron-transporting polymer for printed transistors. *Nature* **2009,** *457* (7230), 679-686.

53. Kobayashi, S.; Nishikawa, T.; Takenobu, T.; Mori, S.; Shimoda, T.; Mitani, T.; Shimotani, H.; Yoshimoto, N.; Ogawa, S.; Iwasa, Y., Control of carrier density by self-assembled monolayers in organic field-effect transistors. *Nat Mater* **2004,** *3* (5), 317-322.

54. Kang, S. J.; Park, Y. J.; Sung, J.; Jo, P. S.; Park, C.; Kim, K. J.; Cho, B. O., Spin cast ferroelectric beta poly(vinylidene fluoride) thin films via rapid thermal annealing. *Appl. Phys. Lett.* **2008,** *92* (1), 012921.

55. Kergoat, L.; Herlogsson, L.; Piro, B.; Pham, M. C.; Horowitz, G.; Crispin, X.; Berggren, M., Tuning the threshold voltage in electrolyte-gated organic field-effect transistors. *Proceedings of the National Academy of Sciences* **2012,** *109* (22), 8394-8399.

56. (a) Bubnova, O.; Khan, Z. U.; Wang, H.; Braun, S.; Evans, D. R.; Fabretto, M.; Hojati-Talemi, P.; Dagnelund, D.; Arlin, J.-B.; Geerts, Y. H.; Desbief, S.; Breiby, D. W.; Andreasen, J. W.; Lazzaroni, R.; Chen, W. M.; Zozoulenko, I.; Fahlman, M.; Murphy, P. J.; Berggren, M.; Crispin, X., Semi-metallic polymers. *Nat Mater* **2014,** *13* (2), 190-194; (b) Alemu, D.; Wei, H.-Y.; Ho, K.-C.; Chu, C.-W., Highly conductive PEDOT:PSS electrode by simple film treatment with methanol for ITO-free polymer solar cells. *Energy & Environmental Science* **2012,** *5* (11), 9662-9671.

57. Wen, Y.; Liu, Y., Recent Progress in n-Channel Organic Thin-Film Transistors. *Advanced Materials* **2010,** *22* (12), 1331-1345.

58. Narayan, K. S.; Madhushankar, B. N.; Gautam, V.; Senanayak, S. P.; Shivanna, R., Water-Gated Phospholipid-Monolayer Organic Field Effect Transistor Through Modified Mueller–Montal Method. *Electron Device Letters, IEEE* **2013,** *34* (2), 310-312.

59. Herlogsson, L.; Noh, Y.-Y.; Zhao, N.; Crispin, X.; Sirringhaus, H.; Berggren, M., Downscaling of Organic Field-Effect Transistors with a Polyelectrolyte Gate Insulator. *Advanced Materials* **2008,** *20* (24), 4708-4713.

60. Klauk, H.; Zschieschang, U.; Pflaum, J.; Halik, M., Ultralow-power organic complementary circuits. *Nature* **2007,** *445* (7129), 745-748.

61. DiBenedetto, S. A.; Facchetti, A.; Ratner, M. A.; Marks, T. J., Molecular Self-Assembled Monolayers and Multilayers for Organic and Unconventional Inorganic Thin-Film Transistor Applications. *Advanced Materials* **2009,** *21* (14-15), 1407-1433.

62. Everaerts, K.; Emery, J. D.; Jariwala, D.; Karmel, H. J.; Sangwan, V. K.; Prabhumirashi, P. L.; Geier, M. L.; McMorrow, J. J.; Bedzyk, M. J.; Facchetti, A.; Hersam, M. C.; Marks, T. J., Ambient-Processable High Capacitance Hafnia-Organic Self-Assembled Nanodielectrics. *Journal of the American Chemical Society* **2013,** *135* (24), 8926-8939.

63. Zhang, X.; Bronstein, H.; Kronemeijer, A. J.; Smith, J.; Kim, Y.; Kline, R. J.; Richter, L. J.; Anthopoulos, T. D.; Sirringhaus, H.; Song, K.; Heeney, M.; Zhang, W.; McCulloch, I.; DeLongchamp, D. M., Molecular origin of high field-effect mobility in an indacenodithiophene–benzothiadiazole copolymer. *Nat Commun* **2013,** *4*.

64. Hamadani, B. H.; Gundlach, D. J.; McCulloch, I.; Heeney, M., *Undoped polythiophene field-effect transistors with mobility of 1 $cm^2V^{-1}s^{-1}$*. AIP: 2007; Vol. 91, p 243512.

65. Giri, G.; Park, S.; Vosgueritchian, M.; Shulaker, M. M.; Bao, Z., High-Mobility, Aligned Crystalline Domains of TIPS-Pentacene with Metastable Polymorphs Through Lateral Confinement of Crystal Growth. *Advanced Materials* **2014,** *26* (3), 487-493.

66. (a) Singh, K. A.; Sauvé, G.; Zhang, R.; Kowalewski, T.; McCullough, R. D.; Porter, L. M., Dependence of field-effect mobility and contact resistance on nanostructure in regioregular poly(3-hexylthiophene) thin film transistors. *Applied Physics Letters* **2008,** *92* (26), -; (b) Joshi, S.; Pingel, P.; Grigorian, S.; Panzner, T.; Pietsch, U.; Neher, D.; Forster, M.; Scherf, U., Bimodal Temperature Behavior of Structure and Mobility in High Molecular Weight P3HT Thin Films. *Macromolecules* **2009,** *42* (13), 4651-4660.

67. Yan, F.; Hong, Y.; Migliorato, P., Temperature dependent characteristics of all polymer thin-film transistors based on poly(9,9-dioctylfluorene-co-bithiophene). *Journal of Applied Physics* **2007,** *101* (6), -.

68. (a) Bedi, A.; Senanayak, S. P.; Das, S.; Narayan, K. S.; Zade, S. S., Cyclopenta[c]thiophene oligomers based solution processable D-A copolymers and their application as FET materials. *Polymer Chemistry* **2012,** *3* (6), 1453-1460; (b) Das, S.; Senanayak, S. P.; Bedi, A.; Narayan, K. S.; Zade, S. S., Synthesis and charge carrier mobility of a solution-processable conjugated copolymer based on cyclopenta[c]thiophene. *Polymer* **2011,** *52* (25), 5780-5787.

69. (a) Chen, C.-H.; Hsieh, C.-H.; Dubosc, M.; Cheng, Y.-J.; Hsu, C.-S., Synthesis and Characterization of Bridged Bithiophene-Based Conjugated Polymers for Photovoltaic Applications: Acceptor Strength and Ternary Blends. *Macromolecules* **2009,** *43* (2), 697-708; (b) Cho, S.; Seo, J. H.; Park, S. H.; Beaupré, S.; Leclerc, M.; Heeger, A. J., A Thermally Stable Semiconducting Polymer. *Advanced Materials* **2010,** *22* (11), 1253-1257.

70. (a) Kanimozhi, C.; Yaacobi-Gross, N.; Chou, K. W.; Amassian, A.; Anthopoulos, T. D.; Patil, S., Diketopyrrolopyrrole–Diketopyrrolopyrrole-Based Conjugated Copolymer for High-Mobility Organic Field-Effect Transistors. *J. Am. Chem. Soc.* **2012,** *134* (40), 16532-16535; (b) Narayan, B.; Senanayak, S. P.; Jain, A.; Narayan, K. S.; George, S. J., Self-

Assembly of π-Conjugated Amphiphiles: Free Standing, Ordered Sheets with Enhanced Mobility. *Advanced Functional Materials* **2013,** *23* (24), 3053-3060; (c) Zhang, X.; Richter, L. J.; DeLongchamp, D. M.; Kline, R. J.; Hammond, M. R.; McCulloch, I.; Heeney, M.; Ashraf, R. S.; Smith, J. N.; Anthopoulos, T. D.; Schroeder, B.; Geerts, Y. H.; Fischer, D. A.; Toney, M. F., Molecular Packing of High-Mobility Diketo Pyrrolo-Pyrrole Polymer Semiconductors with Branched Alkyl Side Chains. *Journal of the American Chemical Society* **2011,** *133* (38), 15073-15084.

71. Sonar, P.; Singh, S. P.; Li, Y.; Soh, M. S.; Dodabalapur, A., A Low-Bandgap Diketopyrrolopyrrole-Benzothiadiazole-Based Copolymer for High-Mobility Ambipolar Organic Thin-Film Transistors. *Advanced Materials* **2010,** *22* (47), 5409-5413.

72. Vasimalla, S.; Senanayak, S. P.; Sharma, M.; Narayan, K. S.; Iyer, P. K., Improved Performance of Solution-Processed n-Type Organic Field-Effect Transistors by Regulating the Intermolecular Interactions and Crystalline Domains on Macroscopic Scale. *Chemistry of Materials* **2014**.

73. Zhan, X.; Facchetti, A.; Barlow, S.; Marks, T. J.; Ratner, M. A.; Wasielewski, M. R.; Marder, S. R., Rylene and Related Diimides for Organic Electronics. *Advanced Materials* **2011,** *23* (2), 268-284.

74. Rajaram, S.; Shivanna, R.; Kandappa, S. K.; Narayan, K. S., Nonplanar Perylene Diimides as Potential Alternatives to Fullerenes in Organic Solar Cells. *The Journal of Physical Chemistry Letters* **2012,** *3* (17), 2405-2408.

75. Wurthner, F.; Stolte, M., Naphthalene and perylene diimides for organic transistors. *Chemical Communications* **2011,** *47* (18), 5109-5115.

76. Kim, R.; Amegadze, P. S. K.; Kang, I.; Yun, H.-J.; Noh, Y.-Y.; Kwon, S.-K.; Kim, Y.-H., High-Mobility Air-Stable Naphthalene Diimide-Based Copolymer Containing Extended π-Conjugation for n-Channel Organic Field Effect Transistors. *Advanced Functional Materials* **2013,** *23* (46), 5719-5727.

77. Zhan, X.; Tan, Z. a.; Domercq, B.; An, Z.; Zhang, X.; Barlow, S.; Li, Y.; Zhu, D.; Kippelen, B.; Marder, S. R., A High-Mobility Electron-Transport Polymer with Broad Absorption and Its Use in Field-Effect Transistors and All-Polymer Solar Cells. *Journal of the American Chemical Society* **2007,** *129* (23), 7246-7247.

78. (a) Kolhe, N. B.; Asha, S. K.; Senanayak, S. P.; Narayan, K. S., n-Type Field Effect Transistors Based on Rigid Rod and Liquid Crystalline Alternating Copoly(benzobisoxazole) Imides Containing Perylene and/or Naphthalene. *The Journal of Physical Chemistry B* **2010,** *114* (50), 16694-16704; (b) Kim, B.-G.; Jeong, E. J.; Chung, J. W.; Seo, S.; Koo, B.; Kim, J., A molecular design principle of lyotropic liquid-crystalline conjugated polymers with directed alignment capability for plastic electronics. *Nat Mater* **2013,** *12* (7), 659-664.

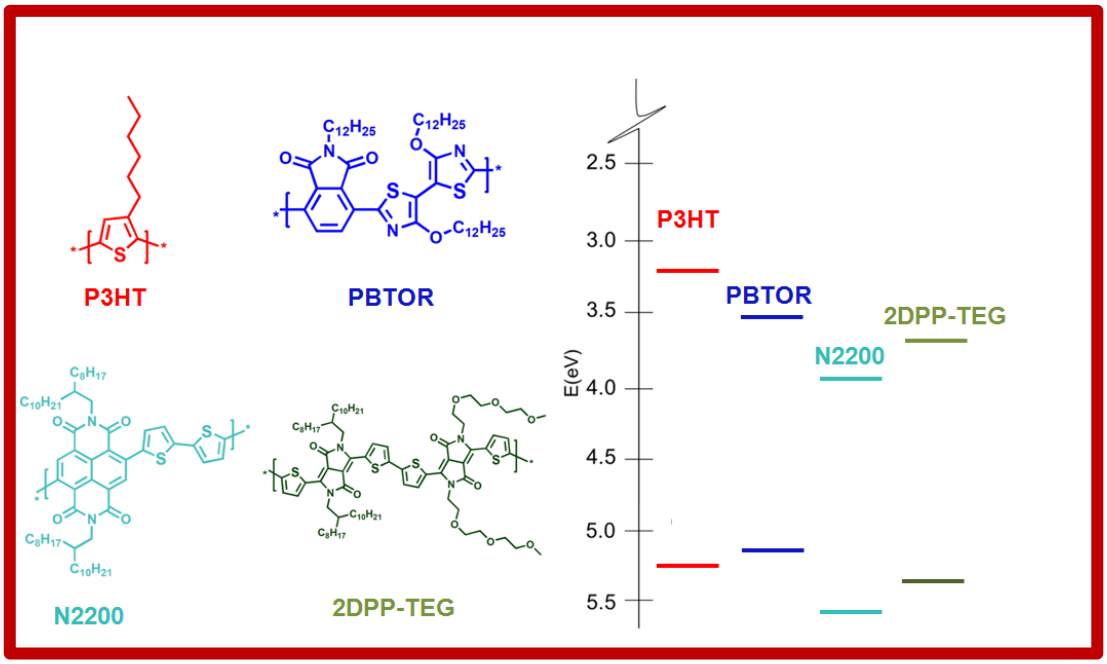
79. Babel, A.; Jenekhe, S. A., High Electron Mobility in Ladder Polymer Field-Effect Transistors. *Journal of the American Chemical Society* **2003,** *125* (45), 13656-13657.

80. Kolhe, N. B.; Devi, R. N.; Senanayak, S. P.; Jancy, B.; Narayan, K. S.; Asha, S. K., Structure engineering of naphthalene diimides for improved charge carrier mobility: self-assembly by hydrogen bonding, good or bad? *Journal of Materials Chemistry* **2012,** *22* (30), 15235-15246.

81. Sommer, M., Conjugated polymers based on naphthalene diimide for organic electronics. *Journal of Materials Chemistry C* **2014,** *2* (17), 3088-3098.

Chapter 2

Materials and Methods



Chapter 2

Materials and Methods

2.1 Introduction

The fabrication procedure and the processing conditions of the materials have a tremendous impact on the transport properties of the polymer based field effect transistors (PFETs). A pre-requisite for obtaining high performing PFETs is thus a proper choice of materials which have enhanced transport properties[1]. In addition, it should be ensured that the multiple layers of materials are compatible with each other for solution processable growth techniques[1-2]. This chapter discusses the fabrication procedure and the range of materials (semiconducting, dielectric and electrode) utilized for developing high performance PFETs. Also discussed are the measurement methods and the instrumentation associated with the FET characterization.

2.2 Polymer Semiconductors

Semiconducting materials utilized for the PFET application in the present studies include: p-type (hole conducting), n-type (electron conducting) or ambipolar (both electron and hole conducting) polymers. Each of these polymeric materials has a distinct fabrication procedure to obtain best performing devices. This section describes the characteristics of the semiconductors and the fabrication procedure used to optimize the PFET characteristics.

2.2.1 p-type semiconductors

a) P3HT

P3HT belongs to the group of alkyl-substituted poly-thiophene, commonly known as poly(3-alkyl-thiophene) (P3AT) which has been a model system for polymer electronics. These polymers are promising for optoelectronic applications owing to its thermal stability and excellent solution processability. A number of techniques based on electrochemical and oxidative polymerization have been reported for the synthesis of alkyl-thiophene based polymers with different molecular weight[3]. Based on the position of the alkyl chains in

consecutive thiophene units the polymer chains can be categorized into different conformations: head-to-head (HH) or head-to-tail (HT) or tail-to-tail (TT) combinations. These conformations have different conjugation length and transport properties[4]. Alkyl thiophenes can also be categorized as regio-random polymers which have randomly distributed conformations and regio-regular polymers containing only one of the conformations. Typically, μ_{FET} increases with increase in the degree of regio-regularity and falls by orders of magnitude for regio-random films[4-5]. Taking note of the effect polymer properties have on transport, poly-3-hexyl-thiophene with high molecular weight ~ 87000 g/mol, low polydispersity index of 1.2 and regio-regularity > 98 % was procured from American Dye Corporation and used for device fabrication without further purification. P3HT solution of 10 mg/ml concentration was prepared in chlorobenzene and spin coated at 1000 rpm for 1 minute to obtain films of thickness 50 – 80 nm. The films were then annealed at 110 °C for 30 minutes to remove the solvent and enhance the inherent crystallinity. Typical macromolecular organization of P3HT on the insulator is shown in **Figure: 2.1**.

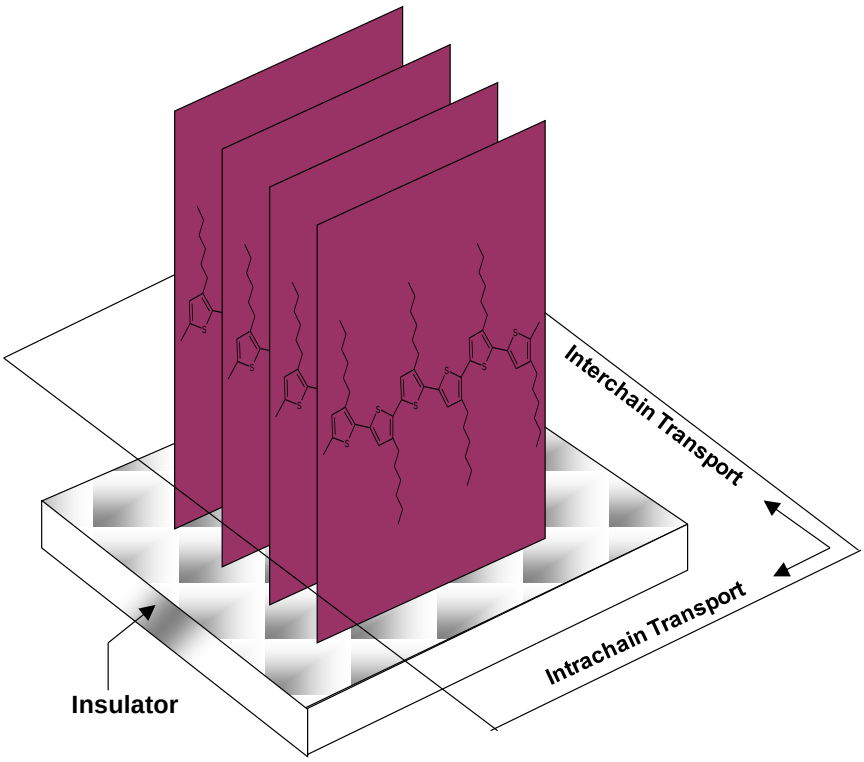


Figure 2.1: *Schematic of the self-assembled structure for P3HT molecule as obtained from the GIXRD measurement. Reproduced with permission from reference 4.*

b) PBTOR

Polymer chain conjugation length and co-planarity plays a critical role in enhancing the charge transport properties[6]. One of the strategies to enhance the co-planarity of the conjugated core is by using secondary forces like van der Waals interactions to obtain rigid structure[7]. Understanding these effects the polymer 4,4'-dialkoxy-5,5'-bithiazole (BtzOR) is designed.

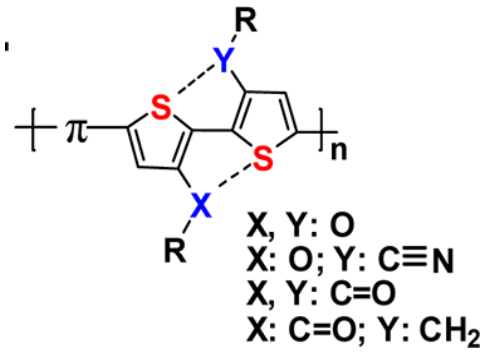


Figure 2.2:*Head-to-head linkages via intramolecular S···O conformational locking; S···O =S(thienyl)···O(alkoxy) and S(thienyl)···O(carbonyl). Reproduced with permission from reference 7*

This polymer takes advantage of secondary forces like the S(thiazolyl)···O(alkoxy) (**Figure: 2.2**) originating from the intramolecular interactions to obtain extended *π-π* conjugation and high crystallinity. Typical absorption spectrum of the polymer indicates a broad absorption with optical band-gap of 1.6 eV (**Figure: 2.3**).

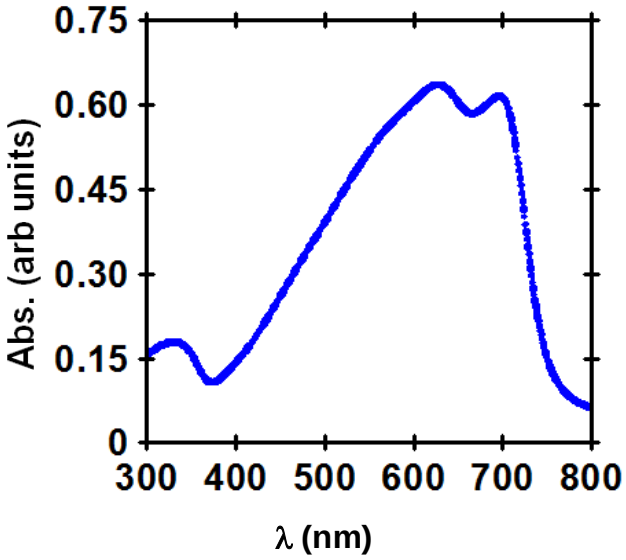


Figure 2.3: *Absorption Spectra of PBTOR thin films (~ 50 nm) coated on quartz substrate.*

XRD measurements performed on the polymer films demonstrate lamellar packing with diffraction pattern corresponding to backbone length and π-π stacking. The higher degree of crystallinity can also be attributed to the backbone co-planarity induced by the C−H···H−C repulsions between the phthalimide and thiazole units (**Figure: 2.6**) which ultimately enhances carrier mobility[7]. The structure of PBTOR polymer procured from Polyera ActivInk Inc. is shown in **Figure: 2.6**. This polymeric material was used for PFET fabrication without further purification. For the film preparation, PBTOR was dissolved in chlorobenzene (10 mg/ml concentration) and coated at 1000 rpm for 1 minute to obtain films of thickness 50 – 80 nm. The films were then annealed at 110 °C for 30 minutes to enhance the crystallinity.

2.2.2 n-type semiconductors

The electron transporting layer utilized for the studies in this thesis is the naphthalene based electron-depleted core. Among the numerous building blocks being developed to fabricate air stable *n*-channel semiconducting materials, rylene based polymers are promising due to planar aromatic core which demonstrate performances comparable to *p*-type semiconducting materials[8]. As a model *n*-type semiconducting polymer system, in this thesis, naphthalene diimde based N2200 or NDIOD-T2 ([poly{[*N*,*N*′-bis(2-octyldodecyl)-1,4,5,8-naphthalenedicarboximide-2,6-diyl]-*alt*-5,5′-(2,2′-bithiophene)} was used. Optical and electrochemical properties of NDIOD-T2 reveal the band gap to be ~ 1.45 eV (**Figure: 2.4**).

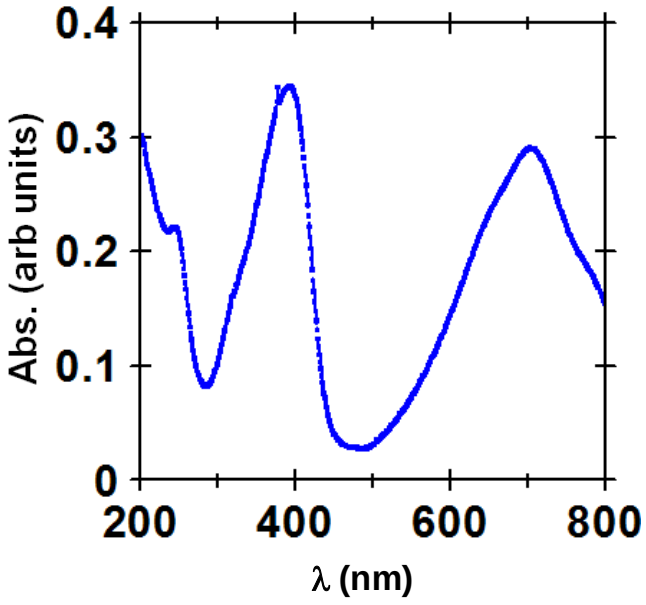


***Figure 2.4**: Absorption Spectra of N2200 thin films (~ 50 nm) coated on quartz substrate.*

Chemical structure of the polymer N2200 is seen in the **Figure: 2.6**. In this polymer, the long octa-decyl alkyl chain improves the solubility and the interdigitated structure enhances the π-π stacking. In addition the tighter packing ensures minimal percolation of moisture or oxygen to the core making this polymer stable to ambient conditions[9]. N2200 was obtained from Polyera Inc and used for various characterizations without further purification. Thin films were prepared by dissolving the polymer in cholorobenzene (10 mg/ml concentration) and spin coating at 1000 rpm for 1 minute. The films were then annealed at 110 °C for 2 hrs to enhance the order and ensure complete removal of the solvent.

2.2.3 Ambipolar semiconductors

Ambipolar semiconductors are of interest for the development of complementary electronics. Hence, in recent years focused efforts have been devoted towards the development of polymeric materials with both *n*-type and *p*-type transport[10]. Diketopyrrolopyrole (DPP) molecules are one of the most investigated high performing polymeric material[11]. For studies involving ambipolar transport DPP based high performing co-polymer referred as 2DPP-TEG (**Figure: 2.6**) was used. 2DPP-TEG was synthesized by the co-polymerization of two DPP-DPP moieties with amphiphillic substitution of triethylene glycol (TEG) and dodecyl chain. The strong intermolecular interaction between the DPP-DPP units induces self-assembly leading to excellent charge transport[12]. In addition, the TEG chain increases the solubility and the amphiphillic substitution enhances the aggregation dynamics, resulting in spontaneous crystallization. The absorption spectra of the co-polymer extend up to ~ 1000 nm with optical band-gap of 1.2 eV[13]. Other relevant parameters of the polymer include high weight average molecular weight of 314 kg/mol and a polydispersity index of ~ 4.

The macromolecular assembly of 2DPP-TEG was observed using GIXRD experiments. GIXRD pattern indicates edge-on stacking of the polymer on the insulating layer (**Figure: 2.5**). This results in isolating the conjugated core from the dielectric induced polar disorder, and hence the density of states (DOS) in this polymer is unaffected by the underlying dielectric layer. 2DPP-TEG polymer was dissolved in chlorobenzene and coated at 1000 rpm for 1 minute to obtain films of thickness of 50 - 80 nm. The polymer films were then annealed at 180 °C for 2 hrs to optimize the transport performance.

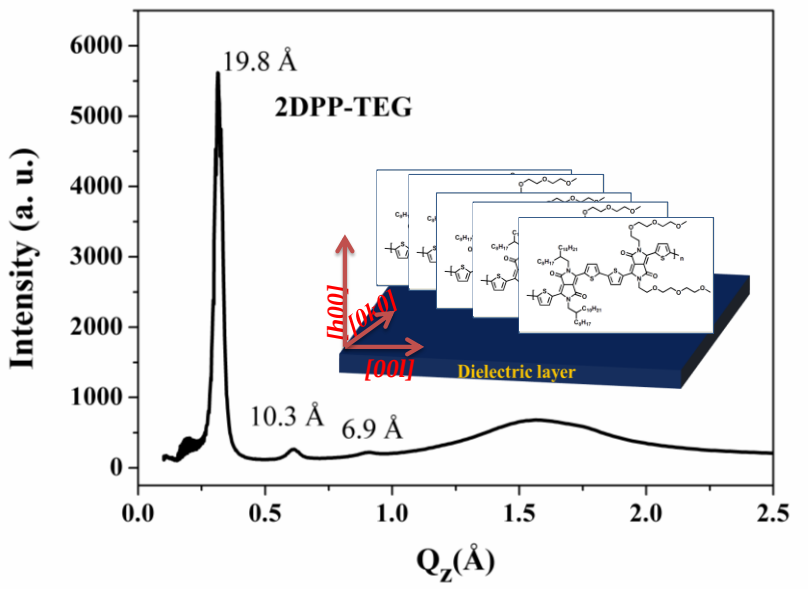


Figure 2.5: *Schematic of the edge-on stacking of 2DPP-TEG molecule on the dielectric layer as obtained from GIXRD*

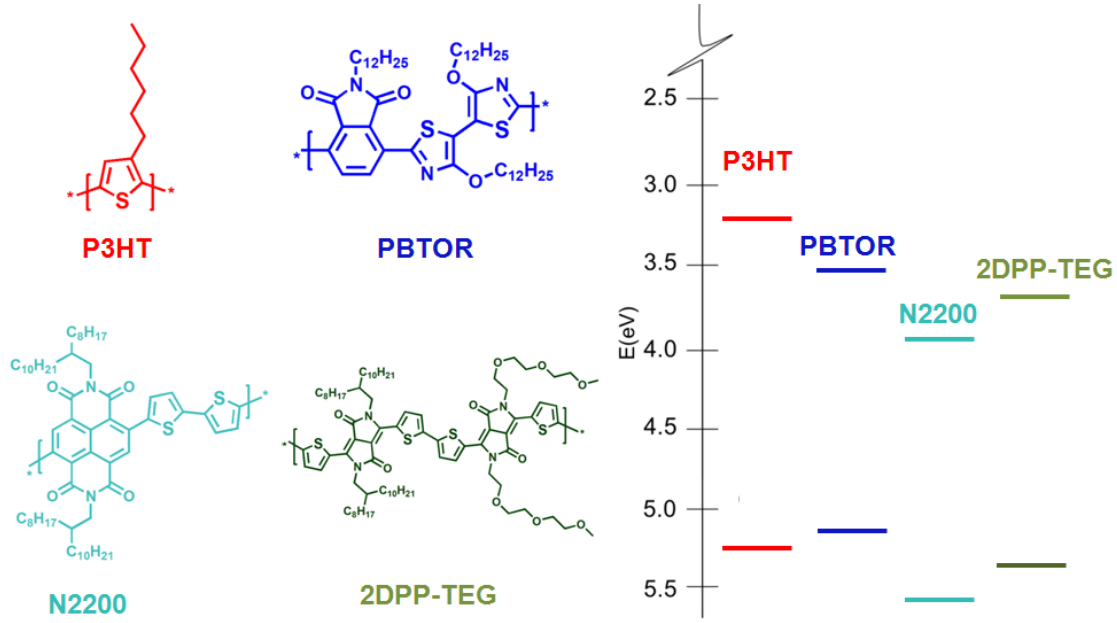


Figure 2.6: *Structure and energy levels of different semiconductors utilized for the studies in the thesis. The color utilized for the structure is reflective of the solution color.*

2.3 Dielectric layer

Dielectric layer plays a key role in the operation of the PFET. In general it is observed that, high-*k* dielectric layer result in broadening the DOS of the polymer semiconductor which hinders the transport in the PFET [14]. In addition, it is also observed that the roughness of the dielectric layer also significantly modifies the microstructure of the semiconducting films[15]. Hence, one of the important steps in obtaining high performance PFETs is to have dielectric layer which forms optimum interface with the semiconducting layer. Dielectric layers can be categorized based on polarizability as ferroelectric (FE) or paraelectric (PE) and depending on the dielectric constant as high-*k* or low-*k* dielectric materials. This section characterizes the dielectric materials utilized for the studies in this thesis.

2.3.1 Divinyltetramethyldisiloxane-bis(benzocyclobutene) (BCB)

BCB dielectric layer (structure in **Figure: 2.7**) was obtained from Dow Chemicals and used for device fabrication by diluting with Mesitylene (Spectroscopic Grade) in the ratio 1:1. The diluted BCB solution, was spin coated at 800 rpm for 1 minute and annealed inside a glove box at 290 ^{o}C for 30 - 45 mins to obtain films of thickness 0.6 μm. BCB is a thermosetting polymer which requires a curing temperature of 250 ^{o}C for obtaining a dense polymer network which is leakage free. Curing the BCB films enhances the gap-filling properties, polarization and results in low moisture absorption. MIM structures fabricated (detailed in section 2.5.1) from this dielectric material demonstrated a *k* value close to 2.65 with negligible frequency dispersion till 10 MHz[16]. BCB delivers highly transparent films with refractive index of 1.44 (, an important prerequisite for optically active devices.

2.3.2 Poly(methyl-methacrylate (PMMA)

PMMA (**Figure: 2.7**) is a transparent thermoplastic often used as a lightweight or shatter-resistant alternative to glass. PMMA pellets were obtained from Sigma Aldrich Inc. These pellets were dissolved in polar solvents like propylene carbonate to obtain a concentration of 80 mg/ml. The solution was then spin coated inside the glove box at 1000 rpm for 1 minute and annealed at 110 ^{o}C for 1 hr. Annealing removes the solvent and provides leakage free dielectric films. The resultant optical quality transparent dielectric films had refractive index ~ 1.42 (at λ ~ 632 nm), and *k* ~ 3.6 (at 10 kHz). For solutions of PMMA prepared with low polarity solvents like chlorobenzene, cross-linkers were needed to obtain leakage free behavior.

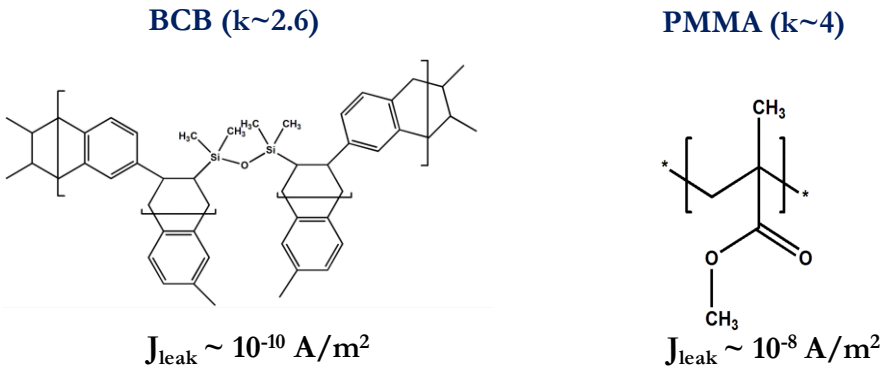


Figure 2.7: *Structure, dielectric constant and the leakage properties of the BCB and PMMA dielectric layer.*

2.3.3 Polyvinylidene Fluoride (PVDF)

PVDF based dielectrics are known to exist in three regular conformations corresponding to its phases with similar potential energies. The three known conformations correspond to *all-trans(β-phase),tg^+tg^-(α-phase)* and *$tttg^+tttg^-$(γ-phase)*, with *β-phase* as the most polar FE-phase. In this thesis, both homopolymers of PVDF as well as co-polymers like - P(VDF-Hexafloropropylene) (PVDF-HFP) and P(VDF-Trifloroethylene) (PVDF-TrFE) were used for the studies. The structure of these polymer dielectrics is shown in **Figure: 2.8**.

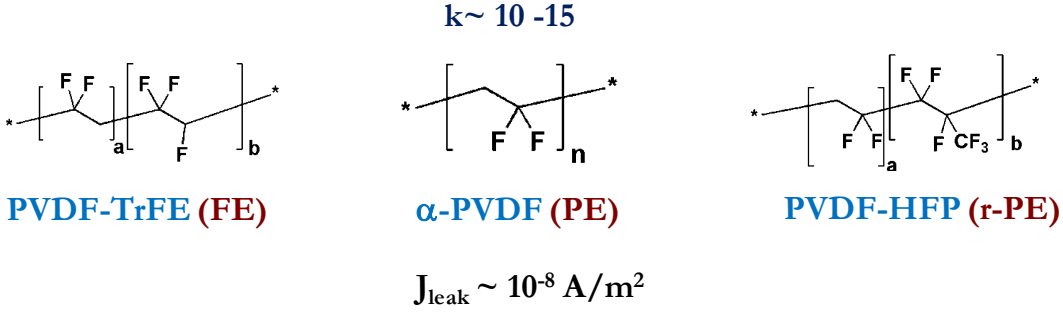


Figure 2.8: *Structure, dielectric constant and the leakage properties of PVDF based polymer dielectrics in different phases.*

The phases in these dielectric materials can be controlled by the processing condition, the substrate and by applying external strain. PVDF based dielectric films were prepared by dissolving the pellets in the respective solvents: PVDF, PVDF-HFP in dimethylformamide at 80 mg/ml and PVDF-TrFE in butanone or cyclohexanone at 40 mg/ml. The solutions are then spin coated at 800 rpm for 1 minute. This was followed by

annealing the films at 150 · Typical thickness of the dielectric layers was maintained in the range of 0.2 - 0.4 μm. These processing conditions were chosen to ensure the formation of desirable ferroelectric and paraelectric phases[17]. The films were characterized to obtain a typical *k* of 10 – 15 [18]. Owing to its high polarity, this dielectric material has a frequency dispersion, and it was observed that for frequencies greater than 10 kHz the bulk dielectric constant decreases significantly[19].

2.3.4 Self-assembled Nano-dielectrics (SAND)

This is a unique class of multi-layered high-*k* dielectric material obtained by a combination of organic-inorganic dielectric layers through a solution processable method.

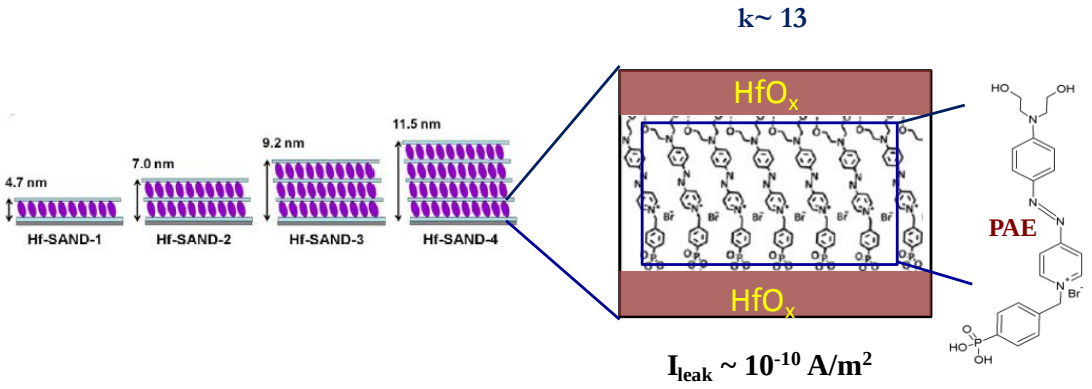


Figure 2.9: *Schematic of the multi-layered SAND growth techniques. Zoomed figure indicates the composition of each SAND layer*

The structure includes inorganic HfO_x layer obtained by atomic layer deposition or sol-gel method (films of thickness 1 - 2 nm). The sol-gel coated films were annealed at 150 °C for 1 hr. This was followed by self-assembling of high-polar organic layer by immersing the substrates in a preheated ~ 3 mM solution of PAE: 4-[[4-[bis(2-hydroxyethyl)amino]phenyl]diazenyl]-1-[4(diethoxyphosphoryl)benzyl]pyridinium bromide for 1 h at 60 °C. Multilayered variants of the SAND dielectric structures were obtained by controlling the number of self-assembled bi-layers for HfO_x and PAE, and denoted by the index *n* (**Figure: 2.9**)[20]. The advantage of this dielectric structure is the precise control of the thickness in the range of 8 nm – 50 nm which was obtained by multiple iteration of self-assembly under ambient condition. Typical *k* of 13 and a maximum capacitance of 0.8 μF/cm^2 was obtained for the multilayered structure.

2.4 Metal Electrodes

Metal electrodes were coated by physical vapor deposition technique in all the cases. Typical condition for the vapor deposition involves: 10^{-6} mbar vacuum, deposition rate of 1 Å/s and a film thickness of 40 nm. For *p*-FETs, Au based S-D electrodes were utilized and for *n*-FETs Al as well as Au S-D electrodes were used depending on the injection behavior of the semiconductor.

Patterned gate electrodes were utilized for all the PFETs. The gate electrodes were obtained under 10^{-6} mbar vacuum by physical vapor deposition. Patterning of the electrodes minimizes the parasitic capacitance due to decreased overlap of the source, drain, gate electrode and enhances the dynamic performance of the PFETs (details in chapter 5). The width of the gate pattern was varied in the range of 5 μm to 250 μm to obtain PFETs with different channel length and retain low parasitic capacitance. Al electrodes were used as gate in the studies involving PFETs fabricated with PE polymer dielectrics[14b]. However, in the PFET devices with FE dielectric layer Au electrodes were used since native oxide of the Al result in a depolarizing field at the gate-dielectric interface[17, 21]. In the SAND based PFETs, where the self assembly of the layers require a hydrophilic surface Al electrodes were utilized as the gate electrode.

2.5 Device Fabrication

2.5.1 Capacitor

Metal-Insulator-Metal (MIM) structures (**Figure: 2.10**) were fabricated with dielectric materials sandwiched between two metal electrodes.

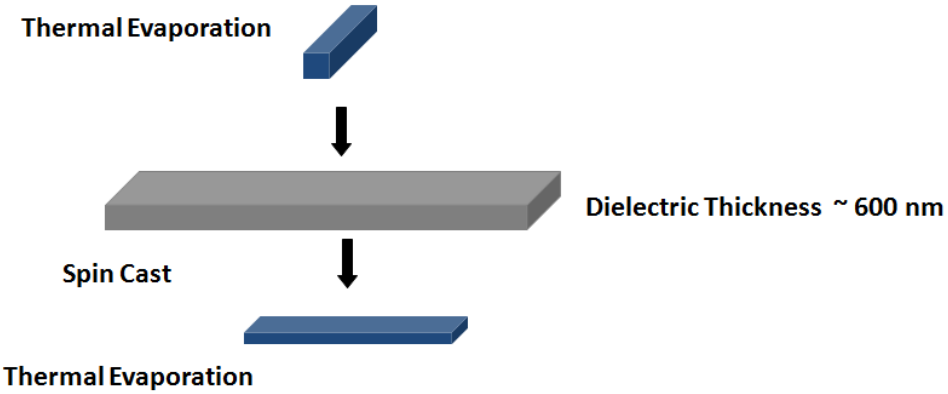


Figure 2.10: *Schematic of the fabrication procedure for a MIM capacitor*

The fabrication procedure involves coating of metal electrodes (10^{-6} mbar, 1 Å/s, 40 nm thick) on RCA treated glass substrates and then introducing the polymer thin films. This was then followed by depositing the next metal layer (10^{-6} mbar, 1 Å/s, 40 nm thick) by physical vapor deposition. In some cases, MIM structures are fabricated next to the PFETs to simultaneously monitor the variation in the dielectric constant as well as the PFET properties.

2.5.2 Diode

Hole only diode devices were fabricated on pre-cleaned ITO substrates (15 ohm/□), obtained from XINYAN Technology Ltd. with a typical architecture of (ITO/PEDOT:PSS/Polymer/Au). The PEDOT:PSS layer was spin coated at 2000 rpm and annealed at 110 °C for 1 hour in air. Polymer films of varying thickness (200 nm to 2 μm) were obtained and annealed in N_2 atmosphere. Electron only devices were fabricated on Al coated pre-cleaned glass substrates on which polymer layer was coated followed by Al cathode electrode. Metal electrodes were coated by thermal evaporation (10^{-6} mbar, 1 Å/s, 60 nm thick).

2.5.3 Polymer Field Effect Transistor (PFET)

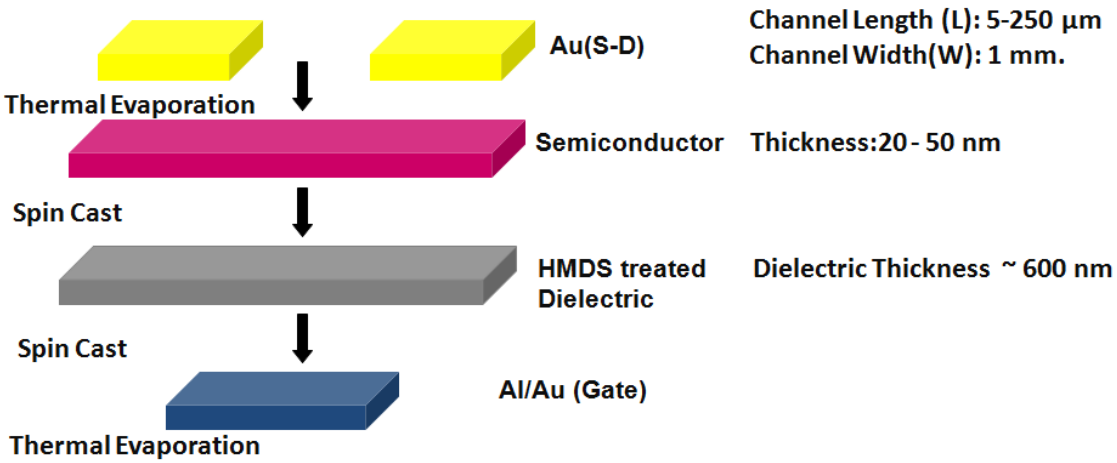


Figure 2.11: *Schematic of the PFET fabrication procedure.*

PFETs were fabricated on RCA treated glass substrates coated with metal gate electrodes. The metal gate electrodes were coated using a physical vapor deposition method under vacuum condition of 10^{-6} mbar with a typical rate of 1 Å/s. Thickness of the metal electrodes were maintained at 20 – 40 nm. This was followed by the coating of dielectric layers in the desired phase as required for the study. On top of the dielectric layer a thin

monolayer of hexamethyldisiloxane (HMDS) was introduced at 1500 rpm for 1 minute and annealed at 110 °C for 2 hrs. Polymer thin films are then introduced on these substrates and annealed under specific condition essential for obtaining ordered and crystalline structures. The devices were then completed by coating S-D electrodes (10^{-6} mbar, 1 Å/s, 20 nm thick) which could be Al or Au depending on the semiconducting material. Schematic of the procedure is shown in **Figure: 2.11**.

2.5.4 Hall Measurement

In principle, Hall measurement can be performed on any set of electrodes which are not linear.

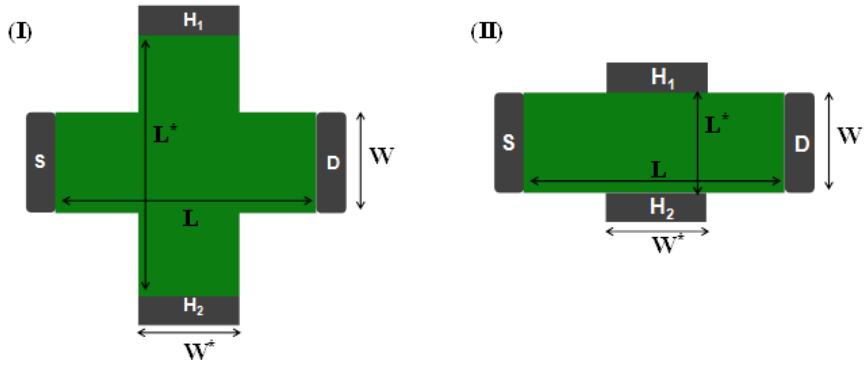


Figure 2.12: *Top view of the device used for Hall measurement where, L is the channel length, L^* is the distance between the Hall probes (H_1 and H_2), W is the channel width and W^* is the width of the Hall probes. The green region corresponds to the patterned semiconductor. Geometry I corresponds to the van der Pauw method and geometry – II is referred as the Hall bar geometry.*

Typical geometries utilized for the Hall measurement in different semiconductors are shown in **Figure: 2.12**. Both the geometries have been utilized for the measurement of Hall Voltage in semiconducting materials. However, geometry – I has certain advantages over geometry –II which are as follows:

(i) In geometry- I, the effect of V_{ds} on the Hall voltage is minimized since the Hall probes (H_1 and H_2) are far away from the channel area.

(ii) Error analysis was performed on both the geometries to obtain the preferred geometry for the estimation of Hall parameter for a polymer semiconductor. The error in geometry- I can be estimated as[22]:

$$\frac{\Delta\mu_{Hall}}{\mu_{Hall}} \approx e^{-\pi\left(\frac{L-W^*}{2W^*}\right)} \qquad \text{…….. (2.1)}$$

For device parameters: $L \approx 0.1 – 0.2$ mm, $W \approx 0.5$ mm, $L^* \approx 0.1 – 0.2$ mm, $W^* \approx 0.1$ mm $\frac{\Delta\mu_{Hall}}{\mu_{Hall}}$ is obtained to be in the range of 0.04 – 0.15

Similarly, the error in geometry-**II** can be expressed as:

$$\frac{\Delta\mu_{Hall}}{\mu_{Hall}} \approx \left(1 - e^{-\pi\left(\frac{L}{2W}\right)}\right)\left(1 - \frac{2W^*}{\pi W}\right) \qquad \text{…….. (2.2)}$$

For device dimensions of : $L \approx 1 – 3$ mm, $W \approx 0.2 – 1.4$ mm, $L^* \approx 0.3 – 0.6$ mm, $W^* \approx 0.5$ mm.

$$\frac{\Delta\mu_{Hall}}{\mu_{Hall}} \approx 0.22 – 0.45 \qquad \text{…….. (2.3)}$$

As evident from the error calculation geometry – I is more accurate than geometry – II for the estimation of the Hall parameters. Hence, for all the Hall measurement studies geometry – I was preferred.

This device fabrication procedure involved patterning the spin coated semiconducting film by lithographic and printing techniques. This was then followed by fabricating multiple electrodes in a cross fashion as shown in the **Figure: 2.12** by physical masking technique. It was ensured that the distance between Hall probes was comparable to the width of the source-drain electrodes and, the width of the Hall probes was smaller than the channel length.

2.5.5 Logic Circuits

Complementary inverters and NAND gates were fabricated as top-contact bottom gate structure with the required polymer semiconducting layers. For the device fabrication multiple embedded gate electrodes are coated on a single glass substrate to fabricate the required number of transistors. The logic circuits were then completed using fabrication techniques as used for the individual PFET devices. The metallic interconnects between the transistors were coated by thermal evaporation of Au after the fabrication of individual transistors. Noise margin and gain was optimized by varying the electrode width of the load and driver PFETs. The schematic of typical logic circuits is shown in **Figure: 2.13**.

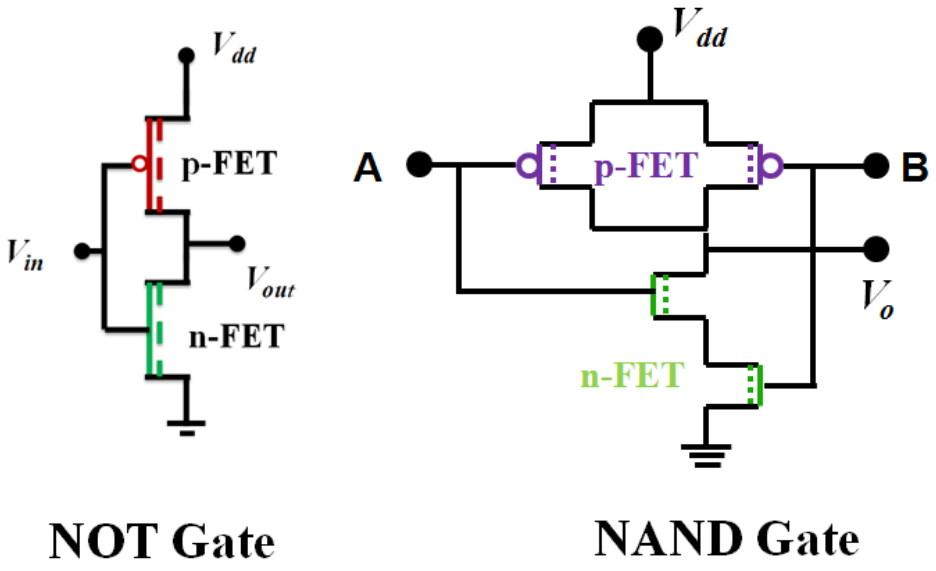


Figure 2.13: *Schematic of the connections for the logic circuits fabricated as a part of the study in this thesis.*

2.6 Experimental Techniques

2.6.1 C-V measurements

The MIM devices were characterized using the in-built *C-V* meter of Keithley 4200 SCS and HP4294A. The procedure for measurement involved applying a small ac voltage in the range of 30 -100 mV and measuring the capacitive response at different frequencies. A complete picture of the capacitive behavior of the dielectric materials was obtained by measuring the capacitance response with different bias voltage to estimate the effective capacitance at the transport interface with different magnitude of V_g.

2.6.2 DC Characterization

PFET devices were characterized for the standard output and transconductance measurements to estimate the μ_{FET} and I_{on}/I_{off} ratio by a set up consisting of Keithley 2400 source meter and high impedance Keithley 6514 Electrometers or Keithley 4200 SCS parameter analyzer (**Figure: 2.14**). The instruments were driven by a home built Labview program. The devices parameters were extracted by the expression: $I_{ds} = \frac{\mu_{FET} W C_i}{2L}(V_g - V_t)^2$, where W is the channel width, L is the channel length, C_i is the capacitance per unit area of the dielectric structure. For studying bias stress of the PFET devices, continuous bias was applied for 10^4 seconds and transconductance plots were measured at regular

intervals. Similarly, the stability of the devices were monitored from the transconductance curve while the device was exposed to ambient condition.

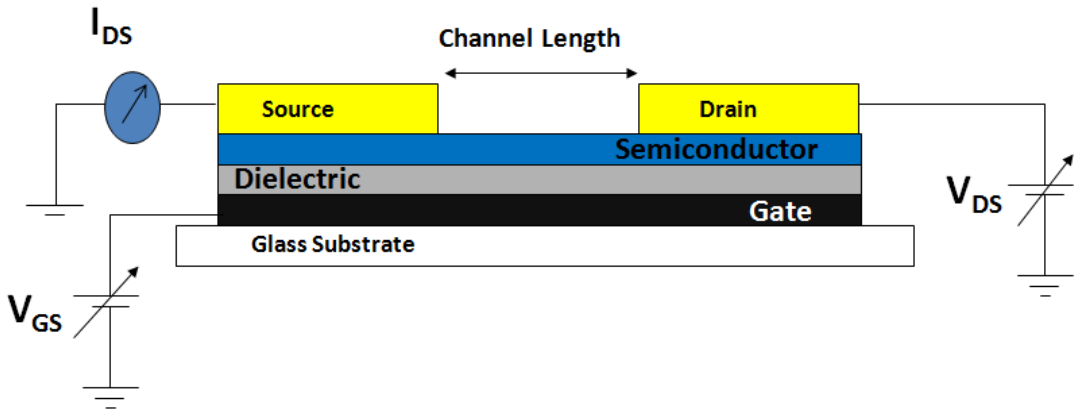


Figure 2.14: *Experimental Set-up for DC characterization of the PFETs.*

The temperature dependent transport measurements were performed using a closed cycle Helium Cryo set-up (CTI Inc). During the measurement, it was ensured that the devices were maintained under vacuum of 10^{-3} – 10^{-4} mbar where external factors originating from condensed phase of water do not create variations in the T of the chamber.

Space Charge Limited Current (SCLC) measurements were performed by applying bias using Keithley 2400 Sourcemeter and measuring the current using Keithley 6514 Electrometer which were controlled by a custom-made Lab view program.

For the polymer inverters the input-output transfer characteristics were obtained using a set up consisting of Keithley 2400 Sourcemeter which applies the input voltage and the output was monitored using Keithley 6514 Electrometer.

2.6.3 AC Characterization

A train of square voltage pulse (±80 V or ± 40 V for n-FET and p-FET respectively) was applied at the gate with an arbitrary waveform generator (K-Pulse Card Keithley or SMU) while the drain electrode was held at a DC bias (0 or ± 80 V using Keithley 2400).The transistor switching speed was measured by monitoring the voltage drop across a resistor ($R \approx 1$–10 kΩ depending on the channel length), which is connected between the source electrode and ground. The voltage was monitored using a Lecroy 6100A oscilloscope with a typical input impedance of 1 MΩ. The input capacitance of the set up (Lecroy 6100A and the RF probes) was < 5.5 pF with RC time constant ≈ 5 ns. Similarly, to obtain the drain transient response square pulses (± 80 V or ± 40 V) were

applied at the drain end and voltage at the resistor ($R \approx 0.1 - 5$ kΩ) between the source and ground was monitored while keeping the bias at the gate electrode constant (0 or ± 80 V).

Another figure of merit for PFETs is the frequency-bandwidth product. The frequency-bandwidth product of the PFETs were estimated by monitoring the AC component of I_d (i_d) and I_g (i_g) using a combination of SR 830 lock-in amplifier (bandwidth ~ 100 kHz) and signal generator (HP 8116A of bandwidth 50 MHz). The unity gain frequency was determined as the frequency at which the gain of the device was 1 or $i_d \approx i_g$.

2.6.4 Optoelectronic measurement

The optical response of the top contact bottom gated FETs were monitored by illuminating from both channel side as well from gate side. In the case where illumination was performed from the gate side, the PFETs were fabricated with ITO as the gate electrode. Typical setup of the optoelectronic measurements is shown in **Figure: 2.15**.

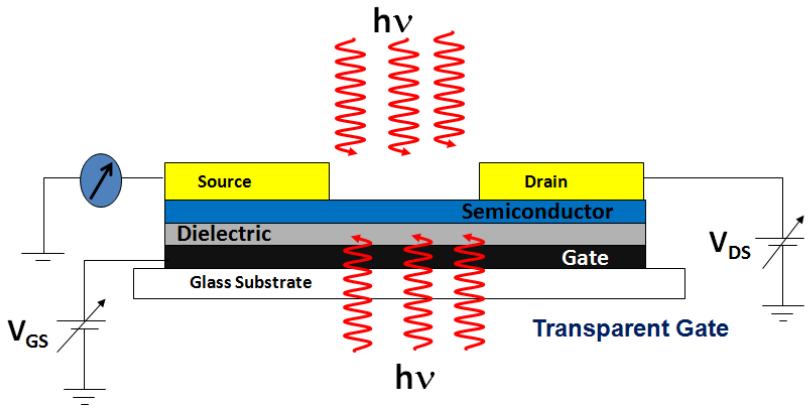


Figure 2.15: *Typical setup for obtaining the photo response of a PFET by both top or bottom illumination.*

The DC characteristics of the PFET were then monitored using Keithley 2400 Source meter and Keithley 6514 Electrometer to obtain information regarding the charge transport in PFETs under illumination.

2.6.5 Magnetic Measurement

For the magnetic measurement on working PFET devices, a home home-built probe assembly was utilized inside a physical property measurement system obtained from Quantum Design Inc. In this set-up it was possible to sweep ***B*** from 8 T to - 8 T in the steps of 0.1 T using He-cooled super-conducting magnets. The biasing for the PFETs were provided by Keithley 2400 Sourcemeter and magnetoresistance or Hall Voltage was monitored using Keithley 2001 Multimeter (input impedance ~ 10 TΩ). Direction of the magnetic field and current was altered to obtain reproducible and consistent measurements.

In addition, magnetic measurements were also performed at different T to observe the variation in Hall voltage or magnetoresistance with T. In the T dependent setup, it was ensured that the samples were maintained under a vacuum of 10^{-3} – 10^{-4} mbar to avoid the effect of external factors on the measurement.

2.6.6 AFM Characterization

Surface morphology and phase contrast of the materials were obtained using the standard, JPK Nanowizard 3 AFM with Cr/Pt coated conducting tip (Multi-75E, Resonant frequency, ω_R ~ 75 kHz) or Aluminum coated silicon nitride-cantilevers (force constant 40 N/m and resonance frequency ω_R ~ 375 kHz) obtained from Budget Sensors.

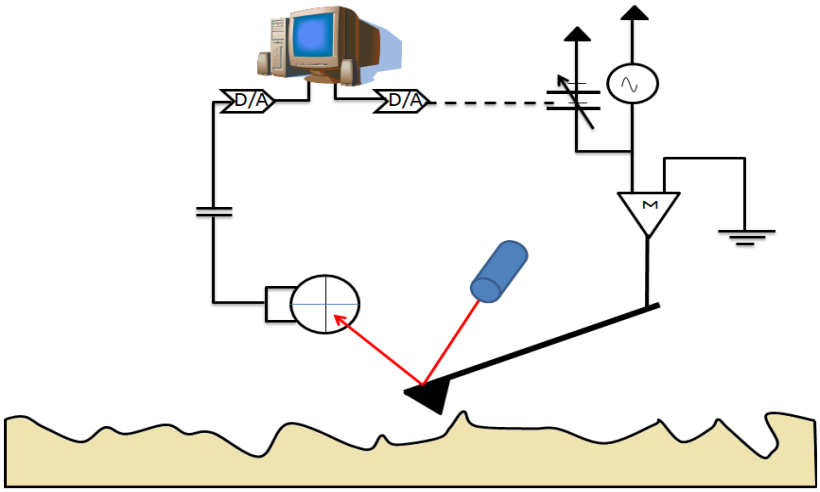


Figure 2.16: *Schematic of the setup used for SCM measurement of the dielectric surface.*

Surface electrical characterizations of the dielectric films were performed for dielectric layers grown on ITO coated substrates by the Scanning Capacitance Microscopy (SCM) technique. The experimental procedure involves measuring the surface electrostatic force which is proportional to *dC/dz* using a Cr/Pt coated conducting tip (Multi-75E, Resonant frequency, ω_R = 75 kHz). A schematic of the set up is shown in **Figure: 2.16**. SCM retrace measures the capacitive force using lock-in amplitude at ω_R, while the tip was driven at $\omega_R/2$ in hover mode (1 nm - 40 nm). To estimate the dipole response, poling of dielectric surface was performed using an in-built sinusoidal source (7 $V_{p\text{-}p}$) through the tip. SCM was then performed on the biased area to measure the difference of force or the surface capacitance with poling and obtain the average polarization contrast (*dP*). The polarization contrast is the measure of the frequency response of the surface dipoles.

2.7 Summary

With a combination of novel materials design and device engineering it was possible to obtain high performing PFETs. Range of materials which cover different classes of dielectric layers, semiconducting materials and gate electrodes were utilized to explore the working of these devices. A combination of electrical, optical and magnetic measurements were performed on these high performing devices to obtain better understanding of the charge transport in polymer FETs. The work described in the next chapters is towards this direction, which involve both design of high performing polymer circuits as well as basic understanding of charge transport in these novel materials.

References

1. Klauk, H., Organic thin-film transistors. *Chem. Soc. Rev.* **2010,** *39* (7), 2643-2666.
2. Burgi, L.; Friend, R. H.; Sirringhaus, H., Formation of the accumulation layer in polymer field-effect transistors. *Appl. Phys. Lett.* **2003,** *82* (9), 1482-1484.
3. McCullough, R. D., The Chemistry of Conducting Polythiophenes. *Advanced Materials* **1998,** *10* (2), 93-116.
4. Sirringhaus, H.; Brown, P. J.; Friend, R. H.; Nielsen, M. M.; Bechgaard, K.; Langeveld-Voss, B. M. W.; Spiering, A. J. H.; Janssen, R. A. J.; Meijer, E. W.; Herwig, P.; de Leeuw, D. M., Two-dimensional charge transport in self-organized, high-mobility conjugated polymers. *Nature* **1999,** *401* (6754), 685-688.
5. Zen, A.; Pflaum, J.; Hirschmann, S.; Zhuang, W.; Jaiser, F.; Asawapirom, U.; Rabe, J. P.; Scherf, U.; Neher, D., Effect of Molecular Weight and Annealing of Poly(3-hexylthiophene)s on the Performance of Organic Field-Effect Transistors. *Adv. Funct. Mater.* **2004,** *14* (8), 757-764.
6. Noriega, R.; Rivnay, J.; Vandewal, K.; Koch, F. P. V.; Stingelin, N.; Smith, P.; Toney, M. F.; Salleo, A., A general relationship between disorder, aggregation and charge transport in conjugated polymers. *Nat Mater* **2013,** *12* (11), 1038-1044.
7. Guo, X.; Quinn, J.; Chen, Z.; Usta, H.; Zheng, Y.; Xia, Y.; Hennek, J. W.; Ortiz, R. P.; Marks, T. J.; Facchetti, A., Dialkoxybithiazole: A New Building Block for Head-to-Head Polymer Semiconductors. *Journal of the American Chemical Society* **2013,** *135* (5), 1986-1996.
8. Chen, Z.; Zheng, Y.; Yan, H.; Facchetti, A., Naphthalenedicarboximide- vs Perylenedicarboximide-Based Copolymers. Synthesis and Semiconducting Properties in Bottom-Gate N-Channel Organic Transistors. *Journal of the American Chemical Society* **2008,** *131* (1), 8-9.
9. (a) Schuettfort, T.; Huettner, S.; Lilliu, S.; Macdonald, J. E.; Thomsen, L.; McNeill, C. R., Surface and Bulk Structural Characterization of a High-Mobility Electron-Transporting Polymer. *Macromolecules* **2011,** *44* (6), 1530-1539; (b) Rivnay, J.; Toney, M.

F.; Zheng, Y.; Kauvar, I. V.; Chen, Z.; Wagner, V.; Facchetti, A.; Salleo, A., Unconventional Face-On Texture and Exceptional In-Plane Order of a High Mobility n-Type Polymer. *Advanced Materials* **2010,** *22* (39), 4359-4363.

10. Chen, J.; Cao, Y., Development of Novel Conjugated Donor Polymers for High-Efficiency Bulk-Heterojunction Photovoltaic Devices. *Accounts of Chemical Research* **2009,** *42* (11), 1709-1718.

11. Hao, Z.; Iqbal, A., Some aspects of organic pigments. *Chemical Society Reviews* **1997,** *26* (3), 203-213.

12. Braga, D.; Horowitz, G., High-Performance Organic Field-Effect Transistors. *Advanced Materials* **2009,** *21* (14-15), 1473-1486.

13. Kanimozhi, C.; Yaacobi-Gross, N.; Chou, K. W.; Amassian, A.; Anthopoulos, T. D.; Patil, S., Diketopyrrolopyrrole–Diketopyrrolopyrrole-Based Conjugated Copolymer for High-Mobility Organic Field-Effect Transistors. *Journal of the American Chemical Society* **2012,** *134* (40), 16532-16535.

14. (a) Veres, J.; Ogier, S. D.; Leeming, S. W.; Cupertino, D. C.; Mohialdin Khaffaf, S., Low-k Insulators as the Choice of Dielectrics in Organic Field-Effect Transistors. *Adv. Funct. Mat.* **2003,** *13* (3), 199-204; (b) Senanayak, S. P.; Guha, S.; Narayan, K. S., Polarization fluctuation dominated electrical transport processes of polymer-based ferroelectric field effect transistors. *Phys. Rev. B* **2012,** *85* (11), 115311; (c) Hulea, I. N.; Fratini, S.; Xie, H.; Mulder, C. L.; Iossad, N. N.; Rastelli, G.; Ciuchi, S.; Morpurgo, A. F., Tunable Frohlich polarons in organic single-crystal transistors. *Nat. Mat.* **2006,** *5* (12), 982-986.

15. Facchetti, A.; Yoon, M. H.; Marks, T. J., Gate Dielectrics for Organic Field-Effect Transistors: New Opportunities for Organic Electronics. *Adv. Mater.* **2005,** *17* (14), 1705-1725.

16. Lay-Lay, C.; Jana, Z.; Jui-Fen, C.; Eric, C. W. O.; Peter, K. H. H.; Henning, S.; Richard, H. F., General observation of n-type field-effect behaviour in organic semiconductors. *Nature* **2005,** *434* (7030), 194-199.

17. Kang, S. J.; Park, Y. J.; Sung, J.; Jo, P. S.; Park, C.; Kim, K. J.; Cho, B. O., Spin cast ferroelectric beta poly(vinylidene fluoride) thin films via rapid thermal annealing. *Appl. Phys. Lett.* **2008,** *92* (1), 012921.

18. Senanayak, S. P.; Guha, S.; Narayan, K. S., Polarization fluctuation dominated electrical transport processes of polymer-based ferroelectric field effect transistors. *Physical Review B* **2012,** *85* (11), 115311.

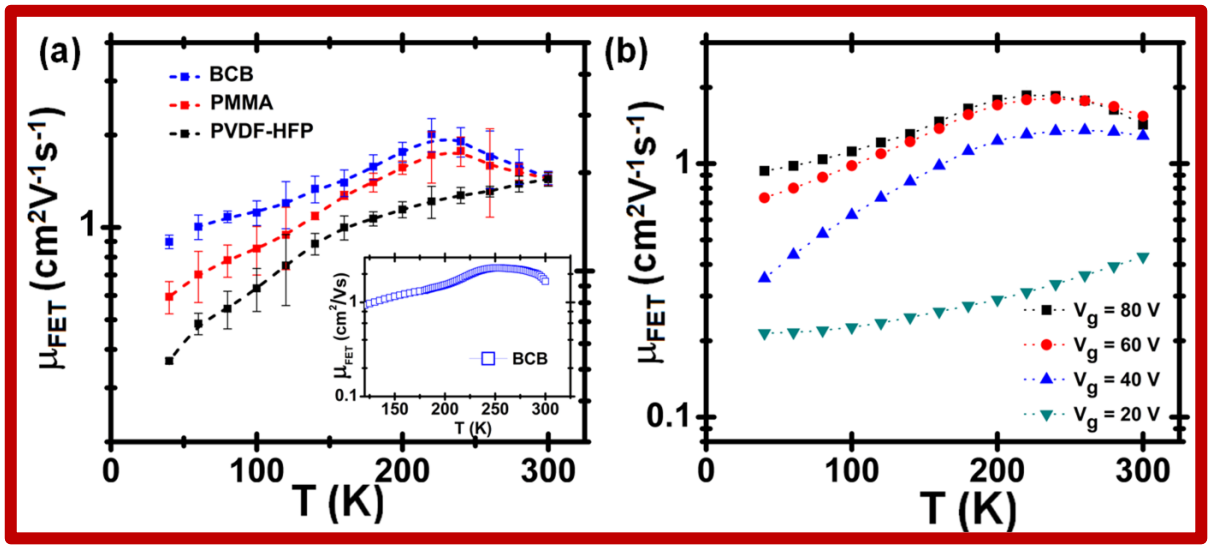
19. Senanayak, S. P.; Narayan, K. S., Strategies for Fast-Switching in All-Polymer Field Effect Transistors. *Advanced Functional Materials* **2014,** *24* (22), 3324-3331.

20. Everaerts, K.; Emery, J. D.; Jariwala, D.; Karmel, H. J.; Sangwan, V. K.; Prabhumirashi, P. L.; Geier, M. L.; McMorrow, J. J.; Bedzyk, M. J.; Facchetti, A.; Hersam, M. C.; Marks, T. J., Ambient-Processable High Capacitance Hafnia-Organic Self-Assembled Nanodielectrics. *Journal of the American Chemical Society* **2013,** *135* (24), 8926-8939.

21. Xia, F.; Xu, H.; Fang, F.; Razavi, B.; Cheng, Z.-Y.; Lu, Y.; Xu, B.; Zhang, Q. M., Thickness dependence of ferroelectric polarization switching in poly(vinylidene fluoride--trifluoroethylene) spin cast films. *Appl. Phys. Lett.* **2001,** *78* (8), 1122-1124.
22. Mey, G. D., Potential Calculations in Hall Plates. In *Advances in Electronics and Electron Physics*, Peter, W. H., Ed. Academic Press: 1983; Vol. Volume 61, pp 1-62.

Chapter 3

Band-like transport in polymer semiconductors



Chapter 3

Band-like transport in polymer semiconductors

3.1 Introduction

Charge transport in organic/polymer semiconductors has many open fundamental questions. Unlike inorganic semiconductors, there has been no universally accepted model for charge transport in organic semiconductors. The general mechanisms of transport in case of semiconducting polymers is dealt in the framework of hopping between disordered-localized states[1] or in terms of mobility edge (ME) models[2]. In a typical ME model, charges occupying density of states (DOS) above the mobility edge contribute to the conductivity whereas, in the hopping mechanism all the charges with suitable energetics for hopping contribute to the conduction. Some of these concepts of charge transport have been developed from *a*-Si and are directly applicable to disordered polymer semiconductors. In this chapter, a model semiconducting-polymer system with high mobility is presented and the charge transport is discussed under the framework of these transport theories.

The classical theory of van der Waals solids[3] predict that for band-like transport to be feasible $\mu_{FET} > 1$ $cm^2V^{-1}s^{-1}$ is essential. Although, a range of polymers[4] have been demonstrated with $\mu_{FET} > 1$ $cm^2V^{-1}s^{-1}$ which is comparable to organic crystals and *a*-Si, band transport is not yet observed in these disordered systems. There have been observation of low activation magnitude and negative *T* coefficient of the μ_{FET} at high gate voltages (V_g) for solution processable films of small-molecule TIPS-pentacene. However, this trend is attributed to localized transport limited by thermal lattice fluctuations rather than extended state conduction[5]. Moreover, the observation of apparent band-like behavior in molecular systems is generally restricted to *p*-type materials[6]. This chapter discusses the results from a rationally designed *n*-type DPP-polymer system which demonstrates band-like transport and highlights the necessary prerequisites for this occurrence.

3.2 High Mobility Polymer Semiconductors

The model system discussed in this chapter is the Diketopyrrolopyrrole (DPP) D-A macromolecule referred as N-CS2DPP-OD-TEG (2DPP-TEG). This polymer has enhanced aggregation due to D-A intermolecular interactions and the order promoting ethylene glycol group. In addition, the tighter packing is expected to increase the ambient stability which makes this material a suitable candidate for fundamental studies on charge transport. It is also conceivable that semiconducting polymers based on appropriate molecular design and interfacial characteristics can provide a platform to investigate 2-D phenomena. In such systems, it may also be possible to suppress the fluctuations originating from structural disorder and traps by rationale molecular design[7]. The density of localized states can approach the mobility edge and the prevailing thermal energy can overcome the low energetic disorder leading to a diffusive band-like transport. These characteristics can manifest as a negative temperature coefficient form of $\mu_{FET}(T)$ at high T. Interestingly, there have been no examples in polymeric systems which reveal features such as low activation energies (E_A) and crossover to an inverse dependence of $\mu_{FET}(T)$ at high temperatures ($T > 250$ K).

In this chapter, 2DPP-TEG is used as an example of one such ordered system. Polymer field effect transistors (PFET) are a versatile platform for studying charge transport in a controlled manner and observe different transport mechanisms[8] from localized activated behavior to band-like weak activated behavior[6, 9]. PFETs based on 2DPP-TEG were fabricated for the transport studies in this polymer. A range of dielectric layers were utilized to introduce disorder in a controlled manner and follow the $\mu_{FET}(T)$ behavior as a function of the broadening of DOS[10]. The transport mechanism gets modified from extended state adiabatic type transport to non-adiabatic activated behavior as the dielectric constant increases. In essence, 2DPP-TEG offers a plausible macromolecular model for studying novel transport phenomena in polymeric systems.

3.3 FET Fabrication

Bottom gated top contact PFETs were fabricated by coating Al electrode (10^{-6} mbar, 1 Å/s, 30 nm thick) by shadow masking technique on standard RCA cleaned glass substrates. The dielectric layer was obtained by spin coating the solutions from their respective solvents (PVDF-HFP at 80mg/ml in N,N-Dimethylacetamide, PMMA in

propylene carbonate at 80 mg/ml and BCB in Mesitylene) at 1000 rpm for 1 minute to obtain films of thickness 0.2 - 0.4 μm. The dielectric films were annealed in N_2 atmosphere. 2DPP-TEG layer was spin coated from a solution of 10mg/ml in chlorobenzene at 1000 rpm for 1 minute to obtain films of thickness ~ 80 nm. Optimized annealing condition to obtain the best performance for this polymer was obtained as 180 °C for 2 hrs. This was followed by the deposition of Au or Al source drain electrode (10^{-6} mbar, 1 Å/s, 20 nm thick) by shadow masking technique to obtain channels of length 5 - 400 μm and width 0.5 - 1 mm. For vacuum gated devices a spacer layer of around 200 nm was introduced around the gate electrode and polymer film coated with S-D electrodes were placed on it to complete the device.

3.4 FET Characterization

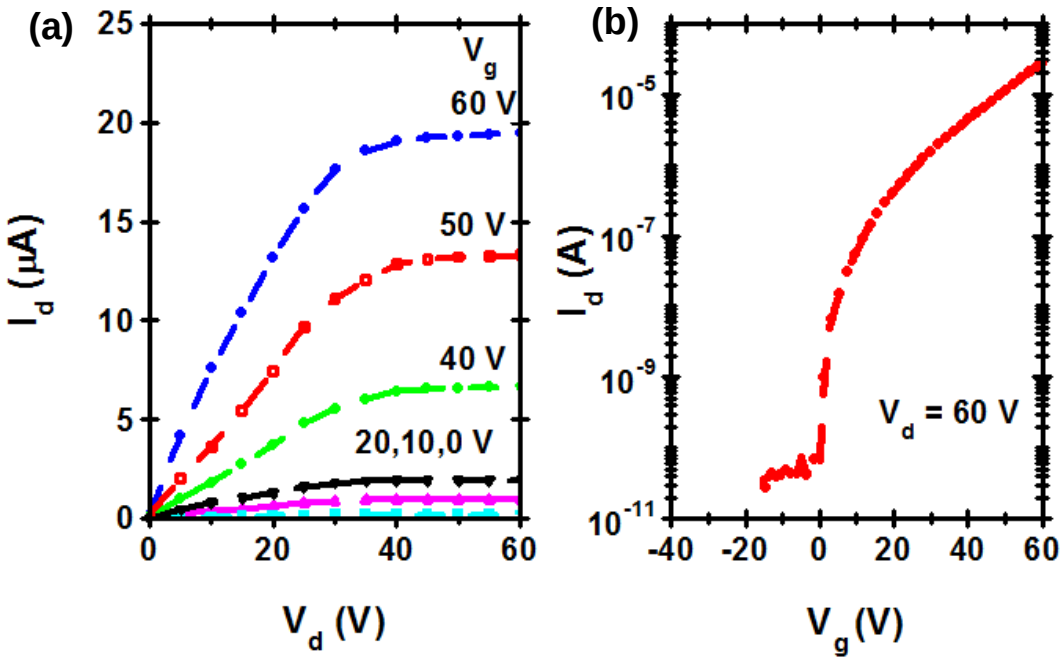


Figure 3.1: *PFET with 2DPP-TEG. Typical (a) output ($I_{ds} - V_{ds}$) and (b) transconductance ($I_{ds} - V_g$) curve for a BCB based PFET with L = 60 μm and W = 1 mm.*

DPP based bottom gate (G) top contact (S-D) FETs demonstrate distinct linear and saturation regime in $I_{ds}(V_{ds})$ profiles and minimal hysteresis in $I_{ds}(V_g)$ characteristics (**Figure: 3.1**). Devices with Al S-D electrodes and BCB dielectric layer demonstrated reliable leakage free behavior and exhibited μ^e_{FET} ~ 2.5 $cm^2V^{-1}s^{-1}$ in the saturation regime as estimated from the standard transconductance equation. Balanced ambipolar charge transport with maximum μ^e_{FET} ~ 0.46 $cm^2V^{-1}s^{-1}$ and μ^h_{FET} ~ 0.41 $cm^2V^{-1}s^{-1}$ were obtained

with Au S-D electrodes in the saturation regime. The ON-OFF ratios exhibited by these PFETs were typically in the range of 10^5 - 10^6. To understand the origin of the excellent transport properties of this polymer, *T* dependent measurements were performed for these devices.

3.4 Temperature Dependent Mobility

Measurement of μ_{FET} and σ were performed over a *T* range of 40 K – 300 K on a variety of dielectrics as shown in **Figure: 3.2a**. The dielectrics covered the category of low-*k*, high-*k* and relaxor materials. Considering the long channel length ($L \approx 60$ μm - 100 μm) used in these devices, contact resistance is negligible compared to channel resistance and does not affect the transport measurements significantly. The key findings of the *T* dependent measurements are: (i) low level of energetic disorder signified by the magnitude of activation barrier; (ii) crossover from $\frac{d\mu_{FET}}{dT} > 0$ at low *T* (40 K – 200 K) to $\frac{d\mu_{FET}}{dT} < 0$ at high *T* (> 200 K); (iii) tunability of the transport mechanism from activated to adiabatic by modulating the interface disorder and charge density.

It is instructive to examine the $\mu^e_{FET}(T)$ behavior using simple single activated fits to gauge the magnitude of the thermal barrier. Transport measurements indicate low $E_A \approx$ 16 meV (in *T* range 100 K < *T* < 220 K) for PFETs fabricated with BCB dielectric and Al S-D electrodes. As the dielectric strength *k* increases from 2.6 to 8 (for PVDF-HFP), the maximum μ^e_{FET} (in activated regime) decreases from 2.5 $cm^2V^{-1}s^{-1}$ to 1.5 $cm^2V^{-1}s^{-1}$ and E_A increases to 47 meV. A characteristic of significance in the $\mu^e_{FET}(T)$ profiles is the transition from $\frac{d\mu_{FET}}{dT} > 0$ at low *T* to $\frac{d\mu_{FET}}{dT} < 0$ at high *T*, around a crossover temperature T_{trans}. $\mu^e_{FET}(T)$ measurements indicate T_{trans} ~ 200 K for PFETs fabricated with BCB dielectric layer which increases to around 220 K for PFETs with PMMA as the dielectric layer. However, PFETs fabricated with relaxor dielectric layer PVDF-HFP do not exhibit any crossover in the entire *T* range. This behavior can be understood based on a simple argument that in order to observe a crossover to adiabatic transport in molecules, the energy bandwidth should be larger than the energy change involved in scattering which implies the minimum condition of mobility $(\mu_{min}) > \frac{er^2}{2\hbar}$, where *r* is the intermolecular distance, *e* is the electronic charge and $\hbar$ is the reduced Plank's constant[3]. In case of PVDF-HFP based PFETs, μ_{FET} is less than the required $\mu_{min} \approx 1.9$ $cm^2V^{-1}s^{-1}$ (*r* = 0.36 nm for 2DPP-TEG

obtained from GIXRD). Absence of a transport cross-over in PVDF-HFP based PFETs can then be related to the lower μ_{FET}^{e} magnitude originating from dipolar induced disorder.

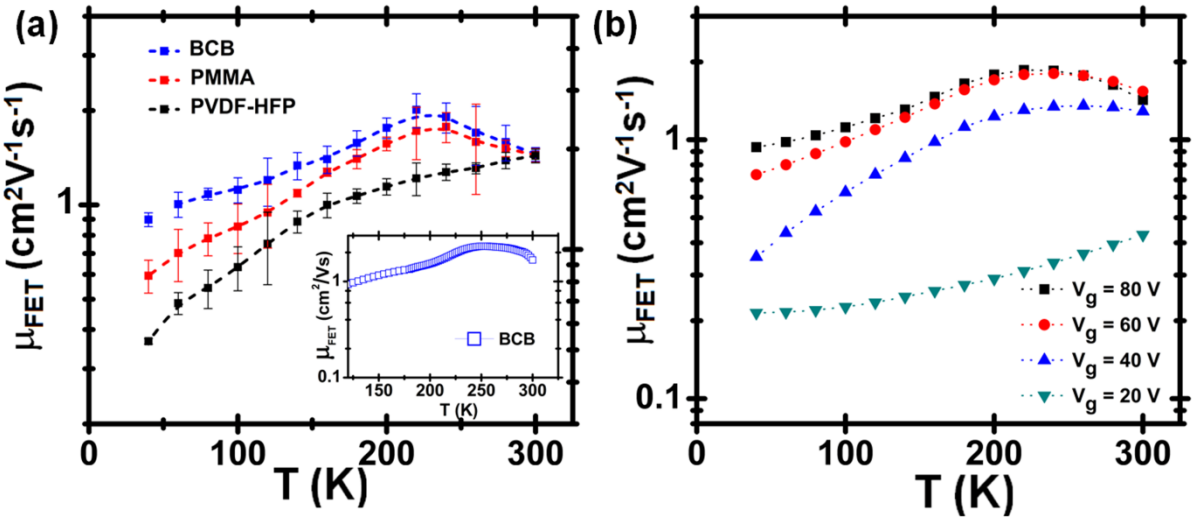


Figure 3.2: *T dependence of the PFET characteristics. (a) $\mu_{FET}(T)$ of 2DPP-TEG FETs for different dielectrics; error bars indicate the mean deviation from a set of three devices; inset depicts $\mu_{FET}(T)$ with a higher resolution (ΔT ~ 2 K) from a different batch. (b) V_g dependence of $\mu_{FET}(T)$ on a BCB based 2DPP-TEG FET.*

3.5 Origin of the deviation from Arrhenius type $\mu_{FET}(T)$

In general, a weak *T* dependent or negative coefficient of $\mu_{FET}(T)$ is observed for crystalline Si and in organic crystals like rubrene. The deviation from the typical Arrhenius type activated behavior in polymeric semiconductors is rare. In most of the cases, this trend is attributed to external factors and not observation of band-like transport. In this section all these factors are examined in the context of the $\mu_{FET}(T)$ trend observed in 2DPP-TEG to bring out the inherent nature of the transport.

3.5.1 Structural transition with T

It has also been reported that in tetracene like molecular systems negative coefficient of $\mu_{FET}(T)$ arises from a *T* induced structural re-arrangement[11] or due to bias stress in the molecule[12]. Factors relating to any structural transition are discounted in the present case based on DSC (**Figure: 3.3**) and FTIR (**Figure: 3.4**) measurements which do not indicate any structural transition or abnormal water related peaks in the entire *T* range.

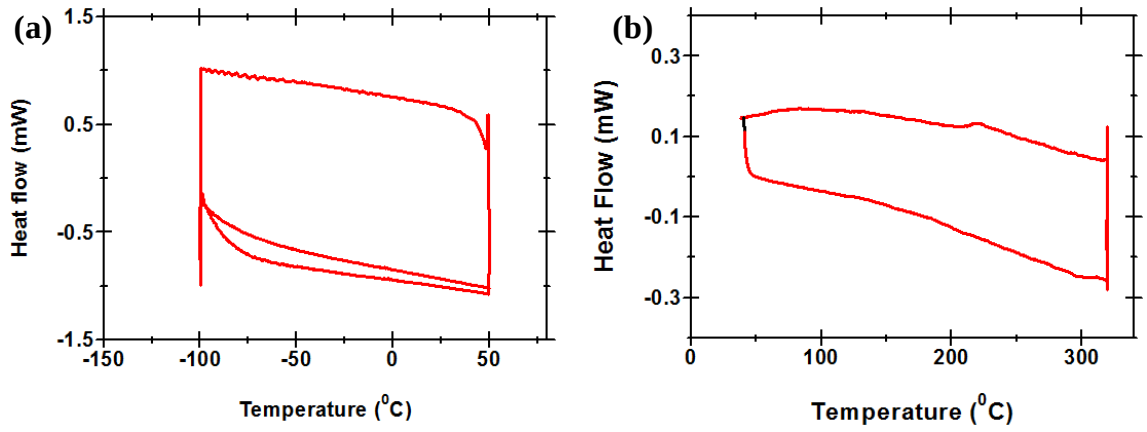


Figure 3.3: *DSC of the polymer 2DPP-TEG obtained in (a) temperature range (-100 ^{o}C - 50 ^{o}C) and (b) temperature range 40 ^{o}C - 320 ^{o}C.*

The DSC measurement indicates no phase or structural transition in the range of -100 ^{o}C to 320 ^{o}C (173 K – 600 K) indicating that the origin of T_{trans} (in the range of 200 K – 240 K) is purely because of transport mechanism variation.

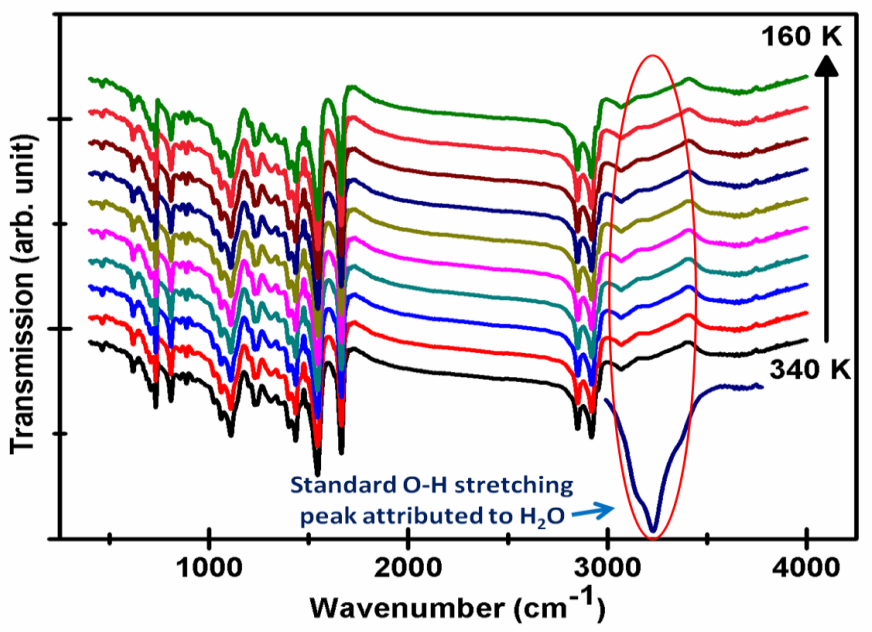


Figure 3.4: *FTIR measurement of the 2DPP-TEG in the T range of 160 K – 340 K.*

In addition FTIR measurements were also performed to map any structural variation and any absorption of water. FTIR transmission spectra of the 2DPP-TEG molecule were performed by embedding the molecule with anhydrous KBr forming a pellet. Temperature dependent FTIR transmission spectra was obtained in the temperature range of 160 K to

340 K with a ΔT = 20 K using BRUKER IFS 66v/S. All the measurements were performed under vacuum (10^{-3} mbar). The FTIR spectra do not exhibit any structural transition in the complete T range. In general, the existence of absorbed/adsorbed water on the molecular surface is attributed to the simultaneous presence of ~3350 cm^{-1} of O-H stretching and 1600 cm^{-1} (scissoring frequency of water). In the present case no peak is observe at 3350 cm^{-1}. Even though there is a transmission peak at 1600 cm^{-1} in each spectra, the absence of strong O-H stretching peak rules out the presence of water in the sample[13]. Also the peak around 1600 cm^{-1} is invariant with T which indicates that the peak is attributed to the sample itself.

3.5.2 Bias stress

The negative coefficient in the $\mu_{FET}(T)$ can also originate due to bias stress in PFETs[12]. Hence, PFET measurements were performed over a time scale of 10^4 s.

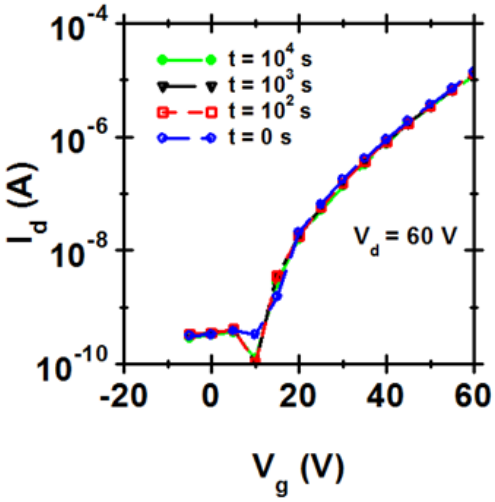


Figure 3.5: *Typical time variation of the transconductance measurement obtained for a PFET (L = 100 μm, W = 1mm) with BCB dielectric layer and 2DPP-TEG active layer.*

The device was continuously biased at V_d = 60 V and V_g = 60 V and the transconductance sweep was performed at regular intervals. The transconductance plots as shown in **Figure: 3.5** do not indicate any significant change till a time period of 10^4 s.

3.5.3 Super-Cooled water related trapping

The observation of negative coefficient in the $\mu_{FET}(T)$ measurements can also originate from water related traps at the interface[14]. Super-cooled H_2O at the dielectric-semiconductor interface introduces traps which modifies the trends in the transport. In the present case, this possible reasoning of water as a source for interpreting the observations is absolutely not possible. The following sets of evidences prove this point:

(a) The procedure of measurement involved loading the samples on a probe station in a cryogenic vacuum assembly. The samples were heated to T ~ 373 K in high vacuum (~ 10^{-4} - 10^{-5} mbar) for a sufficiently long period (20 - 30 minutes) eliminating any possible sources of water in the sample and the chamber.

(b) Any form of *T*-dependent measurements (conductivity, TGA, DSC, FTIR) does not show storage of water molecules. To prove that the absorption of water molecule is negligible TGA (270 K – 700 K), DSC (200 K – 600 K) and FTIR (160 K- 240 K) measurements were performed (**reference [4a] and Section 3.5.1**). TGA measurement does not demonstrate any weight loss for a T ~ 600 K and DSC measurements do not show any abnormal peaks relating to water absorption on the molecule. In addition, FTIR also does not show water related absorption peaks in the complete *T* range of 160 K – 340 K.

(c) Electrochemically, water and oxygen create traps due to the formation of an oxidized polymer anion by the reaction[15]:

$$O_2 + 2H_2O + a\,Pol^- \rightleftharpoons a\,Pol + OH^-$$

The reduction potential for half-cell involving water is ≈ - 3.6 eV. Electron trap levels in polymer due to water is generally observed at energy levels of -3.6 eV[16]. Hence molecules with LUMO level deeper than -3.6 eV are stable to water related trapping [15] which is indeed the case with 2DPP-TEG[4a]. The over-potential at the LUMO of 2DPP-TEG makes the process energetically unfavorable. Additionally, degradation of organic molecules can also arise due to percolation of water molecules inside the polymer chain. This can be avoided by molecular design which enables tighter packing and prevents the percolation of water molecule [15, 17]. From the molecular point of view, the amphiphillic substitution in 2DPP-TEG provides stronger aggregates (strong π-π stacking established by GIXRD experiments[18]), hence the role of water molecule affecting the charge transport is minimal.

(d) The hydrophillicity of the polymer surface was probed and the water contact angle was measured to be ($110^0 \pm 7^0$) proving the hydrophobic nature of the polymer surface.

(e) A sizable number of devices (> 100) were measured. The characteristics of the devices does not depend on the history of the devices (storage-exposure-cooling-heating), clearly pointing out the absence of effects from residual moisture.

(f) It should also be noted that the reports indicating super-cooled water effects generally reveal changes in slope for $I_{ds}(T)$ or $\mu_{FET}(T)$ on a smaller *T* range [19] beyond which the activated behavior is revived. However, the $\mu_{FET}(T)$ trend in 2DPP-TEG shows variation in

slope which continues till a T range of 300 K, much above the super-cooled phase transition temperature.

(g) Magnitude of the T_{trans} is dependent on the gate voltage V_g. If charge trapping due to super-cooled water is responsible for the negative coefficient of mobility, then the features should be more pronounced at low V_g, as opposed to what is observed in the present case (**Figure: 3.2b**).

(h) The $\mu_{FET}(T)$ trends of 2DPP-TEG indicates that the transition temperature (T_{trans}) can be tuned with the dielectric layer on which the polymer layer is coated (**Figure: 3.2a**). It was observed that with increase in polarity of the dielectric layer T_{trans} increases to higher value which results in the suppressing the band-like features (as shown in **Figure: 3.2a**). This trend seen in FETs fabricated with PVDF-HFP dielectric layer can be directly attributed to the interface traps introduced with polar dielectrics and not existence of water related traps.

Detailed measurements were also performed to point out that the intrinsic nature of transport is controlled by the structure of semiconducting polymer and the interfacial energetics. Each of the aspects of transport was verified by tweaking the molecular structure and the dielectric layer respectively. For example: Range of measurements performed on 2DPP-2Dod (the polymer analog without the order promoting ethylene glycol substitution) demonstrate mobility magnitude of 10^{-3} $cm^2V^{-1}s^{-1}$ and the $\mu_{FET}(T)$ behavior does not exhibit the crossover. The E_A obtained from $\mu_{FET}(T)$ of 2DPP-2Dod was significantly high and is ≈ 100-150 meV. It should be noted that the possible source of water from the dielectric component was also completely eliminated by combination of thermal and vacuum treatments. Contact angle measurements were also performed on dielectric surfaces which points to a hydrophobic surface with minimal water.

3.5.4 Field Emission/Luttinger-Liquid type transport

Reported observations of temperature independent behavior in polymers/organic molecule have been attributed to factors like: (i) field induced crossover in conductivity[20] or (ii) Luttinger liquid type 1-D metallic conductivity[21]. In the present case, the FET output characteristics demonstrated well defined linear and saturation regime without any non-linear transport behavior even at $T \approx 40$ K. This indicates that the transport is relatively independent of the lateral field unlike other high mobility polymers where lateral field causes de-trapping of carriers from shallow traps. Hence, the possibility of field induced cross-over from activated to field emission can be neglected in the present case. In addition,

a clear Hall effect (described in section 3.10) as well as interconnected network of self-assembled polymeric structures (**Figure: 3.6**) supports a 2-D microstructure for transport and does not indicate a Luttinger-liquid type mechanism in this system.

These set of observations provide clear evidence that $\mu_{FET}(T)$ trends originate from the inherent transport mechanisms and not from artifacts due to external factors.

3.6 2D transport

At a molecular level, the self-assembled interconnected structure was treated as the basis for 2-D transport in 2DPP-TEG polymer based PFETs. These features are preserved for films of thickness 50 nm to 1 μm. Additionally, both top and bottom gated PFETs demonstrated similar μ_{FET} indicating similar morphology throughout the film thickness.

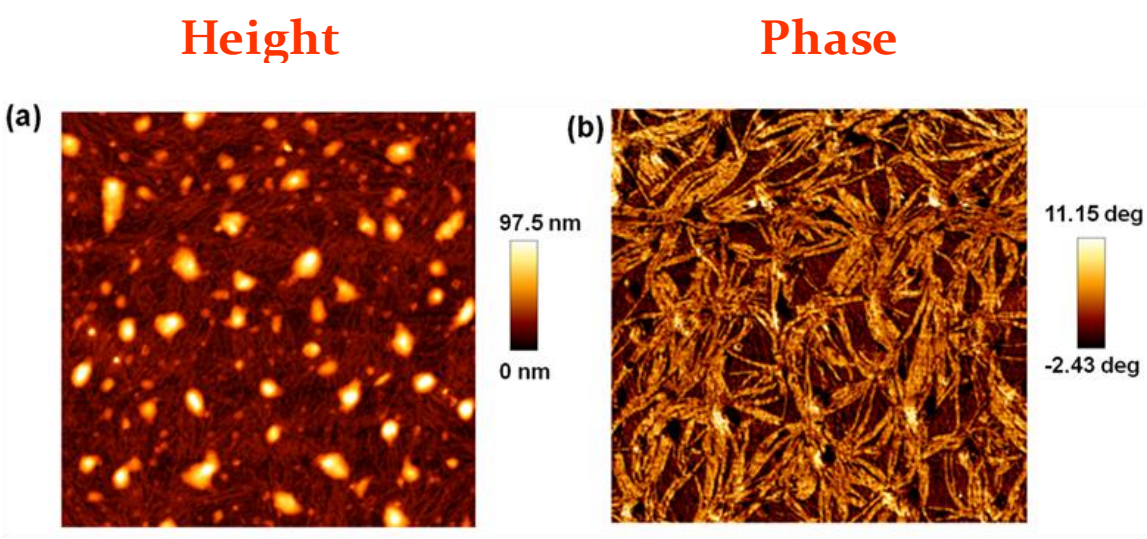


Figure 3.6: *Morphology of the polymer films. (a) AFM topography and (b) phase-contrast image (10 μm × 10 μm) of the polymer film indicating self-assembled interconnected network of aggregates.*

A phenomenological justification of 2-D transport can also be obtained from the analysis of the transconductance curve. In order to numerically prove 2-D transport following analysis was performed:

$I_d^{2D} = A\ \frac{W}{L}\ d_{sc}^{1-\frac{T_o}{T}}\ (\frac{C_i}{e})^{\frac{T_0}{T}}\ \frac{T}{T_o+T}\ (V_g - V_t)^{\frac{T_o}{T}+1}$ for 2-D transport close to the interface and

$I_d^{3D} = A\ \frac{W}{eL}\ d_{sc}^{1-\frac{T_o}{T}}\ (\frac{1}{2kT\epsilon\varepsilon_o})C_i^{\frac{2T_0}{T}-1}(\frac{T}{2T_o-T})(\frac{T}{2T_o})(V_g - V_t)^{\frac{2T_o}{T}}$ for 3-D transport

where, T_0 is the characteristic width of the exponential DOS, W is the channel width, L is the channel length, d_{sc} is the semiconductor thickness of constant carrier density, C_i is the capacitance per unit area, e is electronic charge and A is related to carrier delocalization length and conductivity of the material[22]. In the saturation regime, both the 2-D and 3-D based model lead to direct power-laws:

$I_d^{2D} \propto (V_g - V_t)^{\alpha}$ where, $\alpha = \frac{T_0}{T} + 1$ for 2-D transport and $\alpha = \frac{2T_0}{T}$ for 3D transport.

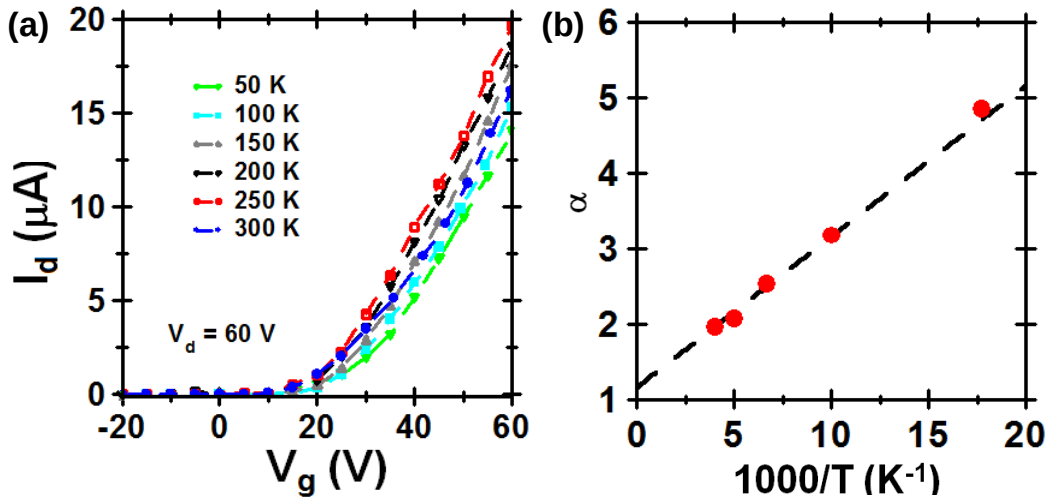


Figure 3.7: *(a) Representative transfer characteristics of a 2DPP-TEG based FET ($L \approx 100$ μm, $W \approx 1$ mm) as a function of temperature. (b) Extracted values of α plotted versus 1/T. The extrapolated linear fit yields the intercept with the vertical axis.*

As evident from the plots of α versus *1/T* in the activated regime, the transport close to the interface is 2-D (**Figure: 3.7**). Furthermore the observation of a finite Hall voltage supports the claim that the transport phenomenon is governed by the 2-D interconnected network[21].

3.7 Gate Induced charges

To understand the role of gate induced carrier density (n_G) on the order-disorder transition, $\mu_{FET}^{e}(T)$ was measured at different V_g (**Figure: 3.2b**). At low V_g (≤ 20 V), the transport crossover is not observed and at higher V_g (≥ 40 V), T_{trans} gets prominent indicating the crossover. In the framework of ME, charge transport involves thermal excitation to states at or below the transport level (E_t). As the states above E_t are filled up with increase in n_G the quasi-Fermi level is lowered and E_A decreases[23]. This trend is consistent with the observed crossover in transport mechanism at $V_g \geq 40$ V. Similarly, at

low V_g (≤ 20 V) μ_{FET} is dependent on V_g and for $V_g \geq 40$ V, the μ_{FET} (at 300 K) varies in the range of 1.4 ± 0.1 $cm^2V^{-1}s^{-1}$ for a V_g change from 40 V to 80 V indicating a weaker V_g dependence of μ_{FET}. This corroborates with the weak E_A and low energetic disorder for charge transport in the PFETs fabricated with BCB dielectrics. In the case of PFETs fabricated with PVDF-HFP dielectric layer no crossover is observed in the $\mu_{FET}^{e}(T)$ trends even at $n_G \sim 4 \times 10^{19}$ cm^{-3} which can be attributed to high interface disorder ($E_A \sim 47$ meV). The importance of the dielectric-semiconductor interface and the annealing effects become apparent upon comparison with vacuum-gated devices. Vacuum-gated devices show relatively low μ_{FET} of $10^{-3}cm^2V^{-1}s^{-1}$ and higher $E_A \sim 150$ meV indicating the presence of large number of electron-traps at the interface. These performance parameters are comparable to other vacuum gated polymeric devices[23] and can be related to the presence of un-passivated surface trap states in these structures. Thus, extended transport in polymeric materials requires a combination of an ordered interface as well as significant amount of n_G to passivate the traps.

3.8 Dielectric-Semiconductor interface

The observed dependence of μ_{FET}^{e} on different dielectric layers (**Figure: 3.2a**) can originate from the dipolar disorder or due to the variation of the interfacial width [24]. Interfacial width variation is defined as the intermixing of the interface boundaries due to dissolution of one solution processable layer by the coating of another solution processable layer on the top. To understand the contribution from interfacial width, high resolution AFM was utilized for measuring the roughness of the dielectric layers before and after the solvent treatment. Chlorobenzene which is used for dissolving the polymer was used for the solvent treatment of the dielectric layer. AFM profiles shown in **Figure: 3.8** do not exhibit significant increase in surface roughness of the dielectric layer with solvent treatment, indicating minimal effect of interface de-mixing on the field effect transport. On this basis, the $\mu_{FET}^{e}(k)$ behavior can be attributed to static dipolar disorder of the dielectric layer. The magnitude of dielectric induced disorder (E_p) is estimated from the expression: $E_A \sim \sqrt{E_{sc}^2 + E_p^2}$, where E_{sc} is the activation in the low-*k* BCB dielectric layer based PFET which is assumed to have negligible E_p[25]. The dipolar induced broadening in the DOS of 2DPP-TEG originating from the dielectric layers PMMA and PVDF-HFP is ≈ 26.5 meV

and 44.3 meV respectively which is considerably lower than the estimates obtained for amorphous polymers like PTAA[10a].

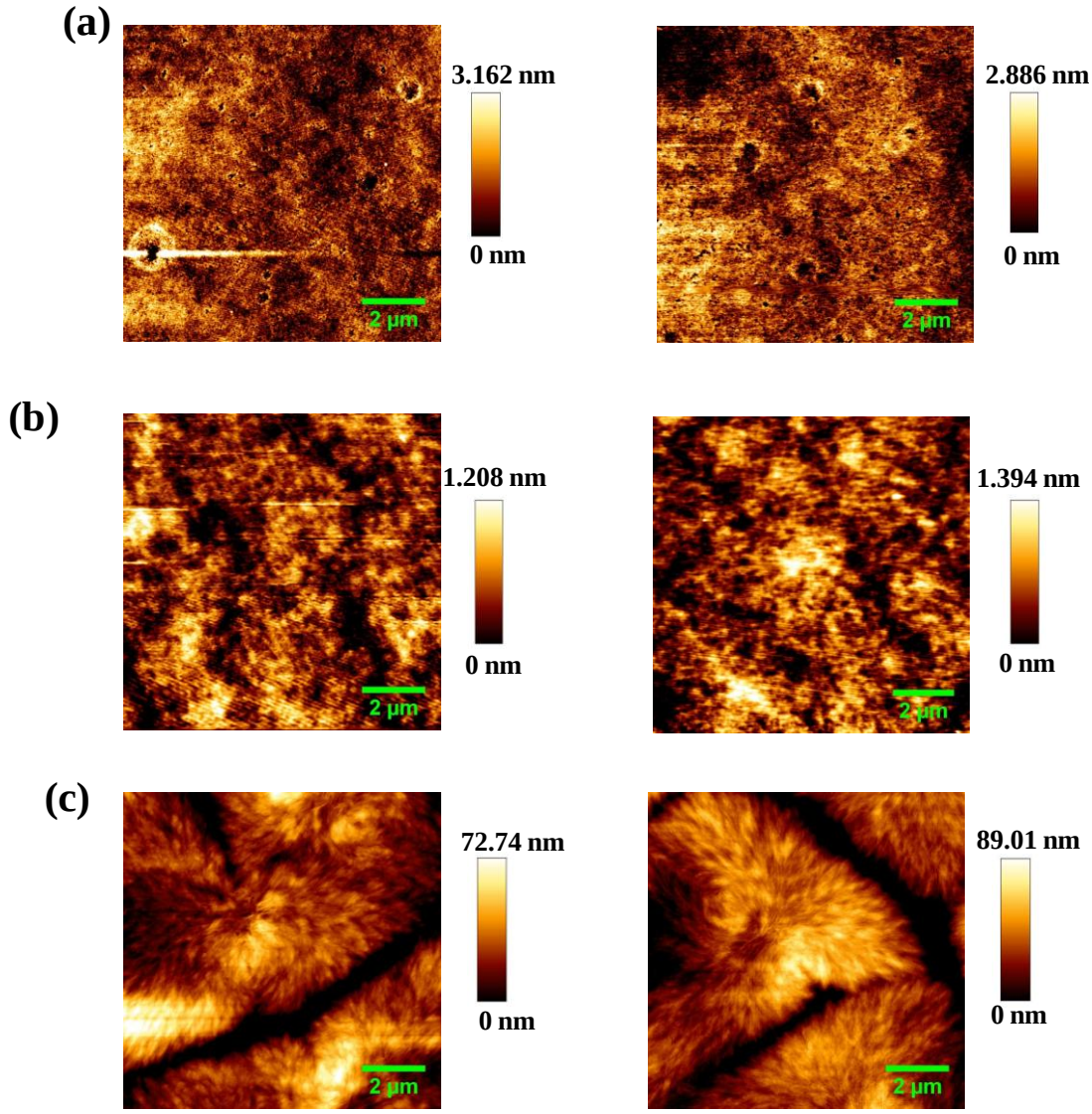


Figure 3.8: *AFM morphology of the dielectric layers: (a) BCB (b) PMMA (c) PVDF-HFP before (left) and after (right) solvent treatment.*

Table 1: *Roughness parameters obtained from AFM of the dielectric films.*

Dielectric	Treatment	Average roughness (nm)	r.m.s roughness (nm)
BCB	Before	0.52	0.71
	After	0.51	0.65
PMMA	Before	0.25	0.31
	After	0.23	0.28
PVDF-HFP	Before	12.05	16.53
	After	15.48	20.23

To understand, this observation DPP-TEG thin films were evaluated using grazing-incidence X-ray diffraction (GIXRD). The GIXRD scattering pattern of 2DPP-TEG is shown in **Figure: 3.9**. As evident from the GIXRD pattern, the polymer adopts a common lamellar structure and edge-on packing with a coherence length of 9.1 nm. The π-π stacking (010) peak has an associated *d* spacing of 0.36 nm and a coherence length of 3.4 nm. GIXRD spectra indicate edge-on stacking of the semiconducting core on the dielectric layer. Low magnitude of dipolar-broadening contribution can then be related to electrostatic isolation of the polymer conjugated core from the dielectric surface because of the edge-on stacking of the polymer (inset **Figure: 3.9)**. Nevertheless, this low but finite dielectric disorder appears to be critical in deciding the eventual $\mu_{FET}^{e}(T)$ behavior.

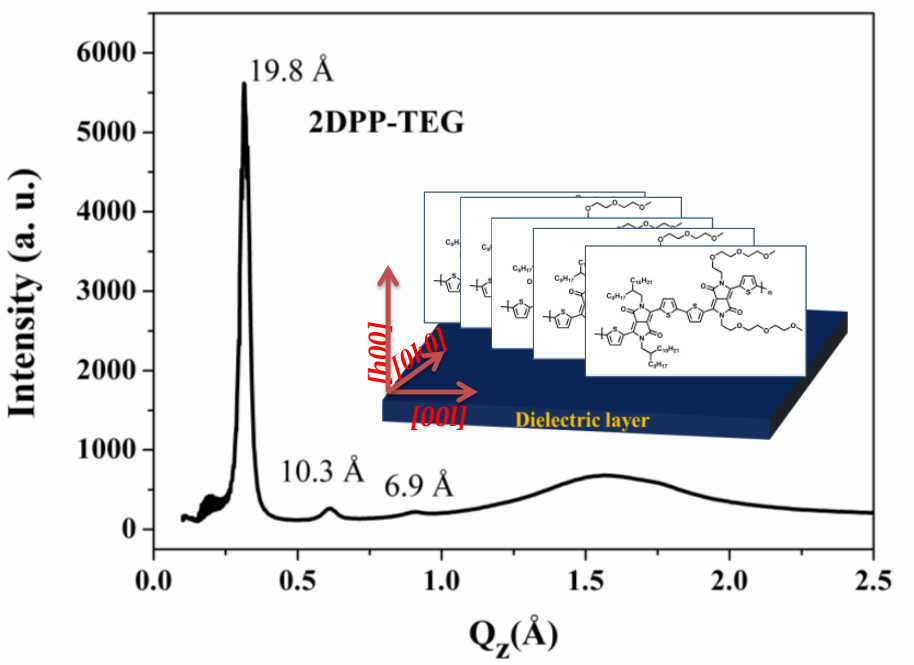


Figure 3.9: *GIXRD pattern for 2DPP-TEG thin films, exhibiting prominent peaks corresponding to (100) and π-π stacking. Inset shows the schematic for edge-on stacking of 2DPP-TEG on the dielectric layer.*

3.9 Molecular Origin of low Disorder

At a microscopic level, the origin of high μ_{FET} and weak disorder in 2DPP-TEG can be understood from the molecular and structural design. Quantum chemical calculations were carried out using density functional theory (DFT) with the B3LYP hybrid functional and 6-31G** basis set. The energy optimized structure demonstrated electron transfer Marcus re-organization energy (λ_e) of 0.11 eV and a torsional disorder of ≈ 2° from a perfectly co-planar conjugated core. Despite the limited number of oligomers (5) considered and neglecting the polarization effect introduced by the dielectric media, λ_e values are qualitatively consistent with the experimentally observed E_A. From the semi-classical Marcus theory the activation energy for the self-exchange charge-transfer reaction is given by $\lambda_e/4$[26]. The contribution of E_A is generally overwhelmed by the inherent disorder of polymeric systems. Interestingly, in this system, $\lambda_e/4$ (25.5 meV) ≈ E_A (16 meV) which indicates that the activation energy required for de-trapping of charge carriers originate from conformational changes. This observation is consistent with observed high mobility values and low degree of disorder for charge transport. In addition, 2DPP-TEG

demonstrates high degree of crystallinity and enhanced π-π stacking due to stronger aggregation which originates from amphiphillic design of the molecule[27]. Analysis of the morphology by high resolution AFM (section 3.7) showed an interconnected network of self-assembled structures (**Figure: 3.7**) making the transport more tolerant to disorder. This is consistent with the observation of low E_A (~ 16 meV) in the temperature dependent transport. In order to analyze the role of π-π stacking and the triethylene glycol (TEG) substitution, PFETs were fabricated under similar condition with a control polymer 2DPP-2Dod. In the case of 2DPP-2Dod where the amphiphillic interactions are absent, the interconnected self-assembled structures were not present . It was noted that this analogue of DPP without the order-promoting TEG group demonstrated μ^e_{FET} ~ 10^{-3} $cm^2V^{-1}s^{-1}$ and $E_A \approx 100$ meV in the regime < 280 K without any presence of crossover *T*. Hence, presence of strong aggregation due to efficient π-π stacking, interconnected network of ordered regions which provide efficient pathway for transport within the disordered regions and co-planarity of the conjugated core are possibly the reasons for 2DPP-TEG to be more tolerant to disorder.

3.10 Band-like transport in 2DPP-TEG

The ME framework offers a scenario where the cross-over in transport is a continuous transition, unlike the hopping based models where crossover is accompanied by a discontinuity in transport parameters[28]. Evidence such as $E_A \approx k_B T_{trans}$ offer a simple argument supporting ME based processes. In order to obtain the DOS profiles, $\mu^e_{FET}(V_g)$ was measured and analyzed. It was observed that μ^e_{FET} increases rapidly at low V_g (> 40 V) as the states are quickly filled up and at high V_g (≥ 40 V), μ^e_{FET} becomes independent of the induced charges at the interface corroborating the existence of exponential-type DOS (**Figure: 3.10**). The magnitude of E_A and the nature of the DOS indicates that the trap levels are close to the band edge which explains the origin of diffusive transport due to de-trapping of charge carriers by thermal fluctuations[7]. The effective mobility, μ_{FET} is expressed as $\mu_0 \frac{\tau}{\tau + \tau_{tr}}$, where τ is the average time the carrier spends travelling between shallow traps, τ_{tr} is the lifetime of shallow traps and μ_o is the trap free mobility. If $\tau << \tau_{tr}$,the transport is trap limited with activation energy as obtained from Arrhenius fit. However in the regime $\tau >> \tau_{tr}$ which corresponds to the extended transport regime close to the mobility edge, $\mu_{FET} \sim \mu_0 T^{-\gamma}$ with γ ~ 0.9 - 1.4 (**Table 2**) [29]. The magnitude of γ is reflective

of the prevailing scattering contributions, which in the present molecule is relatively lower than other organic molecules like rubrene and pentacene[30].

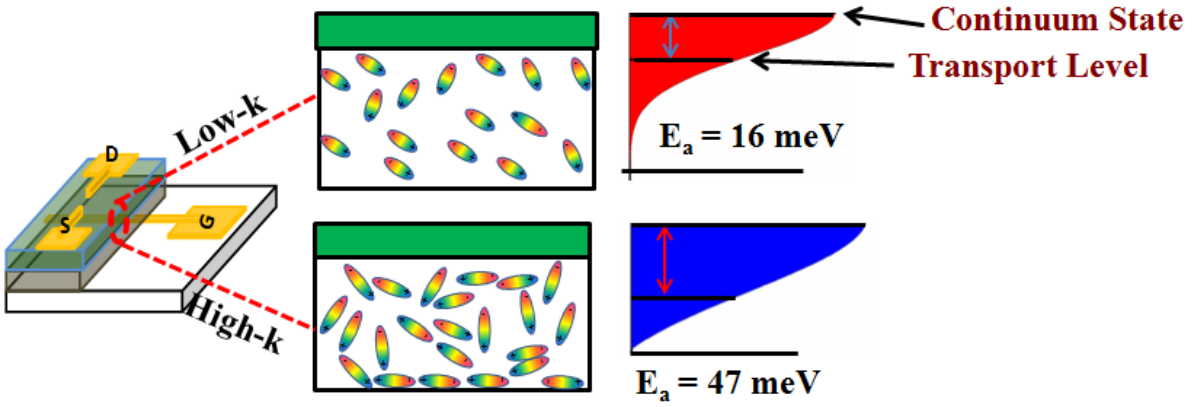


Figure 3.10: *Schematic of the device and the DOS for 2DPP-TEG polymer semiconductors in the presence of low-k and high-k dielectrics.*

3.11 Hall Voltage measurement in 2DPP-TEG

In the band-like transport regime, ($T > T_{trans}$) to confirm the presence of completely delocalized trap free carriers, Hall voltage (V_H) measurements were performed. V_H signatures in a PFET is a sensitive probe to measure the degree of delocalized adiabatic transport, since it requires the charges to be mesoscopically extended to have a well-defined wave vector which can couple with the magnetic field[29-30]. Observation of clear V_H in PFETs have been challenging due to low $\mu_{FET,}$ high contact resistance and threshold voltage instabilities, moreover obtaining clear negative T dependence is relatively rare in such disordered materials. Bottom gated top contact PFETs were fabricated using transparent patterned ITO (15 ohm/□, obtained from XINYAN Technology Ltd.) as the gate. Transparent gate electrodes were chosen to ease the patterning of the electrodes. BCB dielectric layer was then spin coated at 1000 rpm for 1 minute to obtain films of thickness 0.4 μm. The dielectric films were annealed in N_2 atmosphere. Patterned semiconducting layer was introduced using lithographic and printed techniques to accommodate only the S-D electrodes and the Hall probes. The patterning of the semiconducting layer minimizes spurious voltage signal being picked up by the Hall probes. This was followed by the deposition of Al source drain electrode (10^{-6} mbar, 1 Å/s, 20 nm thick) by shadow masking technique to obtain channels of length 200 - 400 μm and width 200 – 500 μm. Al electrodes transverse to the channel were coated (10^{-6} mbar, 1 Å/s, 20 nm thick) to serve as the Hall

probes using physical masking technique by aligning under a microscope. Typical width of the Hall probes (W^*) were maintained at 40 – 80 μm and the distance between the Hall probes (L^*) were varied in the range of 100 μm – 1 mm (as shown in top inset **Figure: 3.11a**). This device geometry is similar to the Hall probe assembly used for a-Si and rubrene[31].

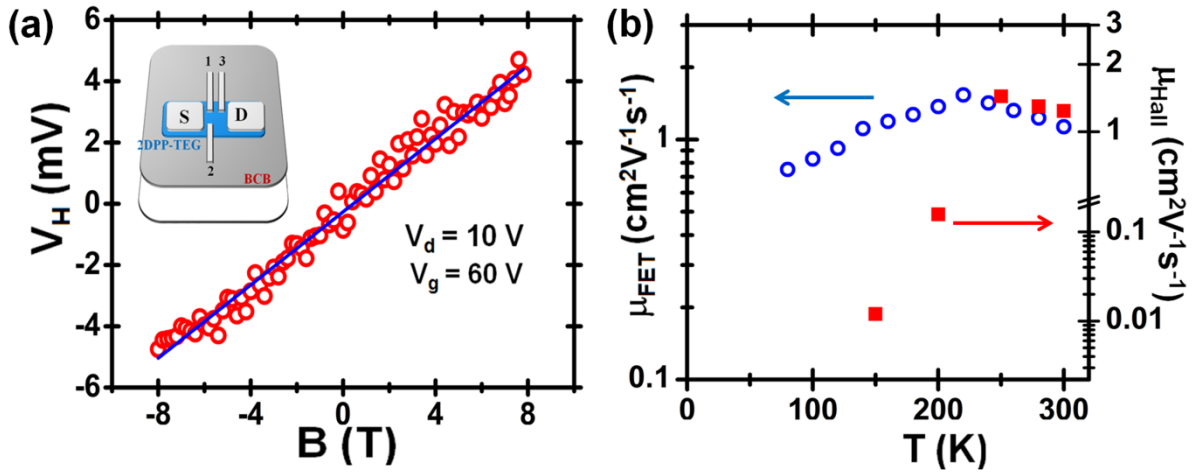


Figure 3.11: *Hall voltage measurements for 2DPP-TEG in PFET geometry (L = 200 μm and W = 200 μm, W* = 40 μm and BCB dielectric). (a) Plot of V_H with B (Top inset shows the schematic of the patterned Hall device geometry, patterned gate not shown, electrodes 1 and 2 represent the Hall probes and electrode 3 is for four probe conductivity measurement); (b) comparative plot of μ_{FET} (blue markers) and μ_{Hall} (red markers) at different T.*

V_H signal was observed in devices at 300 K with BCB dielectric layer and Al S-D electrodes for $|V_g|$ > 60 V. Geometrical correction factors were introduced wherever required to obtain accurate estimation of V_H. The observation of V_H signal is consistent with the $\mu_{FET}(V_g)$ trend, wherein at high V_g the transport is trap-free and independent of induced charge density. Experimental artifacts were minimized by measuring V_H as a function of (***B***) over a wide range (0 T to 8 T) as shown in **Figure: 3.11a**, and subsequently verifying the trend by reversing the magnetic field direction and changing the polarity of I_{ds}. A complete cycle of V_H with ***B*** is provided in **Figure: 3.12**.

The trap free charge density extracted from the slope of V_H variation with ***B*** ($n_H = I_{ds}\boldsymbol{B}/eV_H \approx 1.4 \times 10^{12}$ cm^{-2}) is in good agreement with the surface charge density obtained from gate capacitance measurements ($n_{FET} = C_i\,(V_g - V_{th})/e \approx 1.6 \times 10^{12}$ cm^{-2}) indicating extended state transport. Remarkably, the magnitude of μ_{Hall} was comparable to μ_{FET}^{e} in the adiabatic transport regime ($T > T_{trans}$) and falls steeply in the non-adiabatic activated

transport regime ($T < T_{trans}$). The magnitude of V_H increases with V_g which is consistent with the observed trends of $\mu_{FET}(V_g)$. Ratio of n_H/n_{FET} can be a measure of the fraction of delocalized charge carriers, this ratio increases with increase in T (in band-like transport regime) and assumes a value of unity at $T \sim 300$ K. A smaller magnitude of V_H with $n_H << n_{FET}$ was observed at low T ($< T_{trans}$) of 200 K corresponding to the low T hopping regime where quantum mechanical interference among different hopping processes can contribute[31a]. The key aspect is the equivalence of intrinsic trap-free μ_{Hall} and μ_{FET} at high T in 2DPP-TEG system bringing out the general consistency of band-like transport.

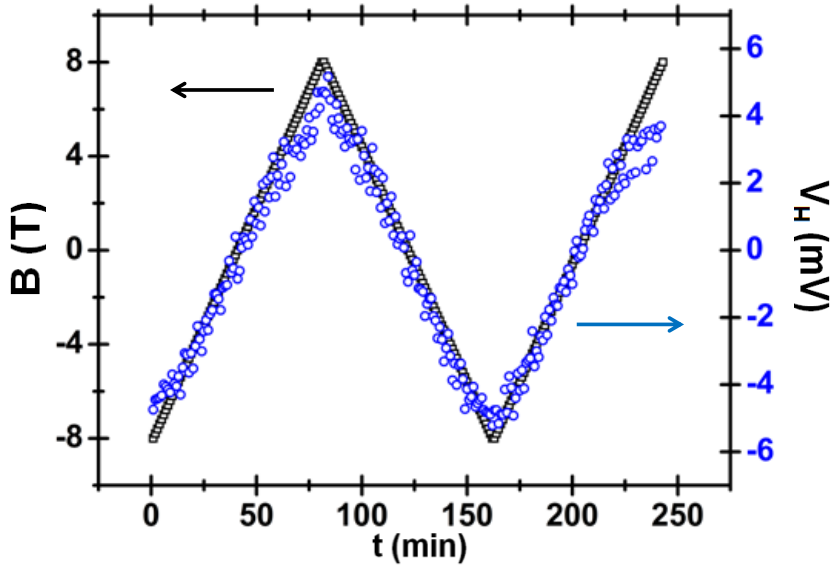


Figure 3.12: *Plot of V_H with **B** for 2DPP-TEG in a PFET geometry (L = 200 μm and W = 200 μm, W* = 40 μm and BCB dielectric) measured over multiple cycles of B variation.*

3.12 Bulk transport in 2DPP-TEG

Detailed picture of the bulk disorder is essential to completely understand the origin of extended state conduction in 2DPP-TEG. Further studies were carried out to determine the bulk properties from space-charge limited (SCL) measurements. Devices were fabricated on pre-cleaned ITO substrates (15 ohm/□), obtained from XINYAN Technology Ltd. For hole only devices (ITO/PEDOT:PSS/Polymer/Au), PEDOT:PSS was spin coated at 2000 rpm and annealed at 110 °C for 1 hour in air. Polymer films of varying thickness (200 nm to 2 μm) were obtained and annealed at 180 °C for 2 hours in N_2 atmosphere.

Similarly electron only devices were fabricated on Al coated pre-cleaned glass substrates on which polymer layer is coated followed by Al cathode electrode. Metal electrodes were coated by thermal evaporation (10^{-6} mbar, 1 Å/s, 60 nm thick). Current density as high as 10^3 A/m^2 is typically obtained for films of thickness 0.5 μm with a low bias ~ 10 V. Clear and distinctive linear and SCL regimes were obtained for both *p*-type and *n*-type transport as seen in the **Figure: 3.13**. The bulk mobility (μ_{SCL}) was obtained using the Mott-Gurney equation given by: $J_{SCL} = \frac{9}{8}\varepsilon_0 k_S \mu_{SCL} \frac{V^2}{d^3}$, where J_{SCL} is the current density of the device in the SCL regime, k_s (≈ 3 - 4) is the relative permittivity of the semiconductor, *d* is the thickness of the active semiconducting layer and *V* is the bias applied. Typical μ_{SCL} magnitude of (9 ± 5) × 10^{-3} cm^{2}V^{-1}s^{-1} was obtained with electron only devices and μ_{SCL} of (6 ± 2) × 10^{-3} cm^{2}V^{-1}s^{-1} was obtained with hole only devices. Bulk activation was obtained from the *T* dependent transport measurements performed in the *T* range of 100 K – 300 K. The presence of a clear SCL regime at low *T* points to the absence of any deep-trap dominated non-linear processes in the bulk transport. Activation energy from the SCL (E_A^{SCL}) measurements were 60 ± 5 meV for *n*-type transport which is comparable to reported high mobility *n*-type polymers[32]. However, *p*-type devices indicate a stronger activation in $\mu_{SCL}(T)$ with E_A^{SCL} ~ 135 ± 12 meV.

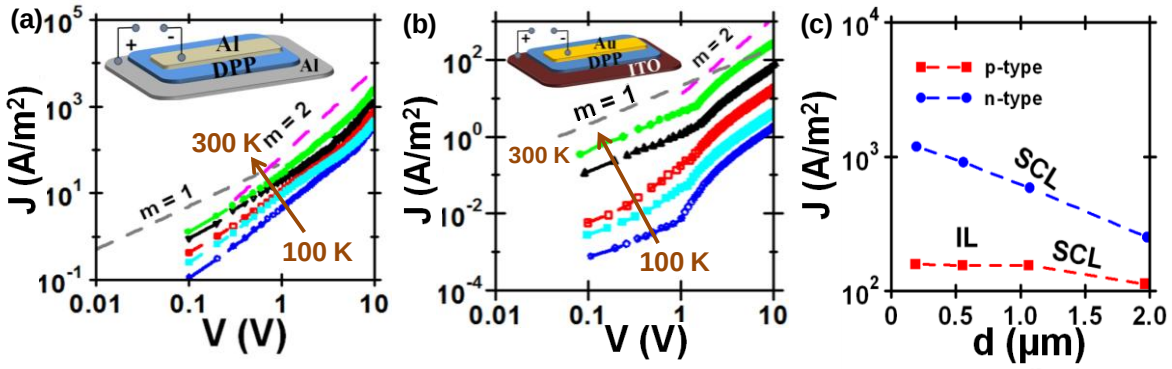


***Figure 3.13**: Bulk characterization of 2DPP-TEG. T dependent SCL transport measured for (a) electron-only device (d ~ 500 nm); (b) hole-only device (d ~ 2 μm). Inset shows the schematic of the devices. (c) Plot of J (E = 5 V/μm) with thickness for both p-type and n-type transport showing injection limited (IL) and space charge limited (SCL) behavior.*

Devices were also fabricated with the polymer layer thickness varying from 0.2 μm - 2 μm to understand the limiting factors in the bulk transport. In the SCL regime it is

expected that current density scales as $J(E) \propto d^{-1}$ whereas, if the current is injection limited(IL), $J(E)$ is independent of the semiconductor thickness[32]. In the case of *n*-type diodes, $J(E)$ has a linear variation with $1/d$ indicating SCL transport. Interestingly, for *p*-type diodes $J(E)$ is independent of film thickness in the range of 0.2 μm to 1 μm and has a linear dependence for films of thickness > 1 μm, indicating a crossover from IL behavior to SCL behavior with increase in active layer thickness. Bulk transport measurements demonstrate the underlying difference in the hole and electron transport in this polymer which is consistent with the trends in field effect transport.

3.13 Ambipolar Transport and Logic devices

DPP based polymers support ambipolar transport with Au S-D electrode. However, the presence of an injection barrier in the hole transport provides an independent handle on the ambipolarity of the FET by controlling the dielectric interface. **Figure: 3.14a** show the change in ambipolar transport with different dielectric materials in PFETs. The degree of ambipolarity ($D = \mu_{FET}^{h}/\mu_{FET}^{e}$) changes from ≈ 0.5 for BCB based devices to ≈ 0.92 for PVDF-HFP dielectric devices. This can be correlated to the presence of polar C-F groups at the interface in PVDF-HFP based PFETs which suitably alters the transport levels[33] to favor a balanced ambipolar transport (as shown in inset **Figure: 3.14a)**. This interpretation is consistent with a |5 V| decrease in threshold voltage for hole transport when PVDF-HFP is used as the dielectric layer compared to low-*k* BCB based PFETs[34].

Table 2: *Summary of the transport properties of the polymer with different dielectrics fitted by a simple ME model.*

k	μ_{FET} ($cm^2V^{-1}s^{-1}$) at T_{trans}	μ_{FET} ($cm^2V^{-1}s^{-1}$) at 300 K	E_A (meV)	γ	D
2.6	2.01	1.47	16	1.01	0.5
3.6	1.72	1.42	31	0.94	0.78
8	-	1.33	47	-	0.92

This element of control on the charge transport by modifying the dielectric layer is utilized to obtain high-performance and balanced ambipolar circuits. All-polymer complementary inverters were fabricated with this high performance polymer to demonstrate the usability in logic circuits.

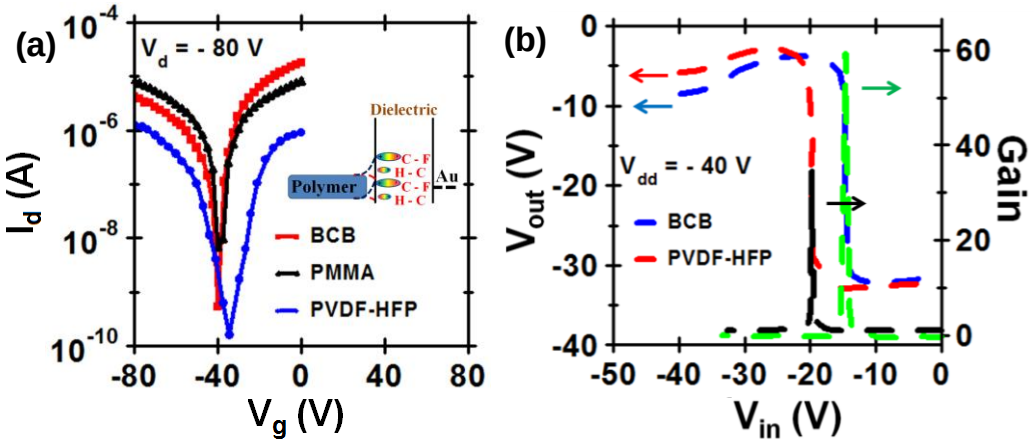


Figure 3.14:*Modification of ambipolar transport in 2DPP-TEG with different dielectric layers. (a) Ambipolar transconductance curve for PFETs with L = 80 μm, W = 1 mm and different dielectric layers; inset shows the schematic of the energy levels of the MIS structure. (b) Typical voltage transfer and gain curves for inverters fabricated with 2DPP-TEG based ambipolar polymer and different dielectric layers.*

Complementary inverters were fabricated as top-contact bottom gate structure with 2DPP-TEG layer acting as both *p*-channel and *n*-channel. The metallic interconnects between the transistors were coated by thermal evaporation of Au after the fabrication of individual transistors. Noise margin and gain was optimized by varying the width of the electrodes. Inverters were characterized by the input-output (V_{in} - V_{out}) transfer characteristics and gain curves. Idealistic (*Z*-type) voltage transfer curves were obtained with balanced charge transport in PVDF-HFP based dielectric layer. These ambipolar inverters with Au S-D electrode operated both in positive and negative input bias (V_{dd}). Voltage gain ($G = \frac{dV_{out}}{dV_{in}}$) magnitude of 40 was obtained with PVDF-HFP dielectric layer and 55 with low-*k* dielectric based inverter. However, the magnitude of *G* increases to 65 and 58 for *n*-FET load inverter and *p*-FET load inverter respectively upon using Al electrode in *n*-FET and Au S-D electrode in *p*-FETs. This enables better off state properties of the inverter, thus enhancing the gain. The operating frequency of these complementary logic circuits was obtained to be > 100 kHz by comparing the output voltage with the input pulse at various frequencies for devices with small channel length of 5 μm. Demonstration

of these bipolar inverters with balanced transport high gain and fast switching response is a starting point in the design of 2DPP-TEG polymer based logic circuits.

3.14 Conclusion

The advent of this new high-mobility semiconducting polymer has opened up a window to address fundamental issues in electrical transport mechanism and obtaining extended state conduction. N-type PFETs with $\mu_{FET} > 2$ $cm^2V^{-1}s^{-1}$ was observed in 2DPP-TEG polymer system. A crossover in *T* dependent processes from activated non-adiabatic transport to an extended adiabatic transport is observed in the high *T* regime where $\mu_{Hall} \sim \mu_{FET}$. Comprehensive studies with different combinations of dielectrics and semiconductors bring out the different conditions for observing band-like extended transport in polymers. The unifying requirement for band-type transport is a combination of molecular and macroscopic parameters originating from the co-planar structure, interconnected aggregates along with an optimum interface and dielectric environment. This demonstration of extended state transport in low-disordered polymeric materials will form the basis to explore various 2D quantum phenomena expected from solution-processed high-mobility PFETs.

References

1. Zaumseil, J.; Sirringhaus, H., Electron and Ambipolar Transport in Organic Field-Effect Transistors. *Chem. Rev.* **2007,** *107* (4), 1296-1323.

2. Ha, T.-J.; Sonar, P.; Dodabalapur, A., Charge transport study of high mobility polymer thin-film transistors based on thiophene substituted diketopyrrolopyrrole copolymers. *Phys. Chem. Chem. Phys.* **2013,** *15* (24), 9735-9741.

3. Stafstrom, S., Electron localization and the transition from adiabatic to nonadiabatic charge transport in organic conductors. *Chem. Soc. Rev.* **2010,** *39* (7), 2484-2499.

4. (a) Kanimozhi, C.; Yaacobi-Gross, N.; Chou, K. W.; Amassian, A.; Anthopoulos, T. D.; Patil, S., Diketopyrrolopyrrole–Diketopyrrolopyrrole-Based Conjugated Copolymer for High-Mobility Organic Field-Effect Transistors. *J. Am. Chem. Soc.* **2012,** *134* (40), 16532-16535; (b) Li, J.; Zhao, Y.; Tan, H. S.; Guo, Y.; Di, C.-A.; Yu, G.; Liu, Y.; Lin, M.; Lim, S. H.; Zhou, Y.; Su, H.; Ong, B. S., A stable solution-processed polymer semiconductor with record high-mobility for printed transistors. *Sci. Rep.* **2012,** *2*.

5. Sakanoue, T.; Sirringhaus, H., Band-like temperature dependence of mobility in a solution-processed organic semiconductor. *Nat Mater* **2010,** *9* (9), 736-740.

6. Panzer, M. J.; Frisbie, C. D., High Carrier Density and Metallic Conductivity in Poly(3-hexylthiophene) Achieved by Electrostatic Charge Injection. *Adv. Funct. Mater.* **2006,** *16* (8), 1051-1056.

7. Liu, T.; Troisi, A., Understanding the Microscopic Origin of the Very High Charge Mobility in PBTTT: Tolerance of Thermal Disorder. *Adv. Funct. Mater.* **2013**, n/a-n/a.
8. Dhoot, A. S.; Yuen, J. D.; Heeney, M.; McCulloch, I.; Moses, D.; Heeger, A. J., Beyond the metal-insulator transition in polymer electrolyte gated polymer field-effect transistors. *Proc. Nat. Aca. Sci.* **2006,** *103* (32), 11834-11837.
9. (a) Dhoot, A. S.; Wang, G. M.; Moses, D.; Heeger, A. J., Voltage-Induced Metal-Insulator Transition in Polythiophene Field-Effect Transistors. *Phys. Rev. Lett.* **2006,** *96* (24), 246403; (b) Wang, S.; Ha, M.; Manno, M.; Daniel Frisbie, C.; Leighton, C., Hopping transport and the Hall effect near the insulator–metal transition in electrochemically gated poly(3-hexylthiophene) transistors. *Nat Commun* **2012,** *3*, 1210.
10. (a) Veres, J.; Ogier, S. D.; Leeming, S. W.; Cupertino, D. C.; Mohialdin Khaffaf, S., Low-k Insulators as the Choice of Dielectrics in Organic Field-Effect Transistors. *Adv. Funct. Mater.* **2003,** *13* (3), 199-204; (b) Asadi, K.; Kronemeijer, A. J.; Cramer, T.; Jan Anton Koster, L.; Blom, P. W. M.; de Leeuw, D. M., Polaron hopping mediated by nuclear tunnelling in semiconducting polymers at high carrier density. *Nat Commun* **2013,** *4*, 1710; (c) Senanayak, S. P.; Guha, S.; Narayan, K. S., Polarization fluctuation dominated electrical transport processes of polymer-based ferroelectric field effect transistors. *Phys. Rev. B* **2012,** *85* (11), 115311.
11. Sondermann, U.; Kutoglu, A.; Bassler, H., X-ray diffraction study of the phase transition in crystalline tetracene. *J. Phys. Chem.* **1985,** *89* (9), 1735-1741.
12. Salleo, A.; Chen, T. W.; Völkel, A. R.; Wu, Y.; Liu, P.; Ong, B. S.; Street, R. A., Intrinsic hole mobility and trapping in a regioregular poly(thiophene). *Physical Review B* **2004,** *70* (11), 115311.
13. Braun Dietrich , H. C., Matthias Rehahn, Helmut Ritter, Brigitte Voit., Polymer Synthesis: Theory and Practice: Fundamentals, Methods, Experiments (5th edition). . **2012**.
14. (a) Street, R. A.; Northrup, J. E.; Salleo, A., Transport in polycrystalline polymer thin-film transistors. *Physical Review B* **2005,** *71* (16), 165202; (b) Gomes, H. L.; Stallinga, P.; Cölle, M.; de Leeuw, D. M.; Biscarini, F., Electrical instabilities in organic semiconductors caused by trapped supercooled water. *Applied Physics Letters* **2006,** *88* (8), -; (c) Mattias Andersson, L.; Osikowicz, W.; Jakobsson, F. L. E.; Berggren, M.; Lindgren, L.; Andersson, M. R.; Inganäs, O., Intrinsic and extrinsic influences on the temperature dependence of mobility in conjugated polymers. *Organic Electronics* **2008,** *9* (5), 569-574.
15. Di Pietro, R.; Fazzi, D.; Kehoe, T. B.; Sirringhaus, H., Spectroscopic Investigation of Oxygen- and Water-Induced Electron Trapping and Charge Transport Instabilities in n-type Polymer Semiconductors. *J. Amer. Chem. Soc.* **2012,** *134* (36), 14877-14889.
16. Nicolai, H. T.; Kuik, M.; Wetzelaer, G. A. H.; de Boer, B.; Campbell, C.; Risko, C.; Brédas, J. L.; Blom, P. W. M., Unification of trap-limited electron transport in semiconducting polymers. *Nat Mater* **2012,** *11* (10), 882-887.
17. (a) Jones, B. A.; Facchetti, A.; Wasielewski, M. R.; Marks, T. J., Tuning Orbital Energetics in Arylene Diimide Semiconductors. Materials Design for Ambient Stability of n-Type Charge Transport. *J. Amer. Chem. Soc.* **2007,** *129* (49), 15259-15278; (b) Mei, J.;

Bao, Z., Side Chain Engineering in Solution-Processable Conjugated Polymers. *Chem. Mat.* **2013**.

18. Kanimozhi, C.; Yaacobi-Gross, N.; Burnett, E. K.; Briseno, A. L.; Anthopoulos, T. D.; Patil, S., Role of Alkyl Chain in Rational Design of N-Type Diketopyrrolopyrrole-based Conjugated Polymers: What have we learned? In *Manuscript under preparation*, 2013.

19. (a) Gomes, H. L.; Stallinga, P.; Cölle, M.; de Leeuw, D. M.; Biscarini, F., Electrical instabilities in organic semiconductors caused by trapped supercooled water. *Appl. Phys. Lett.* **2006,** *88* (8), -; (b) Kemerink, M.; Hallam, T.; Lee, M. J.; Zhao, N.; Caironi, M.; Sirringhaus, H., Temperature- and density-dependent channel potentials in high-mobility organic field-effect transistors. *Phys. Rev. B* **2009,** *80* (11), 115325.

20. Worne, J. H.; Anthony, J. E.; Natelson, D., Transport in organic semiconductors in large electric fields: From thermal activation to field emission. *Appl. Phys. Lett.* **2010,** *96* (5), 053308.

21. Yuen, J. D.; Menon, R.; Coates, N. E.; Namdas, E. B.; Cho, S.; Hannahs, S. T.; Moses, D.; Heeger, A. J., Nonlinear transport in semiconducting polymers at high carrier densities. *Nat Mater* **2009,** *8* (7), 572-575.

22. Kronemeijer, A. J.; Pecunia, V.; Venkateshvaran, D.; Nikolka, M.; Sadhanala, A.; Moriarty, J.; Szumilo, M.; Sirringhaus, H., Two-Dimensional Carrier Distribution in Top-Gate Polymer Field-Effect Transistors: Correlation between Width of Density of Localized States and Urbach Energy. *Adv. Mater.* **2014,** *26* (5), 728-733.

23. Xia, Y.; Cho, J. H.; Lee, J.; Ruden, P. P.; Frisbie, C. D., Comparison of the Mobility–Carrier Density Relation in Polymer and Single-Crystal Organic Transistors Employing Vacuum and Liquid Gate Dielectrics. *Adv. Mater.* **2009,** *21* (21), 2174-2179.

24. Yan, H.; Schuettfort, T.; Kronemeijer, A. J.; McNeill, C. R.; Ade, H. W., Influence of dielectric-dependent interfacial widths on device performance in top-gate P(NDI2OD-T2) field-effect transistors. *Appl. Phys. Lett.* **2012,** *101* (9), 093308.

25. Minder, N. A.; Ono, S.; Chen, Z.; Facchetti, A.; Morpurgo, A. F., Band-Like Electron Transport in Organic Transistors and Implication of the Molecular Structure for Performance Optimization. *Adv. Mater.* **2012,** *24* (4), 503-508.

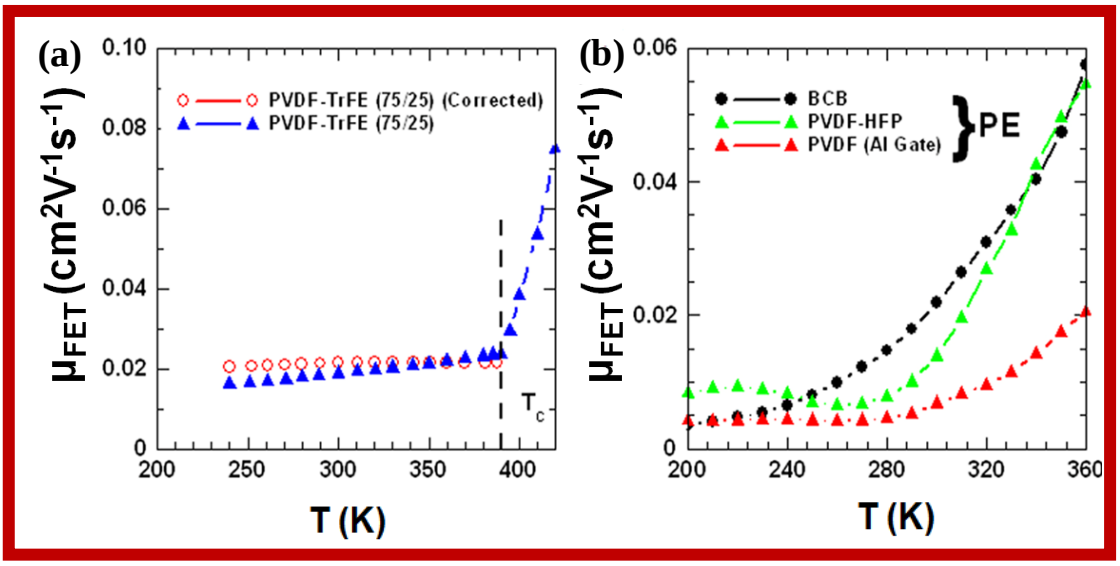
26. Caironi, M.; Bird, M.; Fazzi, D.; Chen, Z.; Di Pietro, R.; Newman, C.; Facchetti, A.; Sirringhaus, H., Very Low Degree of Energetic Disorder as the Origin of High Mobility in an n-channel Polymer Semiconductor. *Adv. Funct. Mater.* **2011,** *21* (17), 3371-3381.

27. (a) Zhang, X.; Bronstein, H.; Kronemeijer, A. J.; Smith, J.; Kim, Y.; Kline, R. J.; Richter, L. J.; Anthopoulos, T. D.; Sirringhaus, H.; Song, K.; Heeney, M.; Zhang, W.; McCulloch, I.; DeLongchamp, D. M., Molecular origin of high field-effect mobility in an indacenodithiophene–benzothiadiazole copolymer. *Nat Commun* **2013,** *4*; (b) Noriega, R.; Rivnay, J.; Vandewal, K.; Koch, F. P. V.; Stingelin, N.; Smith, P.; Toney, M. F.; Salleo, A., A general relationship between disorder, aggregation and charge transport in conjugated polymers. *Nat Mater* **2013,** *12* (11), 1038-1044.

28. Mehraeen, S.; Coropceanu, V.; Brédas, J.-L., Role of band states and trap states in the electrical properties of organic semiconductors: Hopping versus mobility edge model. *Physical Review B* **2013,** *87* (19), 195209.
29. Podzorov, V.; Menard, E.; Rogers, J. A.; Gershenson, M. E., Hall Effect in the Accumulation Layers on the Surface of Organic Semiconductors. *Phys. Rev. Lett.* **2005,** *95* (22), 226601.
30. (a) Chang, J.-F.; Sakanoue, T.; Olivier, Y.; Uemura, T.; Dufourg-Madec, M.-B.; Yeates, S. G.; Cornil, J.; Takeya, J.; Troisi, A.; Sirringhaus, H., Hall-Effect Measurements Probing the Degree of Charge-Carrier Delocalization in Solution-Processed Crystalline Molecular Semiconductors. *Phys. Rev. Lett.* **2011,** *107* (6), 066601; (b) Germs, W. C.; Guo, K.; Janssen, R. A. J.; Kemerink, M., Unusual Thermoelectric Behavior Indicating a Hopping to Bandlike Transport Transition in Pentacene. *Phys. Rev. Lett.* **2012,** *109* (1), 016601.
31. (a) Takeya, J.; Tsukagoshi, K.; Aoyagi, Y.; Takenobu; Y, I., Hall Effect of Quasi-Hole Gas in Organic Single-Crystal Transistors. *Jpn. J. Appl. Phys.* **2005,** *44*, L1393-L1396; (b) Sichel, E. K.; Greber, L.; Wang, K., Hall effect in amorphous Si:H and amorphous Si:H/amorphous Ge:H superlattices. *Applied Physics Letters* **1988,** *52* (13), 1074-1076; (c) Le Comber, P. G.; Jones, D. I.; Spear, W. E., Hall effect and impurity conduction in substitutionally doped amorphous silicon. *Philosophical Magazine* **1977,** *35* (5), 1173-1187.
32. Steyrleuthner, R.; Schubert, M.; Jaiser, F.; Blakesley, J. C.; Chen, Z.; Facchetti, A.; Neher, D., Bulk Electron Transport and Charge Injection in a High Mobility n-Type Semiconducting Polymer. *Adv. Mater.* **2010,** *22* (25), 2799-2803.
33. Baeg, K.-J.; Khim, D.; Jung, S.-W.; Kang, M.; You, I.-K.; Kim, D.-Y.; Facchetti, A.; Noh, Y.-Y., Remarkable Enhancement of Hole Transport in Top-Gated N-Type Polymer Field-Effect Transistors by a High-k Dielectric for Ambipolar Electronic Circuits. *Adv. Mater.* **2012,** *24* (40), 5433-5439.
34. (a) Kobayashi, S.; Nishikawa, T.; Takenobu, T.; Mori, S.; Shimoda, T.; Mitani, T.; Shimotani, H.; Yoshimoto, N.; Ogawa, S.; Iwasa, Y., Control of carrier density by self-assembled monolayers in organic field-effect transistors. *Nat Mater* **2004,** *3* (5), 317-322; (b) DiBenedetto, S. A.; Facchetti, A.; Ratner, M. A.; Marks, T. J., Molecular Self-Assembled Monolayers and Multilayers for Organic and Unconventional Inorganic Thin-Film Transistor Applications. *Adv. Mater.* **2009,** *21* (14-15), 1407-1433.

Chapter 4

Polar Dielectrics in Polymer Field Effect Transistors



Chapter 4

Polar Dielectrics in Polymer Field Effect Transistors

4.1 Introduction

The performance of polymer field effect transistors (PFETs) has been enhanced by the combination of new molecular materials and device fabrication procedure which involve ordered microstructures[1].These sustained efforts have resulted in improvement of polymeric materials systems with high degree of self-organization and mobility (μ_{FET}) magnitudes approaching ≈ 3 $cm^2V^{-1}s^{-1}$ [1a, 2]. In addition, to the development of new polymeric materials with higher μ_{FET}, the performance of PFETs is also enhanced by engineering the dielectric material at the interface[1a]. There have been a range of studies on small molecule based FETs fabricated with different dielectric layers[3]. Since small molecules can be ordered and crystalline, the effects of dielectric layer can be clearly studied. Unlike the studies on small molecule based FETs, there have been fewer efforts in polymer FETs to identify and evaluate the effects of polarization of the dielectric layer[4]. In the molecular systems, it has been hypothesized that effective mass of charge carriers increase if the gate dielectric is sufficiently polar[3]. Similarly, in the case of polymeric semiconductors it has been shown that polar dielectric increases the disorder at the interface and broadens the density of states (DOS) in the semiconductor. However, a clear understanding of the source of disorder in different classes of dielectric materials is hitherto unknown. In this context, a range of polyvinylidene fluoride (PVDF) based polar dielectric materials which exhibit ferroelectric (FE) and paraelectric (PE) properties are explored to understand the effect of dielectric polarization on the charge transport of a PFET device.

4.2 Dielectric in FET

Dielectric layer in the PFET structure plays a critical role in deciding the interfacial disorder which the charge carriers encounter [5]. In case of FETs based on single crystals like: rubrene it was observed that polar dielectrics like Al_2O_3, Ta_2O_5 etc introduce disorder at the interface[3]. This gets reflected in the observed $\mu_{FET}(T)$ trends. With the increase in dielectric constant (*k*), the transport mechanism undergoes a transition from "metallic like" to "insulating like" charge transport. This effect of the high-*k* dielectric layer on the transport mechanism of molecular crystals has been studied from the perspective of Froehlich polarons i.e., charge carriers bound to an ionic polarization cloud in the surrounding medium. In case of polymeric semiconductors, the model adopted to explain the influence of polar dielectric is in terms of static dipolar disorder[3, 5a]. Based on these studies, it is largely accepted that low-*k* dielectric interfaces are beneficial in minimizing localization and provide lower hysteresis in the transconductance plots, whereas polar dielectrics induce electrostatic dipolar disorder which effectively reduce the μ_{FET}. The dielectric induced energetic disorder is estimated from Arrhenius type *T* dependent of the transport studies in the framework of thermally assisted hopping[5a, 6]. The broadening of density of states (E_{broad}) changes 57 meV to 85 meV for a *k* variation from 2 to 4[5a]. Apart from polymer dielectrics, electrolytes or ionic liquids have also been used as dielectric material in a PFET. In these dielectrics the ultrathin Debye layer acts as the capacitive layer enabling device operation at low voltages. The carrier density '*n*' in these electrolyte gated FETs is higher than conventional polymer dielectrics by two orders (> 10^{14} cm^{-2}), so the disorder induced trap states are filled to a greater extent even at small V_g [7]. Thus higher μ_{FET} is obtained in these devices since the carriers encounter fewer empty trap sites. The electrolyte gated transistors have demonstrated E_A ~ 7 meV compared to E_A ~ 56 meV observed in case of low *k* dielectric for regioregular-poly-3-hexylthiophene - P3HT FETs[5b]. However, comparison of the dielectric induced disorder across different device structures and interface would be erroneous due to variations in processing conditions, morphology and interfacial energy. In order to overcome this issue, appropriate dielectric layer was chosen which allowed the access to nearly an order of magnitude range of polarization (*k* ~ 4 to 24) with *T* as the tuning parameter. Such a system offered a test bed to follow the changes in the transport physics with polarization. This variation of the polarization strength in the dielectric layer can modulate the coupling strength of charge carriers with

dielectric from weak to strong coupling regime. In addition, the measurement from different class of dielectric materials with similar dielectric constant provides understanding on the origin of disorder at the interface.

4.3 Device Fabrication

Bottom gated top contact FETs were fabricated by coating required electrode-Al or Cr/Au (10^{-6} mbar, 1 Å/s, 30 nm thick) by shadow mask technique on standard RCA cleaned glass substrates. PFETs with Au gate electrodes were preferred for devices where FE dielectric was essential and Al gate electrodes were coated for devices where the dielectric can exist in mixed phase[8]. The dielectric layers were obtained by spin coating the respective solutions (PVDF and PVDF-HFP at 80mg/ml in N, N-Dimethylacetamide, PVDF-TrFE (75/25) at 40mg/ml in Butane-2-one and BCB in Mesitylene) at 1000 rpm for 1 minute to obtain films of thickness 0.6 μm - 0.8 μm. The films were rapidly annealed in vacuum below their melting point (150 ^{o}C for PVDF, 120 ^{o}C for PVDF-HFP and PVDF-TrFE) to improve crystallinity of the films and obtain desired phases of the dielectric. The BCB films were annealed for 30 minutes at 290 °C in vacuum. P3HT was then coated from a solution of 10mg/ml in chlorobenzene at 1000 rpm for 1 minute to obtain films of thickness ~ 80nm. This was followed by the deposition of Au source drain electrode (10^{-6} mbar, 1 Å/s, 20 nm thick) by shadow masking technique to obtain channels of length 80 - 100 μm and width 1mm (**inset Figure: 4.1a**).

4.4 FET Characterization

PFETs were characterized with two identical source meters - Keithley 2400 and high impedance electrometer Keithley 6514 and cross-checked with measurements from a standard Keithley 4200 semiconductor parameter analyzer. The devices exhibited *p*-type transport with current modulation > 10^3 - 10^4 (leakage current three to four orders of magnitude lower) and μ_{FET} ~ 0.01 $cm^2V^{-1}s^{-1}$ which is comparable with other PFETs fabricated in similar geometry[9]. **Figure: 4.1** depict the typical output and transconductance curve for the top contact bottom gated transistors made with P3HT as the active semiconducting layer and PVDF-TrFE as the dielectric. More than 100 devices were tested for these studies, and the results presented from the representative statistical median.

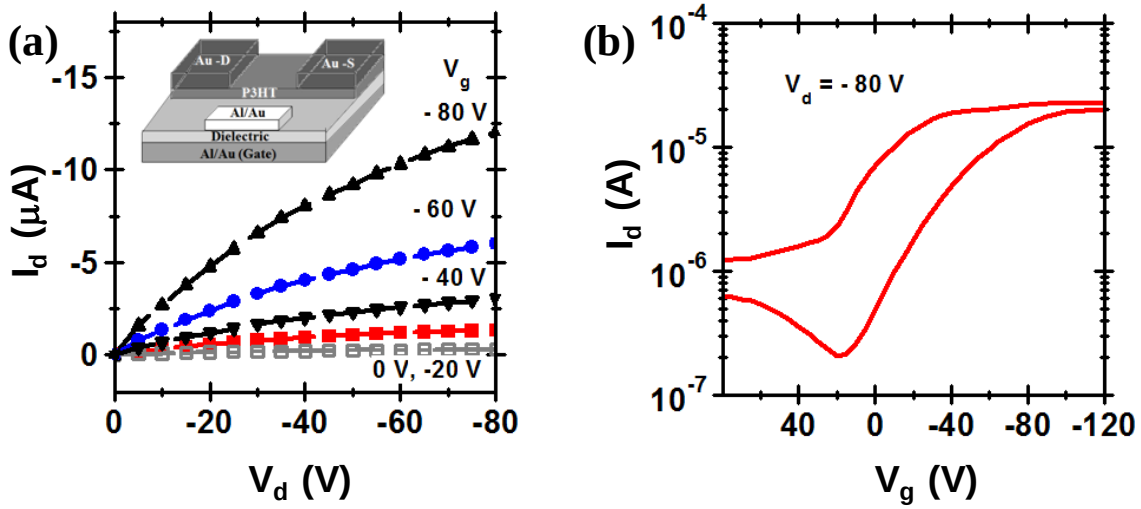


***Figure 4.1**: Typical (a) output and (b) transconductance plots for P3HT/PVDF-TrFE transistors with L = 40 μm, W = 1mm. Inset shows the schematic of the device.*

Temperature dependent transport measurements were performed on these devices (**Figure: 4.2**) to understand the thermal barriers and activation energy involved in the transport.

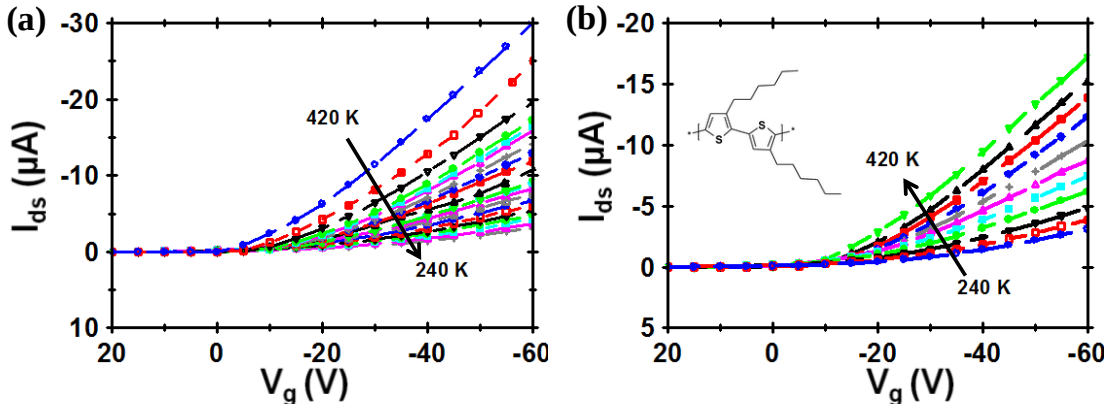


***Figure 4.2**: Typical transconductance curves for PVDF-TrFE (75/25) based FE-FET with L = 40 μm, W = 1mm for T cycles (a) 420 K -240 K (b) 240 K – 420 K at V_d = - 60 V. Inset shows the structure of the polymer. Reproduced with permission from Phys. Rev B, 85 (11), 115311.*

In order to ascertain that the current variation is not a consequence of factors such as bias stress and process variations, the devices were made to go through a complete thermal cycle (100 K – 450 K). Typical hysteresis behavior observed in ferroelectric FETs (FE-FET) were minimized to a large extent by applying sufficient positive bias and driving back

the FET to the original off state condition (within 0 - 5 % variation) to have independent measurements at each *T*.

4.5 Polarization in Ferroelectric FET

In a FE dielectric, the total polarization (P_{tot}) has a non-linear contribution in addition to the linear contribution: $P_{tot} = P_{lin} + 2P_r - P_{sat}$,[10] where P_{lin} is the linear contribution to the polarization, P_r is the remnant polarization and P_{sat} is the saturation polarization. At low *T*, $P_{tot} \approx P_{lin} + P_r$ (as $P_r \sim P_{sat}$) and for high *T*, $P_{tot} \approx P_{lin} - P_{sat}$ (as $P_r << P_{sat}$). It is to be noted that conventional FET equations do not account for the additional non-linear polarization ($P_{nl} = 2P_r - P_{sat}$) of the dielectric (**Figure: 4.3**)

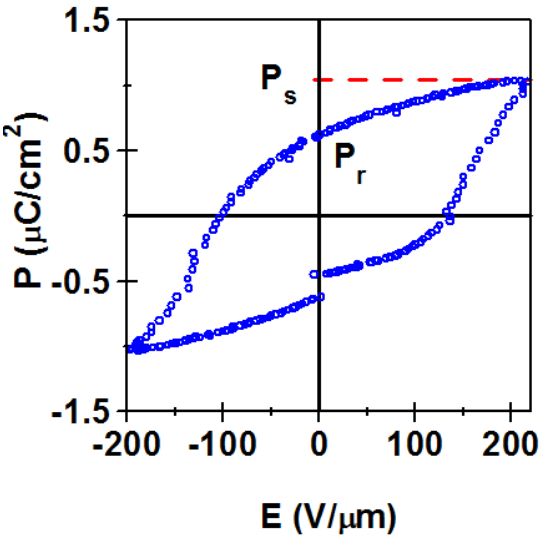


Figure 4.3: *Typical P-E curve of PVDF-TrFE films (400 nm) in a MIM geometry*

A compact model of a FE-FET involving non-linear component would then have an equivalent circuit at the gate which consists of one resistor and four capacitors in parallel (one of which is linear and other three being non-linear)[11]. In the framework of distributed threshold switching model for PVDF the relaxation period of domains follow a distribution function[11]. The non-linear component of the polarization is taken into account by including a correction to V_g, in the form of an equivalent voltage due to FE-polarization: $V_0 \approx P_{nl}d/\varepsilon_0\varepsilon_r$ where *d* is the thickness of dielectric layer, ε_0 is the permittivity of vacuum, and ε_r is the dielectric constant of the dielectric layer. This voltage accounts for the additional charge density at the channel. The saturation regime μ_{FET} was calculated with the modified transconductance expression: $I_{ds} = (\mu_{FET}WC_i/2L)(V_g + V_0 - V_{th})^2$, where C_i is the effective

capacitance of the dielectric layer, *W* is the channel width and *L* is the channel length of the transistor (see **Appendix 1** for the derivation).

The polarization behavior of the dielectric material is obtained from the capacitors fabricated alongside the FETs as MIM (Metal-Insulator-Metal) structures. These capacitors were characterized at 100 Hz using HP4294A **(Figure: 4.4)**. FE-phase of PVDF-TrFE and *β*-PVDF were verified experimentally by *P-E* (Polarization-Electric field) profiles (**Figure: 4.3**). T_c (≈ 390 K) of PVDF-TrFE was also verified from the $C(\omega,T)$ measurements (**Figure: 4.4a**) and was found to be consistent with reported values[12]. However, *β*-PVDF continues to be in the FE phase in the measurement range of 360 K. The measured *k(T)* (**Figure: 4.4**) of the dielectric films reflects thermally activated relaxation mechanism of the polymer chain which promotes the ordered phase and enhances the dielectric constant. In the FE phase, *k(T)* is a measure of the order parameter which takes a quadratic form.

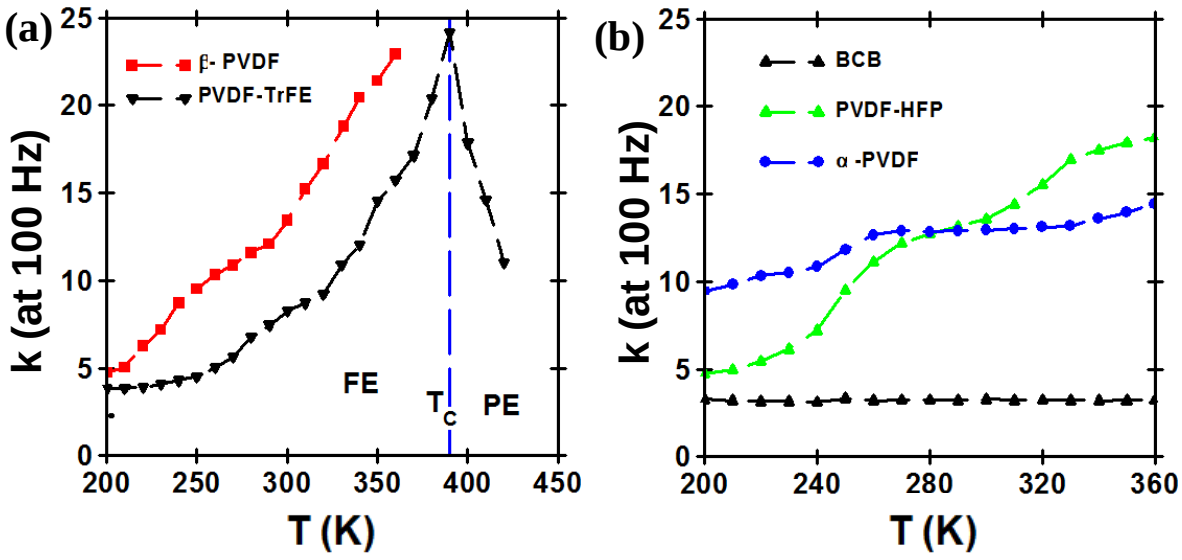


***Figure 4.4**: k(T) variation for different dielectrics measured at 100 Hz in MIM structure for (a) FE dielectrics and (b) PE dielectrics. PVDF-TrFE shows a clear phase transition from the ferroelectric to paraelectric regime. Typical thickness of the dielectric layers ~ 200 – 400 nm. Reproduced with permission from Phys. Rev B, 85 (11), 115311.*

The experimentally measured polarization and *k* at different *T* is incorporated into the modified FET equations to arrive at $\mu_{FET}(T)$ as shown in **Figure: 4.5**. V_0 obtained from $I_d(V_g)$, at different *T*, indeed followed a similar trend as $P_r(T)$ (independently obtained from *P-E* measurements and is shown in **Figure: 4.6**. P_{nl} translates to a small correction in the final μ_{FET} and minor discrepancies in the estimate may arise if poling is not carried out

during the film forming process. Corrections arising from the P_{nl} differs from the effective gate voltage modifications due to factors originating from semiconductor carrier density[13] and trapping of the induced charges at low *T*. It was ensured that the value of *C* obtained from *C-V* measurements was in a similar bias range as that employed for extracting μ_{FET}. It should be noted that *k(T)* represents a macroscopically averaged quantity which is utilized for estimating the microscopic parameter μ_{FET}. Therefore, the inherent variations and fluctuations can dominate $\mu_{FET}(T)$ response and may not reflect the real transport scenario; rather it represents an averaged quantity called $<\mu_{FET}(T)>$.

4.6 $<\mu_{FET}(T)>$

4.6.1 Single layer dielectric

$<\mu_{FET}(T)>$ is obtained for different systems in the range 100 K < T_c < 420 K (**Figure: 4.5**).

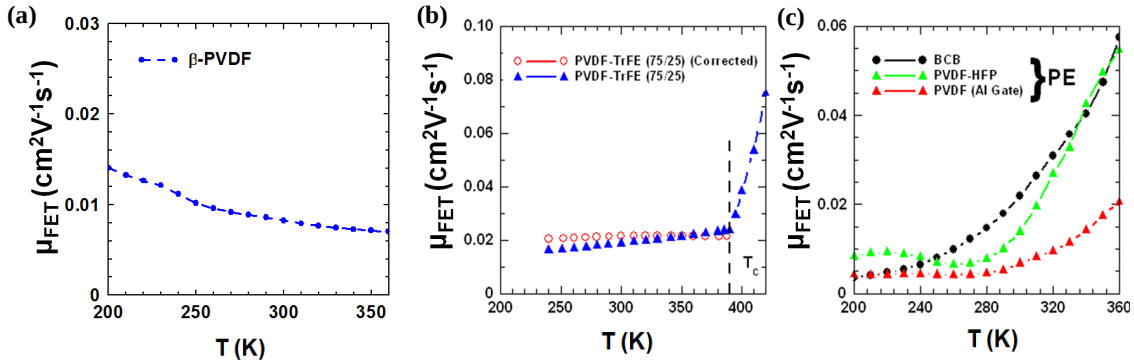


***Figure 4.5**: $<\mu_{FET}>$ for P3HT-FET devices (L = 60 μm, W = 1mm) fabricated with dielectrics (a) ferroelectric β-PVDF, (b) ferroelectric PVDF-TrFE and (b) PE dielectrics PVDF-HFP, α-PVDF and BCB. Solid lines indicate transport in the FE- regime and dashed line is for the transport in PE-regime. Corrected $<\mu_{FET}>$ is obtained by accounting for the nonlinear contribution to the ferroelectric polarization. Reproduced with permission from Phys. Rev B, 85 (11), 115311.*

Arrhenius fits are used to evaluate the *T*-dependence. Different dielectrics yield the following transport characteristics from *T*-dependent FET studies: (i) weak *T* dependence of $<\mu_{FET}(T)>$ in the FE regime, (E_A < 15 meV) for PVDF-TrFE based FE-FETs, which becomes strongly *T* dependent upon the phase transition to PE regime (E_A ~ 0.4 eV); (ii) for β-PVDF based FETs, $<\mu_{FET}(T)>$ is nearly *T* independent, and in fact appears to marginally

decrease with increasing T (240 K < T < 360 K); (iii) for devices with high-k paraelectric layer a strong T-dependence $<\mu_{FET}(T)>$ (E_A ~ 46-76 meV) is evident in 200 K < T < 290 K regime.

The apparent weak T dependence of $<\mu_{FET}(T)>$ cannot be construed as an indicator of higher delocalization lengths since the fluctuations due to $k(T)$ are inbuilt in the $<\mu_{FET}(T)>$ estimates. Hence, E_A obtained from $\mu_{FET}(T)$ should not be taken as a figure of merit to gauge the order (band-like versus hopping) in such device systems. It has been reported that in PVDF the FE switching usually involves domains, which is then expected to be accompanied by T dependent relaxation processes and can manifest as fluctuations. In case of FE-FETs, the observed $<\mu_{FET}(T)>$ includes contribution from $I_{ds}(T)$, thermal motion of the dipoles (which can be gauged by the pyro-electric coefficient) and the collective domain fluctuations. In general, it is observed that $I_{ds}(T)$ is an increasing function of T due to thermal activation processes. The thermal vibration of dipoles increases with T which decreases P_r with T (**Figure: 4.6**)[14].

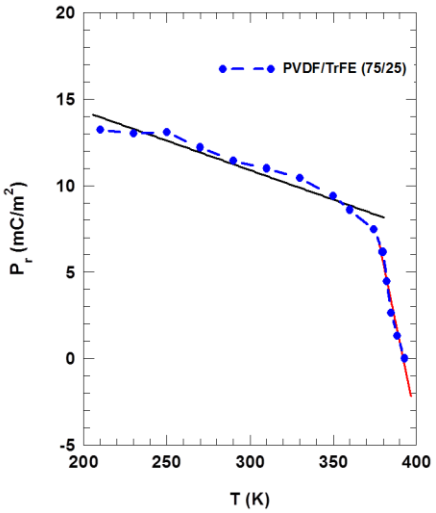


Figure 4.6*: Variation of polarization retention with T for PVDF-TrFE dielectric in MIM structure obtained from P-E curves at different T. Reproduced with permission from Phys. Rev B, 85 (11), 115311.*

The decrease in P_r with T is reflected in the lowering of charge density at the interface. Similarly, increase in T ($T < T_c$) increases the domain fluctuation which introduces dynamic disorder. As evident from the $<\mu_{FET}(T)>$ behavior the transport in the FE- regime is dominated by macroscopic fluctuations (with minor contribution from the

thermal motion of individual dipoles). This domain fluctuation creates a macroscopic dipolar disorder at the interface and suppresses the observed E_A. This dynamic disorder arising from the fluctuations appears to be more significant in the case of β-PVDF which is less crystalline than PVDF-TrFE[15]. Hence, for β-PVDF based FETs a marginal decrease in $<\mu_{FET}(T)>$ is observed with increase in T.

It should be noted that this effect of polarization fluctuation seen as variation in $k(T)$ is different for FE and PE dielectric regimes. The effect of polarization fluctuation on $I_{ds}(T)$ is significantly more in FE-FET than the regular high- k PE dielectric based FETs. This can be related to the distinction between collective (FE) and non-collective polarization (in regular high-k) processes of FE and PE dielectrics respectively[16]. Energetically, the polarization fluctuations can also be depicted as the broadening of the density of occupied states (DOOS) which creating a disordered landscape for charge transport. This type of disorder seems to play a smaller role in high-k (PE) dielectrics and is dominant in FE dielectric based devices. The transition between the static and dynamic disorder becomes obvious upon comparing the $<\mu_{FET}(T)>$ in the region above and below T_c as in the case of PVDF-TrFE. It can thus be concluded that the macroscopic polarization fluctuation is dominant mechanism which controls the charge transport in FE-FET, whereas, static dipolar disorder plays a significant role for the charge transport in devices with high-k PE dielectric layer.

4.6.2 Bi-layer dielectric

In order to distinguish the thermal processes and polarization contribution to $<\mu_{FET}>$, bi-layer dielectric based FETs were fabricated (**Figure: 4.7**).

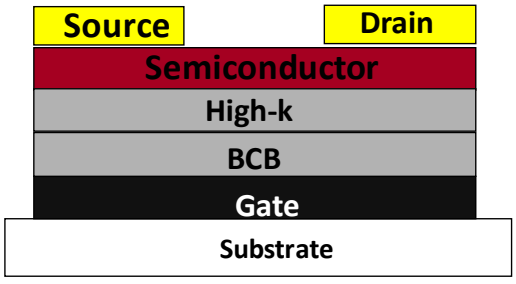


Figure 4.7: *Schematic of the device fabricated for bi-layer dielectric based transport measurements.*

It was ensured that the charge carriers in the semiconductor experiences similar polarization, same FE or PE dielectric was used below the semiconductor . However, the thickness of the dielectric layers were tuned in such a way that the effective capacitance of the bi-layer is mainly governed by the low-k dielectric layer and has no contribution from the top dielectric close to interface. The features observed from *T* dependent studies of the FETs (**Figure: 4.8**) with different bi-layer of dielectrics were the following: (i) $\mu_{FET}^{BCB|FE} > \mu_{FET}^{BCB} > \mu_{FET}^{FE}$ at 300 K where $\mu_{FET}^{BCB|FE}$ is the mobility for FETs with BCB|PVDF-TrFE as the dielectric, μ_{FET}^{BCB} and μ_{FET}^{FE} were the field effect mobilities for BCB and PVDF-TrFE based FETs respectively; (ii) for devices with BCB|PVDF-TrFE in the FE regime, the $\mu_{FET}(T)$ had an activated behavior with activation energy, $E_A^{bi\text{-}layer} \sim 75$ meV, which increased to 130 meV upon phase transition to the PE-regime; (iii) bi-layer dielectric devices made with BCB|high *k* PE-dielectrics also showed an activation mechanism ($E_A^{bi\text{-}layer} \sim 140$ meV) higher than the single layer dielectric devices. It was not possible to make bi-layer dielectric devices with BCB|*β*-PVDF because dominant *β*-phase required the growth of PVDF films on gold substrates.

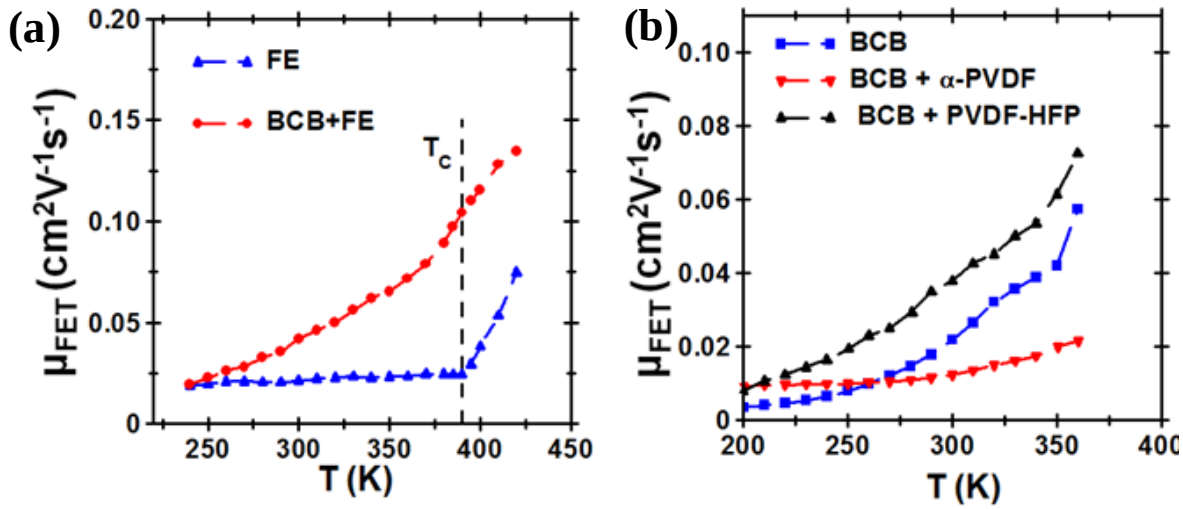


***Figure 4.8**: <μ_{FET}> for bi-layer dielectrics based P3HT PFETs with FE and PE interfaces obtained from devices having similar W/L values (L = 60 μm, W = 1mm). Reproduced with permission from Phys. Rev B, 85 (11), 115311.*

All the devices made from the bi-layer dielectrics exhibited sizable activated behavior and were not dominated by the FE characteristic of fluctuation with *T*. This can be explained on the basis of a reduced effective polarization contribution from the FE layer. The *k(T)* and switching characteristics (in FE dielectric) have been analyzed in terms of nucleation and growth model. The process of kink propagation required for the domain

growth is the source for fluctuation. It is established that this nucleation and growth process decreases with decreased bias and this trend possibly explains the present case of minimal effect from the FE layer in the bi-layer geometry. The experimental results points to a conclusion that bi-layer dielectric device can be utilized to overcome the polarization fluctuation, prevalent in case of the single layer FE-FET. This outcome is of significance in making devices which require sustainable parameters over a wide range of temperature.

Another observation from the *T* dependent study was the lowering of $E_A^{bi\text{-}layer}$ with FE interface. This is indicative of inherent statically ordered phase at the interface similar to the case of low *k* BCB dielectric. The impact of the static dipolar disorder observed in high *k* PE-dielectric is apparently mitigated by employing a FE-dielectric. The transport mechanism is then the combined result of the associated disorder originating from these contrasting environments. The decreased $E_A^{bi\text{-}layer}$ with FE interface can also be attributed to higher carrier concentration, which is consistent with a continuum of localized states above a (hole) transport level, E_t. As the states above E_t are filled with increasing *n* ,the quasi-Fermi level (E_F) is lowered and E_A, *i.e.*, E_F–E_t decreases.[5c]

4.6.3 Analysis of temperature dependence

If the FE component of the bi-layer device is assumed to contribute negligibly to the transport then $<\mu_{FET}^{\text{bi-layer}}(T)>$ can be used as the background reference to evaluate contribution from other additional factors. The polarization fluctuation dependent mobility μ_P was obtained by expressing $<\mu_{FET}>$ as a combination (Matthiessen's rule) of factors originating from interfacial properties and charge retention at the channel by the FE-dielectric,

$$< \mu_{FET} >= (\frac{\mathbf{1}}{< \mu_{\boldsymbol{FET}}^{\boldsymbol{bi-layer}} >} + \frac{\mathbf{1}}{< \mu_{\boldsymbol{P}} >})^{-\mathbf{1}} + \frac{k^{'}(V_g - V_t)^{\delta+1}}{\gamma + 1} \qquad \text{……..(4.1)}$$

where, $<\mu_{FET}^{bi\text{-}layer}>$ is the *T* dependent mobility of bi-layer dielectric based FETs, *k'* is related to the ease of hopping which gives the interfacial properties (interfacial roughness, de-mixing and polymer film morphology on the dielectric), δ is related to the characteristic temperature T_0, γ is related to the width of DOS.[17] This model was utilized to independently extract polarization dependent $<\mu_{FET}>$. The estimated polarization dependent $<\mu_{FET}>$ deviates from an Arrhenius type behavior due to dynamic disorder introduced from the dielectric polarization variation[9].

4.6.4 Temperature dependent study of FE-FET parameters (V_{th}, σ, S):

The mobility measurements in FE-FETs were supplemented by conductivity measurements ($\sigma(T)$) to get a deeper insight into the nature of interfacial transport. $\sigma(T)$ was obtained in the linear regime of operation of the FE-FET with PVDF-TrFE as the dielectric. In the context of 2-D variable range hopping model with $\sigma \propto \exp(T_0/T)^{1/2}$ the localization radius obtained from the Efros-Shklovskii type transport[18] was in the range of 1.5 – 1.9 nm, a value in between that of a PE dielectric (0.7 nm) and an electrolyte (2.6 nm). σ ~ 0.01 S/cm points to a fraction (~ 0.1%) of conductivity contributed from delocalized charge carriers.[19]

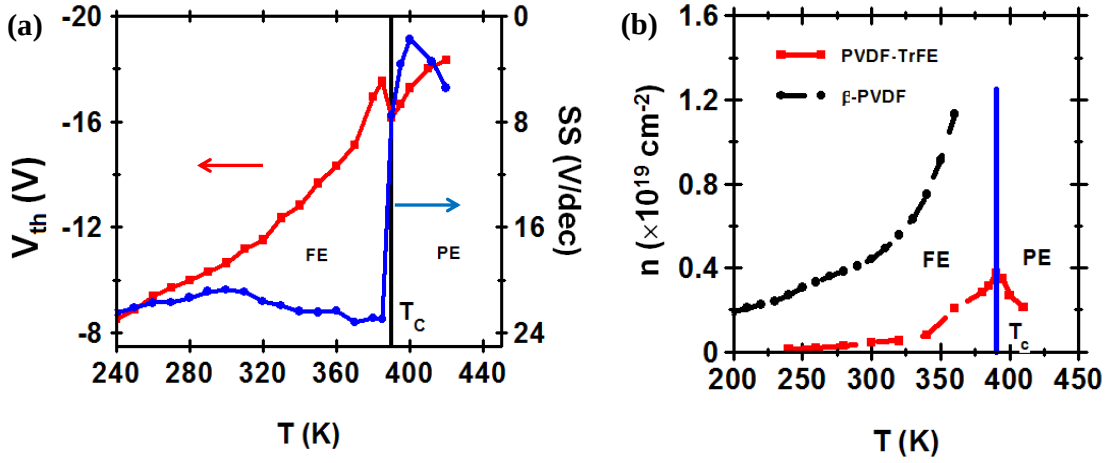


***Figure 4.9**: (a) Variation of V_{th} and SS with T, showing the effect of FE to PE transition obtained from a transistor with PVDF-TrFE as the dielectric and P3HT as the active semiconducting layer (L = 60 μm, W = 1mm). (b) Surface charge density variation of both the PVDF-TrFE and β-PVDF dielectric layer with temperature. Reproduced with permission from Phys. Rev B, 85 (11), 115311.*

The phase transition of the dielectric in single layered FE-FETs is directly reflected in V_{th} (**Figure: 4.9a)**. A sizable step increase in V_{th} was also accompanied by a discontinuity in the sub threshold swing–*SS* (**Figure: 4.9a)**. At T_c, the discontinuity in conductivity ($\approx \Delta\sigma$) was observed to be lower than $\Delta\mu_{FET}$ which implies a lowering of n, i.e., presence of remnant carriers enhance the channel conductance in the FE phase. ΔV_{th} ~ 12 V at T_c can then be reconciled and related to the magnitude of Δn. This clearly indicates the contribution of the FE phase to the extra charge density (**Figure: 4.9b**)[14].

V_{th} variation as a function of k and T can differentiate the contribution of trapping from the impurities and polarization factors. It is observed that, an increase in T is accompanied by a shift in V_{th}, attributed to increased $<\mu_{FET}>$ and decreased trapping,[20]

while an increase in *k* results in higher density of dipolar disorder induced trap states which opposes the V_{th} shift. In the present case, variation of V_{th} with *T* followed the $<\mu_{FET}>$ behavior in the entire FE-regime as is apparent from **Figure: 4.10(a)**. Since $V_{th}(T)$ does not exhibit any obvious relation with $k(T)$ the real picture is more complex than a simplistic impurity/disorder induced trapping, and reinforces the interpretation of the dominant role of random thermal fluctuations.

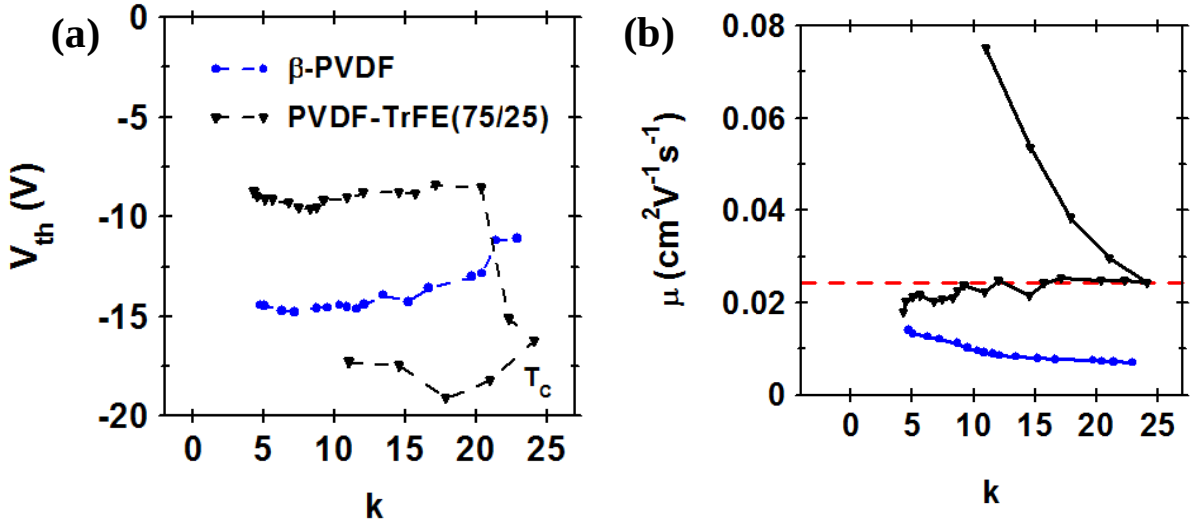


***Figure 4.10**: (a) Variation of V_{th} with k for FE-FET (PVDF/TrFE and β-PVDF as the dielectric); (b) variation of $<\mu_{FET}>$ with k for the same set of devices. Reproduced with permission from Phys. Rev B, 85 (11), 115311. Legends are the same in both figures.*

4.7 Raman Spectroscopic Measurements

The *T* dependent Raman measurements verified the stability of P3HT (200 < T < 420 K) and proves the existence of the strong coupling between the FE layer and the semiconductor[21]. A strong electron-phonon coupling usually manifests itself as asymmetric Raman line shapes in Breit-Wigner Fano (BWF) resonance, which is essentially a coupling of the Raman phonons and the electronic continuum. The BWF line shape is given by:

$$I(\omega) = I_o \frac{\left[\frac{(\omega - \omega_o)}{q} + \Gamma\right]^2}{(\omega - \omega_o)^2 + \Gamma^2} \qquad \text{..... (4.2)}$$

where, ω_0 is the discrete phonon frequency and Γ is the width of the resonant interference between the continuum and discrete scattering channels. The asymmetry parameter ($1/q$)

depends on the average electron-phonon matrix element and the Raman matrix elements between the ground and the electronic state of the phonon and the electron.

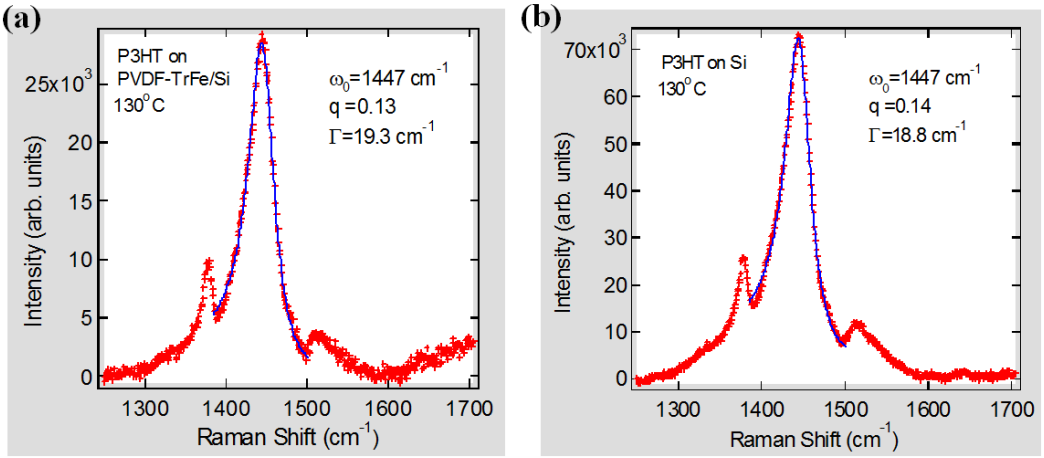


Figure 4.11*: Raman spectra of P3HT films (~ 100 nm) on (a) PVDF/TrFE and (b) Si substrate. Reproduced with permission from Phys. Rev B, 85 (11), 115311.*

The spectra of P3HT coated on PVDF-TrFE retained the features of the constituents, similar to P3HT on Si as a function of *T* (**Figure: 4.11**). However, a change in the P3HT Raman background is observed at around 400 K (ferroelectric to paraelectric transition), upon comparing the Raman line shape of the 1447 cm^{-1} peak for a P3HT film on PVDF-TrFE/Si and a film of P3HT directly coated on Si. The 1447 cm^{-1} peak was fitted with a BWF line shape as shown by the blue curves in the **Figure: 4.11**. The asymmetry parameter and the width (Γ) are similar for both P3HT films at 400 K, indicating that the changes observed in the transport properties at the transition temperature is not due to the semiconductor but rather has an origin in the coupling of the charge carriers with the phonons at the polymer-dielectric interface or because of the polarization variation at the interface.

The Raman spectra for the dielectric films of PVDF-TrFE clearly shows the existence of the β-phase. Upon phase transition a change in the background of the Raman spectra is observed, which is reversible as the temperature is cycled to the FE-phase[22].However, the broadening and frequency shifts of the P3HT Raman peaks as a function of *T* were identical for P3HT on Si and PVDF-TrFe, indicating that the changes in the transport properties at the T_c arises mainly from the coupling of charge carriers when the dielectric is in the FE phase[14].

4.8 Dynamics of depolarizing field

Incidentally, the *β-phase* of PVDF-TrFE has been used to enhance the efficiency of organic solar cells[23] where the long-range FE-field enhances the charge carrier separation. In the presence of a semiconductor, the FE layer develops a depolarizing field (E_{dep})[24] which can be modified to a large extent by photo-generated charge carriers[25]. The FET device geometry allows the tunability of E_{dep} which was used can as a tool to observe the difference in photo-generation dynamics of the PFET transport interface in the polar and non-polar state of the dielectric. In order to closely probe the effect of phase transition on transistor operation, the PFETs were studied in the depletion mode under a constant photo-excitation **(Figure: 4.12)**.

When a transistor operates in depletion mode, the semiconductor does not compensate charges, resulting in depolarization of the ferroelectric material. As soon as light is incident on the semiconductor, photo-generated charge carriers provide the necessary compensation enabling polarization. The photocurrent, $I_{ph}(t)$ response for FE-FETs with PVDF-TrFE as the dielectric is distinctively different from the response obtained from the PFETs fabricated with polyvinyl alcohol (PVA, high k ~ 10) as the dielectric[26]. The rate of increase in $I_{ph}(t)$ upon photo-excitation in FE-FETs is slower since a fraction of the photo-generated charge carriers are utilized to compensate E_{dep}, and this contribution was clearly absent in the PE-phase above T_c. The drain source current with illumination can be described as: $I = I_o(V_g) + I_{ph}$, where, I_o is the dark value of the drain source current and I_{ph} is the light induced component consisting of excess charge carrier contributed from generation and recombination processes. In the case of FE-FETs there is an additional contribution to the drift-term from the E_{dep}, which has a comparatively slow relaxation[24-25]. Upon illumination at low T (T < 200 K), a consistent trend of slower rising rate of $I_{ph}(t)$ with increasing V_g (which implies increased depletion or higher E_{dep}) is observed. At high T, (T > 300 K) the trend in the dynamics of $I_{ph}(t)$ with continuous illumination is altered. The transport processes are then dominated by recombination rather than factors like depolarization.

The I_{ph} decay response upon termination of a light pulse is a recombination limited process due to the presence of large density of traps.[26] I_d settles to an intermediate metastable state with an extremely slow relaxation (50 % drop over a period of 3 h). The retention factor, R_f (≈ I_d in the metastable state/I_{dark}) for devices with FE-dielectric is about 3 times more compared to devices where PVA was used. The high retention fraction is

attributed to a slower relaxation of ferroelectric materials to the depolarized state in the absence of any external bias. R_f decreases with increasing T as expected and does not exist in the PE-phase since recombination factors dominate. Our observations from photo-generated transport show the existence of a field originating from the non-linear contribution to polarization in the FE-layer, which affects bulk charge transport in the polymer. This is a clear signature of a long-range polymer-dielectric interaction and is consistent with the physical model speculated for ferro and paraelectric dielectrics.

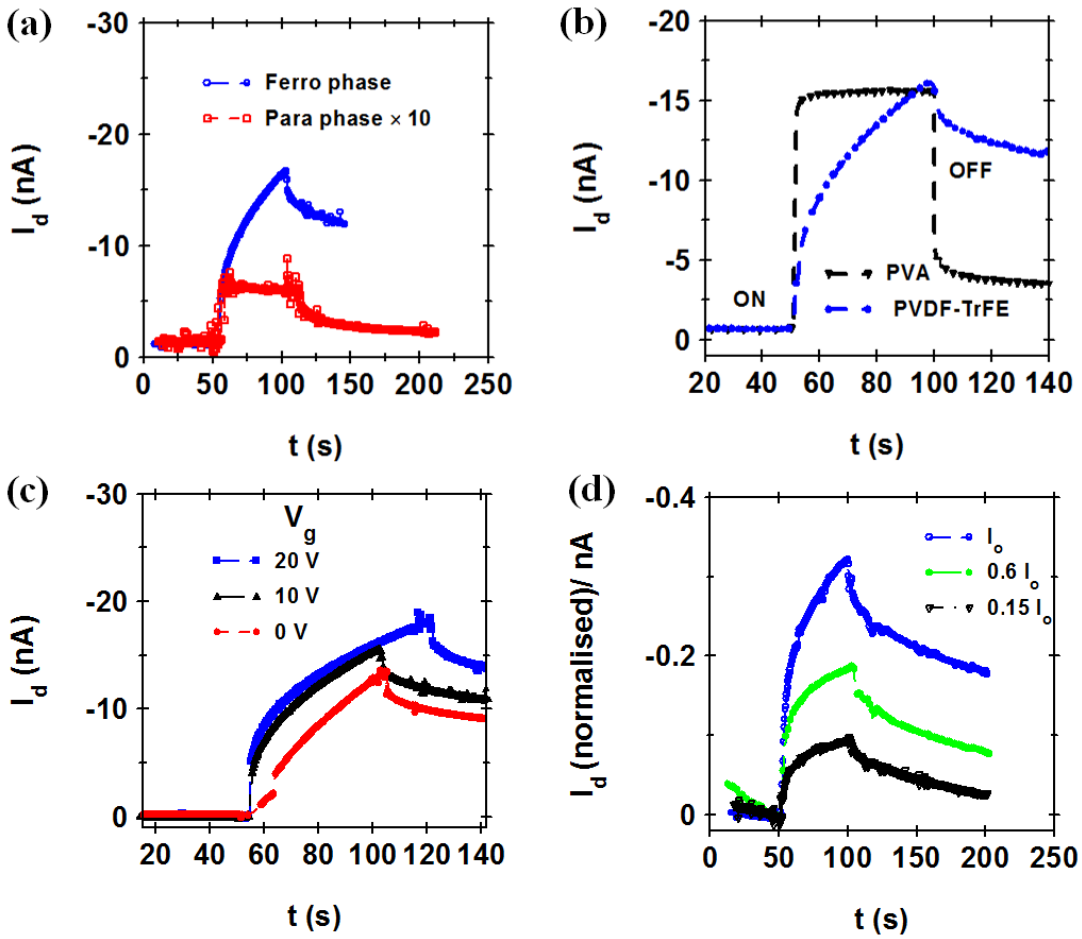


***Figure 4.12**: Photo response of the transistor with different dielectrics and P3HT as the semiconducting layer operating in the depletion mode (V_d = - 60 V, V_g = 20 V) using a light source of intensity I_o = 2 mWcm^{-2} and λ = 532 nm. (a) Difference of photo-response in the FE and PE phase. (b) Photo-response difference between P3HT-FETs made with high k dielectric (PVA) and FE-dielectric PVDF-TrFE at 180 K. (c) Photo-response with variation in intensity of light showing different degree of retention. (d) Change in the photo-response with gate voltage showing the effect of tunable E_{dep} on I_{ph} in FE-FET. Reproduced with permission from Phys. Rev B, 85 (11), 115311.*

4.9 Conclusion

The studies described in this chapter highlight the correlation between interfacial polarization and the semiconductor charge transport in a PFET structure. Dielectric materials which fall in the broad class of ferroelectric (FE) and paraelectric (PE) materials were utilized to investigate the impact of its polar nature on the interfacial charge transport of the PFET. Different disorder mechanisms were observed for FE and PE dielectrics materials which have similar dielectric constant. The transport in FE-FETs clearly depends on polarization fluctuation, unlike the FETs with non-polar dielectrics where the dipolar induced energetic disorder is dominant. The evidence for this interpretation was arrived from the weak *T* dependence of different electrical parameters in the FE regime compared to the strongly activated behavior in the PE regime. Moreover, photo-carrier generation studies in the depletion mode of the FET provided a clear distinction in the transport phenomenon with the phase transition of the dielectric layer. The charge carriers in the FE-phase experience an additional interaction originating from the non-linear component of FE-polarization. The distinct features in the FE regime are then attributed to the considerable influence of dielectric polarization fluctuations, which dominates over conventionally observed intrinsic processes. This strong coupling between the charge carriers and the dielectric layer is confirmed from the *T* dependence Raman spectra measurements. Fundamental understanding of the dielectric influence on the charge transport will be a useful tool to overcome the limitations of PFET devices.

References

1. (a) Sirringhaus, H.; Brown, P. J.; Friend, R. H.; Nielsen, M. M.; Bechgaard, K.; Langeveld-Voss, B. M. W.; Spiering, A. J. H.; Janssen, R. A. J.; Meijer, E. W.; Herwig, P.; de Leeuw, D. M., Two-dimensional charge transport in self-organized, high-mobility conjugated polymers. *Nature* **1999,** *401* (6754), 685-688; (b) Kobayashi, S.; Nishikawa, T.; Takenobu, T.; Mori, S.; Shimoda, T.; Mitani, T.; Shimotani, H.; Yoshimoto, N.; Ogawa, S.; Iwasa, Y., Control of carrier density by self-assembled monolayers in organic field-effect transistors. *Nat Mater* **2004,** *3* (5), 317-322.

2. (a) Hamadani, B. H.; Gundlach, D. J.; McCulloch, I.; Heeney, M., Undoped polythiophene field-effect transistors with mobility of 1cm2V-1s-1. *Appl. Phys. Lett.* **2007,** *91*, 243512; (b) Sirringhaus, H.; Bird, M.; Zhao, N., Charge Transport Physics of Conjugated Polymer Field-Effect Transistors. *Adv. Mater.* **2010,** *22* (34), 3893-3898.

3. Hulea, I. N.; Fratini, S.; Xie, H.; Mulder, C. L.; Iossad, N. N.; Rastelli, G.; Ciuchi, S.; Morpurgo, A. F., Tunable Frohlich polarons in organic single-crystal transistors. *Nat Mater* **2006,** *5* (12), 982-986.

4. (a) Chang, J.-F.; Sirringhaus, H.; Giles, M.; Heeney, M.; McCulloch, I., Relative importance of polaron activation and disorder on charge transport in high-mobility conjugated polymer field-effect transistors. *Phys. Rev. B* **2007,** *76* (20), 205204; (b) Richards, T.; Bird, M.; Sirringhaus, H., A quantitative analytical model for static dipolar disorder broadening of the density of states at organic heterointerfaces. *J. Chem. Phys.* **2008,** *128* (23), 234905.

5. (a) Veres, J.; Ogier, S. D.; Leeming, S. W.; Cupertino, D. C.; Mohialdin Khaffaf, S., Low-k Insulators as the Choice of Dielectrics in Organic Field-Effect Transistors. *Adv. Funct. Mater.* **2003,** *13* (3), 199-204; (b) Panzer, M. J.; Frisbie, C. D., High Carrier Density and Metallic Conductivity in Poly(3-hexylthiophene) Achieved by Electrostatic Charge Injection. *Adv. Funct. Mat.* **2006,** *16* (8), 1051-1056; (c) Xia, Y.; Cho, J. H.; Lee, J.; Ruden, P. P.; Frisbie, C. D., Comparison of the Mobility–Carrier Density Relation in Polymer and Single-Crystal Organic Transistors Employing Vacuum and Liquid Gate Dielectrics. *Adv. Mat.* **2009,** *21* (21), 2174-2179.

6. Letizia, J. A.; Rivnay, J.; Facchetti, A.; Ratner, M. A.; Marks, T. J., Variable Temperature Mobility Analysis of n-Channel, p-Channel, and Ambipolar Organic Field-Effect Transistors. *Adv. Funct. Mater.* **2010,** *20* (1), 50-58.

7. Dhoot, A. S.; Yuen, J. D.; Heeney, M.; McCulloch, I.; Moses, D.; Heeger, A. J., Beyond the metal-insulator transition in polymer electrolyte gated polymer field-effect transistors. *Proc. Natl. Acad. Sci.* **2006,** *103* (32), 11834-11837.

8. Kang, S. J.; Park, Y. J.; Sung, J.; Jo, P. S.; Park, C.; Kim, K. J.; Cho, B. O., Spin cast ferroelectric beta poly(vinylidene fluoride) thin films via rapid thermal annealing. *Appl. Phys. Lett.* **2008,** *92* (1), 012921.

9. Naber, R. C. G.; Tanase, C.; Blom, P. W. M.; Gelinck, G. H.; Marsman, A. W.; Touwslager, F. J.; Setayesh, S.; de Leeuw, D. M., High-performance solution-processed polymer ferroelectric field-effect transistors. *Nat Mater* **2005,** *4* (3), 243-248.

10. Schultz, I.; Goebel, H.; Ullmann, M., Modelling polarisation of ferroelectric SBT capacitors including temperature dependence. *Electronics Letters* **2001,** *37* (20), 1216-1217.

11. Sheikholeslami, A.; Gulak, P. G., A survey of behavioral modeling of ferroelectric capacitors. *Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on* **1997,** *44* (4), 917-924.

12. Xia, F.; Xu, H.; Fang, F.; Razavi, B.; Cheng, Z.-Y.; Lu, Y.; Xu, B.; Zhang, Q. M., Thickness dependence of ferroelectric polarization switching in poly(vinylidene fluoride--trifluoroethylene) spin cast films. *Appl. Phys. Lett.* **2001,** *78* (8), 1122-1124.

13. Nguyen, C. A.; Lee, P. S.; Mhaisalkar, S. G., Investigation of turn-on voltage shift in organic ferroelectric transistor with high polarity gate dielectric. *Organic Electronics* **2007,** *8* (4), 415-422.

14. See supplementary materials at: for P-E curves, R. S., device schematic, conductivity and output curves.

15. Lovinger, A. J., Ferroelectric Polymers. *Science* **1983,** *220* (4602), 1115-1121.

16. Odajima, A.; Wang, T. T.; Takase, Y., An explanation of switching characteristics in polymer ferroelectrics by a nucleation and growth theory. *Ferroelectrics* **1985,** *62* (1), 39-46.

17. Fumagalli, L.; Binda, M.; Natali, D.; Sampietro, M.; Salmoiraghi, E.; Gianvincenzo, P. D., Dependence of the mobility on charge carrier density and electric field in poly(3-hexylthiophene) based thin film transistors: Effect of the molecular weight. *J. Appl. Phys.* **2008,** *104* (8), 084513.

18. eacute; rez-Garrido, A.; Ortu; ntilde; o, M.; Cuevas, E.; Ruiz, J.; Pollak, M., Conductivity of the two-dimensional Coulomb glass. *Phys. Rev. B* **1997,** *55* (14), R8630.

19. Dhoot, A. S.; Wang, G. M.; Moses, D.; Heeger, A. J., Voltage-Induced Metal-Insulator Transition in Polythiophene Field-Effect Transistors. *Phys. Rev. Lett.* **2006,** *96* (24), 246403.

20. (a) Meijer, E. J.; Tanase, C.; Blom, P. W. M.; Veenendaal, E. v.; Huisman, B.-H.; Leeuw, D. M. d.; Klapwijk, T. M., Switch-on voltage in disordered organic field-effect transistors. *Appl. Phys. Lett.* **2002,** *80* (20), 3838-3840; (b) Podzorov, V.; Menard, E.; Borissov, A.; Kiryukhin, V.; Rogers, J. A.; Gershenson, M. E., Intrinsic Charge Transport on the Surface of Organic Semiconductors. *Phys. Rev. Lett.* **2004,** *93* (8), 086602.

21. (a) Zen, A.; Pflaum, J.; Hirschmann, S.; Zhuang, W.; Jaiser, F.; Asawapirom, U.; Rabe, J. P.; Scherf, U.; Neher, D., Effect of Molecular Weight and Annealing of Poly(3-hexylthiophene)s on the Performance of Organic Field-Effect Transistors. *Adv. Funct. Mater.* **2004,** *14* (8), 757-764; (b) Joshi, S.; Pingel, P.; Grigorian, S.; Panzner, T.; Pietsch, U.; Neher, D.; Forster, M.; Scherf, U., Bimodal Temperature Behavior of Structure and Mobility in High Molecular Weight P3HT Thin Films. *Macromolecules* **2009,** *42* (13), 4651-4660.

22. Tashiro, K.; Kobayashi, M., Vibrational spectroscopic study of the ferroelectric phase transition in vinylidene fluoride-trifluoroethylene copolymers: 1. Temperature dependence of the Raman spectra. *Polymer* **1988,** *29* (3), 426-436.

23. Yuan, Y.; Reece, T. J.; Sharma, P.; Poddar, S.; Ducharme, S.; Gruverman, A.; Yang, Y.; Huang, J., Efficiency enhancement in organic solar cells with ferroelectric polymers. *Nat Mat.* **2011,** *10* (4), 296-302.

24. (a) Batra, I. P.; Wurfel, P.; Silverman, B. D., Phase Transition, Stability, and Depolarization Field in Ferroelectric Thin Films. *Phys. Rev. B* **1973,** *8* (7), 3257; (b)

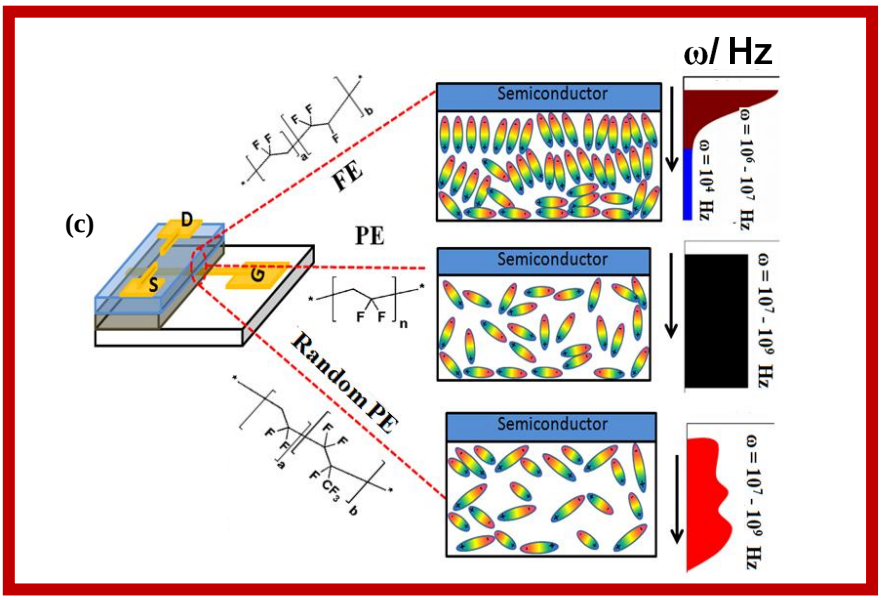
Wurfel, P.; Batra, I. P., Depolarization-Field-Induced Instability in Thin Ferroelectric Films—Experiment and Theory. *Physical Review B* **1973,** *8* (11), 5126.

25. Asadi, K.; Bruyn, P. d.; Blom, P. W. M.; Leeuw, D. M. d., Origin of the efficiency enhancement in ferroelectric functionalized organic solar cells. *Appl. Phys. Lett.* **2011,** *98* (18), 183301.

26. Dutta, S.; Narayan, K. S., Gate-Voltage Control of Optically- Induced Charges and Memory Effects in Polymer Field-Effect Transistors. *Adv. Mat.* **2004,** *16* (23-24), 2151-2155.

Chapter 5

Fast-switching Polymer Field Effect Transistors



Chapter 5

Fast-switching Polymer Field Effect Transistors

5.1 Introduction

The next important device parameter which needs to be addressed for realizing the applications envisaged for flexible electronics is the switching speed of the field effect transistors. Applications such as flexible RFID require enhanced switching speeds from these transistors. A general guideline for improving switching characteristics of polymer field effect transistors (PFETs) is based on the traditional MOSFET principle[1] where the switching-time scales as L^2/μ, (L is the channel length) [2]. Major efforts have been devoted to the design and synthesis of ordered systems and, in this endeavor, $\mu_{FET} \sim 3$ $cm^2V^{-1}s^{-1}$ has been achieved for both electron and hole transport[3].In parallel, sustained efforts have been made to decrease the channel length by different lithographic[4] and printing techniques to obtain significantly low switching time (t_{switch}) [5]. Apart from these factors, t_{switch} in PFETs is also affected by the relaxation processes occurring in the polymer dielectric layer ($t_{dielectric}$) and disorders at the semiconductor-dielectric interface ($t_{interface}$). An understanding of the different sources of contribution to the switching process in PFETs should enable design of high gain-bandwidth organic-circuits. In this direction, a variety of dielectric and semiconducting layers are studied to arrive at a working model for the PFET dynamics. The working model was then implemented to obtain PFETs with response time three order of magnitude higher than convention polymer devices. The highlight of this approach is that it is particularly suited for devices with channel dimensions which come under the realm of low-cost printing methods and is universally usable for different classes of disordered FE.

The switching study involved dielectric materials from the PVDF family which cover a wide class from low-*k* to high-*k* paraelectrics (PE) as well ferroelectrics (FE); and active semiconducting materials: hole conducting rr-P3HT (*p*-FET) and high electron transporting naphthalene diimide core N2200 (*n*-FET). These semiconducting polymers

differ in their stacking and crystallinity at the transport interface [6]. The conjugated core of P3HT stacks close to the dielectric interface whereas in N2200 the long branched 2-octyldecyl separates the conjugated core from the dielectric interface by a distance > 1 nm, thus modifying the static influence of the dielectric on the semiconductor.

These results obtained from the dynamic measurements of the PFETs fabricated from a range of dielectrics and semiconductors provide a rationale guideline to obtain high frequency (~ MHz) organic circuits. A tunable material parameter is obtained which can be used to modify the limiting processes in the switching response. And finally, with optimum material choice, improved device-dipole engineering and easy fabrication techniques ($L \approx$ 20 μm), an all-polymer-complementary inverter- circuit with voltage gain ~ 36 and switching response of 4 MHz (β-PVDF/N2200) was demonstrated.

5.2 Advantages in FE-FETs for dynamic response

The electrical transport in PFETs is controlled by energetic disorder and dielectric fluctuations at the semiconductor-dielectric interface which generally result in broadening of density of states. It was recently observed that some of these issues can be mitigated with the use of polar FE dielectric [7]. Polymer FE dielectrics are known to form structural and energetically ordered interface with activation energy (E_A) ~ 14 meV [7a]. Additionally, FE layer in PFETs enable large transverse fields at low gate voltage (V_g) in order to observe the pinch-off at lower V_{ds} [2, 8]. This aspect is significant in the case of PFETs where lowering channel length to short-channel regime introduces large deviation from ideal long-channel saturation behavior. It is generally accepted that channel length needs to be about four times the dielectric thickness to observe saturation behavior [5]. Microscopically ordered interface and high transverse field using a FE dielectric is expected to assist in improving the static and dynamic performance of PFETs. However, the large polarization in FE is associated with slow response to an external time varying electric field [9]. This slow component of the bulk FE relaxation limits the switching response ($t_{switch} \approx t_{dielectric}$) of FE-FET and hence the fastest response obtained till-date was 0.3 ms [10]. One of the approaches to overcome this limitation is by poling (electric-field induced orientation) the ferroelectric layer near ferroelectric transition temperature ($T_c \approx$ 390 K). Poling of FE layer is known to modify the relaxation process wherein the relaxation time decreases with higher magnitude of applied field[11]. This enhancement in the relaxation process of FE dielectric layer with poling is attributed to the fast domain nucleation and fast switching processes of disordered-FE dipoles[11]. This process is different from the switching dynamics obtained near the coercive

field for ultra-thin dielectric films[12]. In case of 2-D ultra thin films the switching time increases near the coercive field since the switching in these cases occur without the domain walls the co-operative motion of the FE dipoles is absent.

5.3 Device Fabrication and Characterization

Bottom gated top contact FETs were fabricated by coating patterned electrode-Al or Cr/Au (10^{-6} mbar, 1 Å/s, 30 nm thick) with a shadow mask on RCS cleaned glass substrates. Dielectric materials of thickness ~ 200 nm were coated by specific procedures (as described in section 2.3.3) which resulted in desired phases [7a] corresponding to FE, PE and random-PE (*r-PE*). Polymer active layers rr-P3HT and N2200 (~ 50 nm thick) were spin coated from a solution of 10 mg/ml in chlorobenzene at 1000 rpm. P3HT films were annealed at 110 °C for 30 minutes and N2200 films at 110 °C for 2 hrs. This was followed by the deposition of S-D patterned-aligned electrodes by shadow masking technique. Devices were fabricated with *L* varying from 5 µm - 250 µm and W = 1 mm.

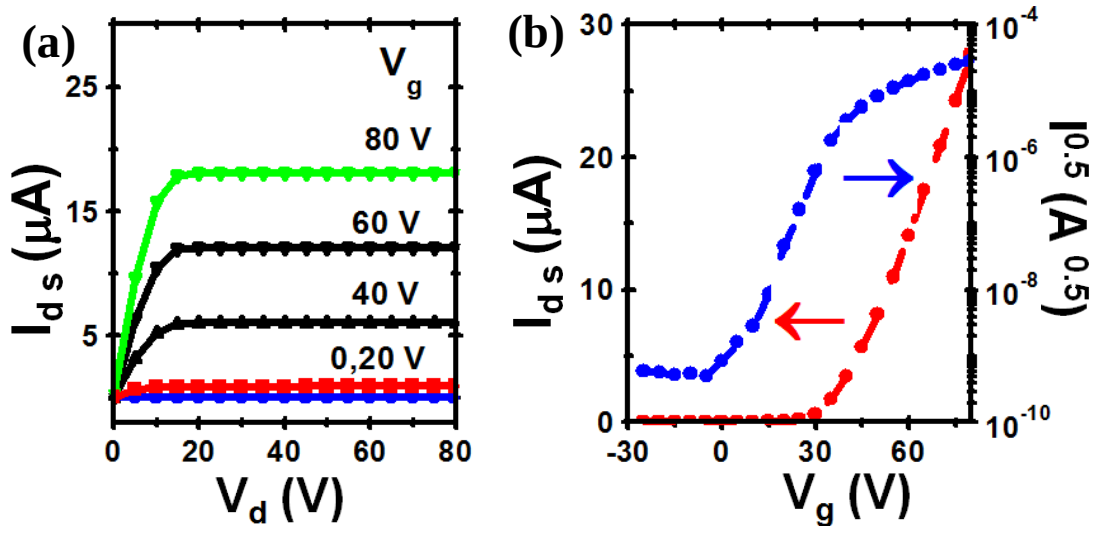


Figure 5.1: *Typical (a) Output and (b) transconductance curve obtained from n-type N2000-PFET (L = 40 µm and W = 1 mm) with β-PVDF dielectric layer (200 nm thickness). Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

All the PFETs were characterized by $I_{ds}(V_{ds}, V_g)$ (**Figure: 5.1a & b**) measurement with Keithley 4200 SCS prior to studying the dynamic characteristics. These devices demonstrated distinct saturation regime which is a pre-requisite for a good switching circuit. Drain current (I_{ds}) scaled linearly with *L*, indicating negligible contact resistance (~

0.5 - 5 % of channel resistance) in all the tested devices. In general, the PFETs demonstrate reliable leakage free transport with maximum hole mobility: μ_{FET}^{h} ~ 0.08 $cm^2V^{-1}s^{-1}$ in case of P3HT as the active layer and maximum electron mobility of μ_{FET}^{e} ~ 0.7 $cm^2V^{-1}s^{-1}$ for N2200. The ON-OFF ratios exhibited by the PFETs were typically in the range of 10^4 - 10^6. These estimates of device performance are comparable to the best values reported for these polymers [6a, 13]. More than 500 devices were tested for these studies and the results presented constitute the statistical mean of the measurement.

5.4 Gate Pulse Switching Response

5.4.1 Experiment

Typical $I_{ds}(\Delta V_g)$ behavior obtained in response to an input square gate-pulse (ΔV_g = |40| V) for a FE-FET fabricated with N2200 semiconductor is shown in **Figure: 5.2**. In order to extract the t_{switch}, following procedure was followed: $I_{ds}(\Delta V_g)$ was monitored in the OFF state and saturation regime, corresponding to V_d = 0 V and |80| V respectively (**Figure: 5.2b**). The OFF state transient originates from the parasitic capacitance of the semiconductor and dielectric layer due to overlapping electrodes while the ON state has the additional contribution of channel current. Transient profile was then estimated in terms of an effective current by taking the difference between the two recorded profiles. In this method, t_{switch} was evaluated as the time taken to completely switch on the PFET with ON/OFF ratio ~ 10^6 (**Figure: 5.2c**). It was ensured that the *RC* time-constant for external circuitry is 100 times lower than the response time of the PFETs. The entire duration to reach the ON state (100 % ≈ $I_{ds,sat}$) is a preferred definition for t_{switch} rather than the standard 90 % and 70 % fraction, so as to include factors originating from the dielectric fluctuation processes which is known to contribute a slow component in the $I_{ds}(t)$ profile[14]. The observed t_{switch} magnitudes were typically in the range of 400 ns to 100 μs and the time scale of dielectric fluctuation is significantly lower than t_{switch} (**Figure: 5.2c**). Contact resistance at the metal-semiconductor interface does not affect the t_{switch} significantly. This was evident from the linear variation of I_{ds} with *L* and the relatively long-channel lengths (5 μm – 250 μm) of the devices.

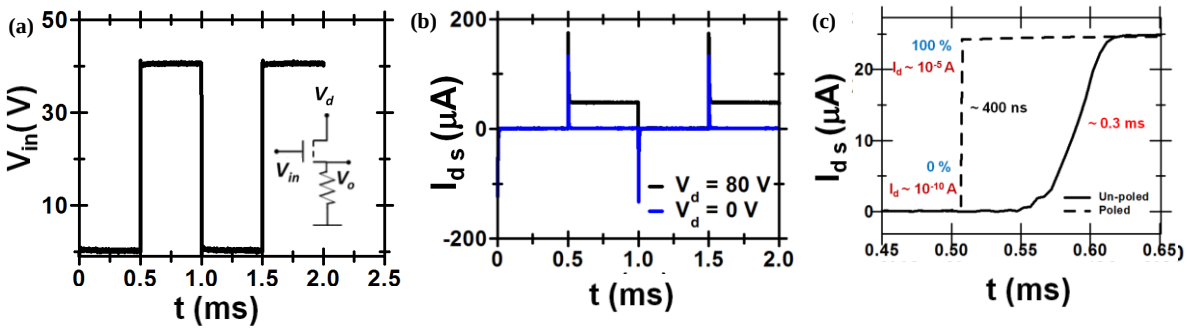


***Figure 5.2**: Switching behavior of a n-type N2200 based FE-FET (L = 20 μm and W = 1 mm) with β-PVDF (200 nm) dielectric layer in response to a square V_g pulse; (a) applied input gate voltage; (inset a) circuit schematic; (b) measured I_{ds} through the resistor (R ~1-10 KΩ) at V_{ds} = 80 V and V_{ds} = 0 V; (c) zoomed switching profile of I_{ds} indicating the manner in which "rise time: t_{switch}" was estimated and demonstration of the enhancement in t_{switch} after poling the interface for n-type N2200 based FE-FETs (L = 20 μm, W = 1 mm) with β-PVDF dielectric layer (200 nm). Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

5.4.2 Mechanism

The time required for switching the transistor completely, i.e. t_{switch} is determined by the carrier transit time ($t_{transit}$) between the electrodes unaffected by the interface disorder, dipole-orientation period of the dielectric layer ($t_{dielectric}$), interface energetic of the traps ($t_{interface}$) and the charging duration of the parasitic capacitors at the S-D-G overlap[2]. The time constant of the RC circuit constituted by the resistor in series with the parasitic capacitor (S-D-G overlap) for PFETs (< 0.5 pF) in the present study is relatively small and its influence can be neglected in these measurements. In a simple approximation, $t_{switch} \approx at_{transit} + bt_{dielectric} + ct_{interface}$, and a, b, c are weighted factors signifying the extent of contributions from each of the processes. t_{switch} variation with L for various dielectric and semiconductor combinations was obtained to understand switching dynamics. Typical $t_{switch}(L)$ response for different class of semiconductors and dielectrics is shown in **Figure: 5.3**. Expectedly, t_{switch} decreases with decrease in channel length of the PFETs, with a typical L^2 behavior. However, the L^2 behavior of t_{switch} is modified in the present case of FE-FETs, where it scales as L^{ϕ} with $\phi \sim 1.2 - 1.6$. This is similar to the trends observed in electrolyte and ionic liquid gated FETs [15] [2, 16]. Highlights of the switching response observed from different dielectrics and semiconducting polymers are as follows: (i) for FE-

FETs, $t_{switch}(L)$ varies as L^{ϕ} with $1.2 < \phi < 1.6$ at large L and becomes independent of channel dimensions upon downscaling; (ii) decrease in the t_{switch} from 300 µs to 400 ns in FE-FETs upon introducing the procedure of interface poling (iii) in case of PE-FETs, ϕ increases and approaches 2 with decrease in k (from α-PVDF: $k \sim 14$ to BCB: $k \sim 2.6$); (iv) in FETs with random co-polymer (*r*-PE) like PVDF-HFP dielectrics, ϕ significantly varies from 1.5 in the case of *p*-FETs to 1.8 – 2.0 when used with *n*-FETs.

5.4.3 FE-FET switching

A transition from power-law behavior to L independent behavior was observed in the switching response of FE-FETs with respect to L.

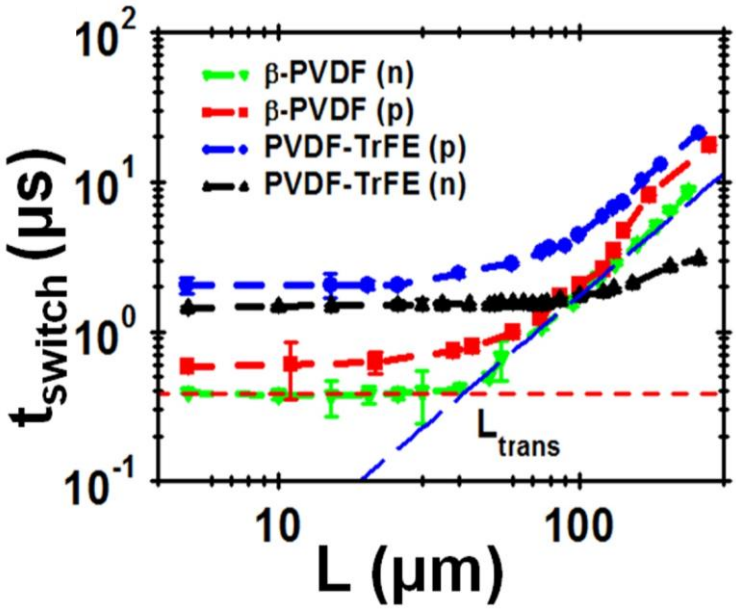


Figure 5.3: *$t_{switch}(L)$ in log-log scale for n-FETs (n) and p- FETs (p) with FE dielectric layers. Error bars indicate the mean deviation obtained from (3-5) devices at each channel length. For the sake of appropriate comparison across different class of materials, the thickness of dielectric and semiconducting layers were in the narrow range (200 ± 10) nm and (50 ± 5) nm respectively and W is 1 mm for all devices. In all the devices, parasitic capacitance from the electrode overlap was maintained at 0.5 pF. Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

t_{switch} being independent of L essentially implies that the switching response in this regime is controlled by the dielectric relaxation (i.e. $t_{switch} \approx t_{dielectric}$) and not by the transit time of charge carriers. The transition channel length (L_{trans}) is defined as the channel length where the transport time of charge carriers in the channel equals the dielectric

relaxation time. L_{trans} was obtained to be 25 µm in the case of PVDF-TrFE and 20 µm for β-PVDF based *n*-FETs (**Figure: 5.3**). Above L_{trans}, $t_{switch}(L)$ takes on a power law behavior and at sufficiently large L, t_{switch} can be expressed as an approximate sum of separate processes; $t_{switch} = at_{transit} + bt_{dielectric} + ct_{interface}$ ($t_{interface} << t_{transit}$ or $t_{dielectric}$). If the criterion of switching is specified to the 90% and 70% magnitude, then L_{trans} assumes a low value of < 5 µm.

It was observed that the exponent ϕ, obtained from $t_{switch} \sim L^{\phi}$ can be tuned by modifying the crystallinity of the FE layer (PVDF-TrFE). The crystallinity in the FE films were estimated from the relative peak intensity of the β-phase from FTIR spectra.

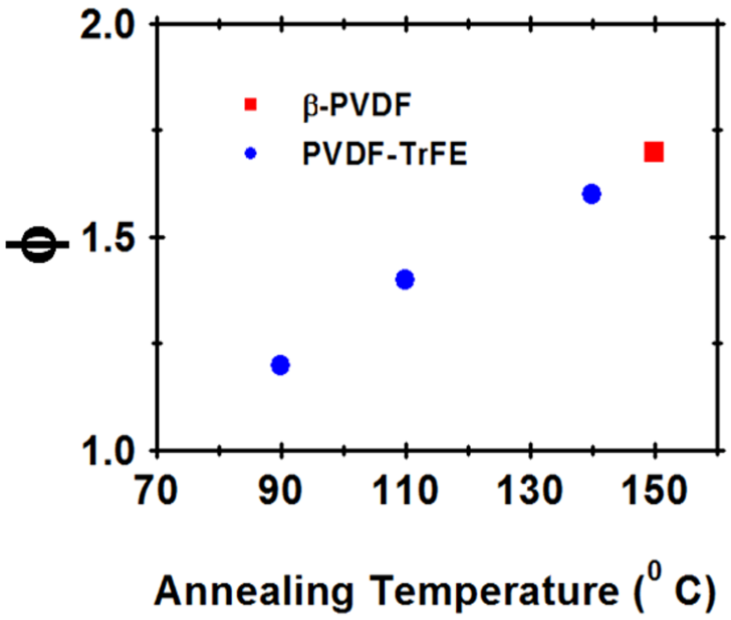


Figure 5.4: *Tuning the parameter φ (extracted from $t_{switch} \sim L^{\varphi}$) by modifying the dielectric layer with varied annealing conditions of the FE layer, which modifies the degree of crystallinity. All the measurements were performed on P3HT (50 nm) based PFETs (L in the range 5 µm to 250 µm and W = 1 mm) with the respective dielectric layer (200 nm). Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

FE-FETs fabricated with varied crystallinity (95% at annealing condition of 140 °C to 50% when annealed at 90 °C) of the FE-layer also followed similar trend in $t_{switch}(L)$ as seen in **Figure: 5.3**. However, a higher value of L_{trans} and slower response is obtained from these devices. It is known that switching of FE without domains is generally a slower process due to the absence of co-operative motion of dipoles [17]. Hence, the slow response

for FE layers with low crystallinity originates from: (i) combination of relaxation dynamics of differently aligned domains and grain boundaries; and (ii) slower dipole relaxation processes in the sizable amorphous regions. As the crystallinity of PVDF-TrFE layer in FE-FET decreased, the exponent ϕ in the $t_{switch}(L)$ dependence reduced from 1.6 to 1.4 (**Figure: 5.4**) . Therefore, the variation in ϕ is related to the dielectric related properties, relaxation processes and transport at the interface and not geometrical parameters like contact resistance or parasitic capacitance.

In the regime where t_{switch} is controlled by $t_{dielectric}$, the dynamic behavior can also be modified by the top molecular semiconductor layer. FE-FETs fabricated from β-PVDF dielectric layer ($L \approx 5$ μm < L_{trans}), showed an increase in t_{switch} from 400 ns to 600 ns when the polymer layer is changed from N2200 to P3HT (**Figure: 5.3**). This trend can be related to the depolarization effect of the semiconducting layer on the FE dielectric. Introduction of semiconducting layer on a FE induces depolarization [7a, 18] which disrupts the ordered and co-operative dipoles of the FE. This depolarization phenomenon can be qualitatively estimated using photocurrent (I_{ph}) profiles of the PFETs operating in depletion mode.

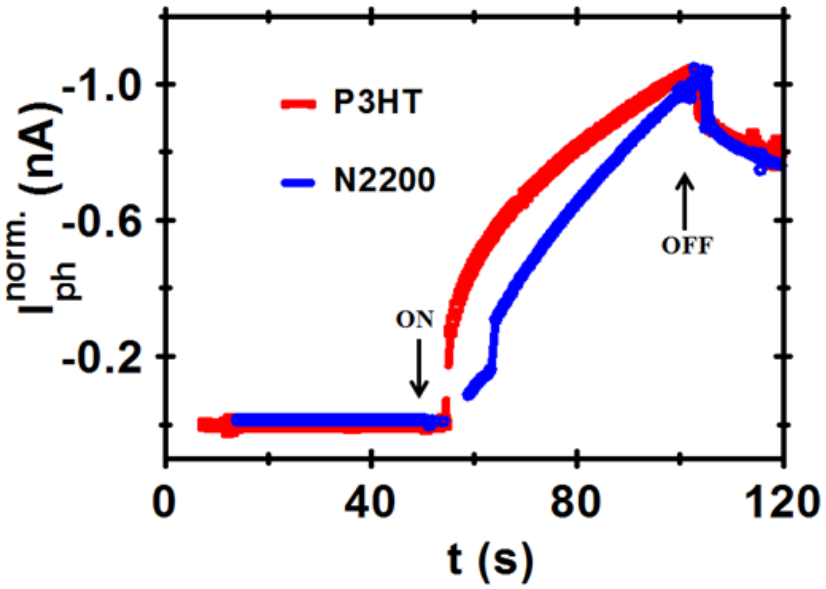


Figure 5.5: *Normalized I_{ph} (illuminated at λ = 543 nm) for n-FETs(N2200) and p-FETs (P3HT) with PVDF-TrFE dielectric layer. The PFETs (L = 80 μm and W = 1 mm) operate in the depletion regime (V_g = - 80 V for n-FET and 80 V for p-FETs) under finite V_{ds} = ± 40V and the experiment was performed at T ~ 180K. ON and OFF indicate beginning and end of illumination. Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

Slow response of the I_{ph} upon photo-excitation in FE-FETs is observed since a fraction of the photo-generated charge carriers are utilized to compensate the E_{dep}. It is observed that, for *n*-FETs with N2200 as active layer, the rise time of $I_{ph}(t)$ profile is lesser compared to P3HT based devices(**Figure: 5.5**). This indicates that the extent of depolarization induced by the N2200 layer is less compared to P3HT layer which can be directly related to the isolation of the polymer conjugated core from the FE layer by the alkyl side-chains[13]. Due to the minimization of the depolarization from the semiconductor the co-operative response of FE is retained to obtain better t_{switch} in case of FE-FETs fabricated with N2200 based semiconducting layer. In general, our results point to the fact that polymers with isolated core and edge-on arrangement should be preferred for fast switching.

5.4.4 Poling of FE dipoles

In case of FE-FETs, the semiconductor films coated on dielectrics were biased at ± 40V (for dielectric films of thickness 200 nm) with gold coated PDMS soft contacts for 30 minutes at T ~ 370 K under vacuum (10^{-3} mbar), before the coating of the S-D electrode. 40 V was chosen as the bias voltage since it corresponds to the polarization saturation (P_s) field for FE-films of 200 nm thickness.

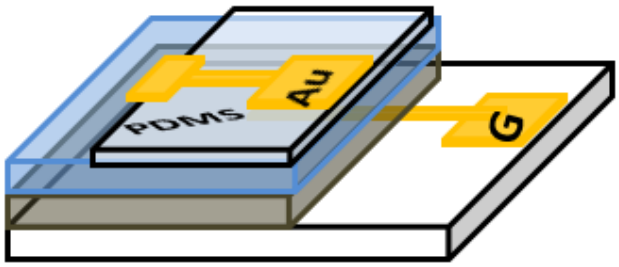


Figure 5.6*: Schematic of MFSM device set up for poling the FE layer. Grey region is the FE film, blue region is the semiconductor. Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

PDMS soft contacts were prepared by coating 1 µm thick gold film on (2 - 3) mm free standing PDMS substrate. Device with the FE and semiconducting layer was clipped with PDMS contacts completing the Metal Ferroelectric Semiconductor Metal (MFSM) structure (Schematic in **Figure: 5.6**). It was ensured that the MFSM structures were in accumulation mode with bias. The domain nucleation and growth rates were monitored and optimized by trials as shown in **Figure: 5.7**.

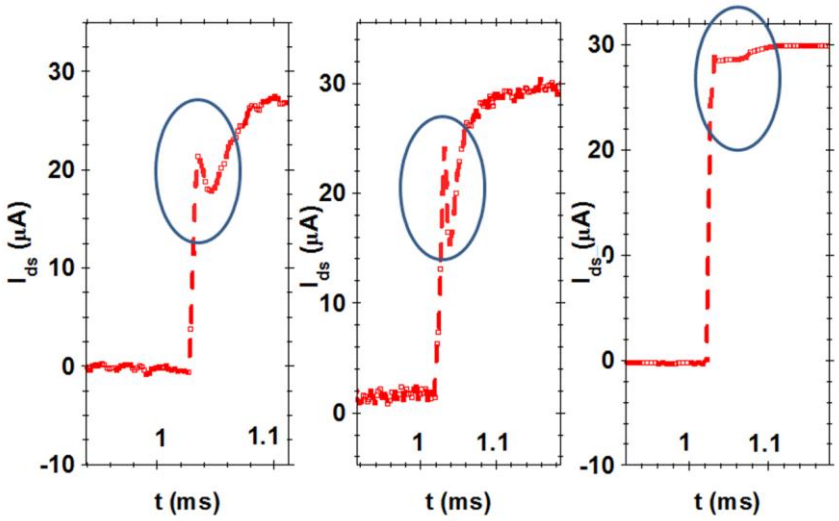


Figure 5.7: *Pulsed response of FE-FETs with incomplete domain nucleation indicating the presence of a slow time scale involved in the dynamic process. Measurements were performed on n-type N2200 based FE-FETs (L = 40 μm and W = 1 mm) with β-PVDF dielectric (200 nm) for a gate pulse voltage of 80V. Clean pulsed response without any slow component due to nucleation limited processes was observed in optimized devices by poling for 30 minutes at a T ~ 370 K. Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

FE-FETs (*β*-PVDF/N2200, *L* = 10 μm) fabricated with poled ferroelectric layers demonstrated an enhancement in the dynamic response from 300 μs to 400 ns which is evident in **Figure: 5.2c**. This poling induced enhancement in switching response is analyzed in terms of the intrinsic domain dynamics of FE-dielectric. In a polymer-FE dielectric the total time for polarization switching is governed by nucleation limited switching (NLS) which involves $t_{nucleation}$ the time taken for domain nucleation and $t_{relaxation}$ the response of the domains (dipoles thereof) to the field, i.e., $t_{dielectric,FE} = t_{nucleation} + t_{relaxation}$. Typically it is seen that the domain nucleation is the slowest step [17a]. Once the nucleation of domains occurs, further alignment and orientation is relatively fast due to the co-operative dipole motion in FE-dielectrics. The initial bias applied to the *MFSM* overcomes the slow domain nucleation step and the FE relaxation becomes dependent only on the domain relaxation. Hence, faster switching speeds are obtained for FE-FETs with pre-poled interfaces. This enhanced switching behavior due to the poling process is sustained till ~ 10^4 minutes when the device is continuously operated at 300 K under ΔV_g = *80 V or 40 V* and V_{ds} = *80 V*. It is also observed that poling for shorter duration does not complete the nucleation process and is reflected by a slow component in the switching

profile as shown in **Figure: 5.7**. It should be mentioned that FE-FETs (N2200 active layer, β-PVDF dielectric layer, L = 20 µm and W = 1 mm) fabricated using un-poled dielectrics typically exhibited slower response (~ 0.3 ms) similar to the earlier reported results [10]. This method of enhancing the polarization relaxation by pre-poling can be applied for any disordered FE films which follows nucleation limited switching mechanism [19].

5.4.5 Impedance Spectroscopy

Impedance spectroscopy was performed for both surface and bulk dipole of the dielectric materials.

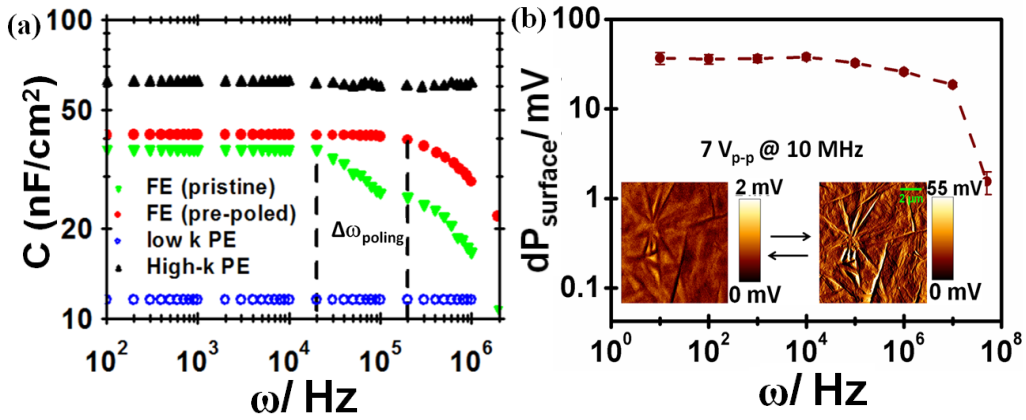


Figure 5.8: *(a) Bulk capacitance response from MIM devices for different dielectric layers (200 nm), $\Delta\omega_{poling}$ represents the change in frequency response of FE layer upon poling; (b) measurement of polarization contrast with frequency from SCM spectroscopy. Inset (b) is the representative polarization contrast (at 10 MHz) obtained from SCM measurements for PVDF-TrFE layer (200 nm) coated on ITO. Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014*

The response of the bulk dipoles was obtained by fabricating MIM capacitors (200 nm thick dielectric layer) with different dielectrics. It was observed that, in the case of low-k dielectrics, bulk capacitance (C) is largely independent of ω in the frequency range of 100 Hz - 1MHz range (**Figure: 5.8a**). However, in the case of FE capacitors (PVDF-TrFE), C is ω dependent and perceptibly decreases beyond 10^4 Hz. Upon applying the poling procedure, the ω-range extends beyond 10^5 Hz (**Figure: 5.8a)**. This variation in the $C(\omega)$ due to the poling procedure can be related to the aligned dipoles of the FE layer with bias[11].

In addition to the bulk dipoles, the surface dipoles contribute significantly to the effective polarization of a FE film. This becomes evident upon comparing the polarization retention (P_r) from FE layers of different thickness. The contribution from the surface dipoles was obtained by extrapolating the P_r variation to a zero thickness film. Following

this procedure the contribution of surface dipoles to the P_r was estimated for both β-PVDF and PVDF-TrFE dielectric films and is shown in **Figure: 5.9**.

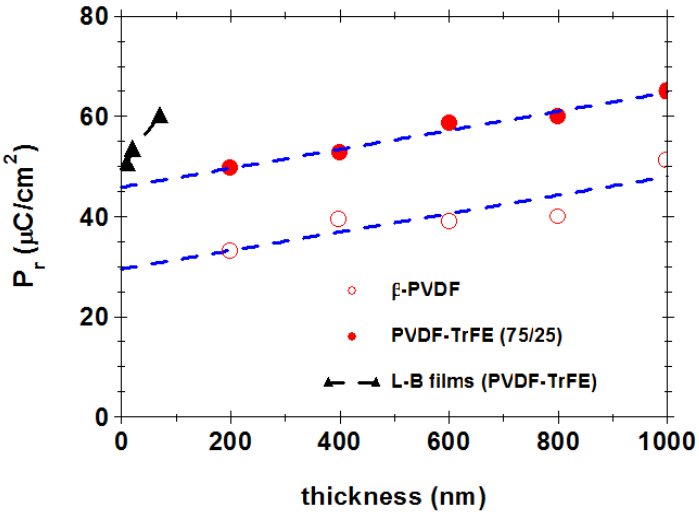


Figure 5.9: *Plot of P_r for films of different thickness obtained from spin coated or Langmuir-Blodgett (L-B) monolayer based FE in a MIM structure. The plot is extrapolated to obtain P_{surf}. Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

The dynamics of the surface dipoles of a FE films was monitored by scanning capacitance microscopy (SCM) measurements (**Figure: 5.8b**). Dielectric films grown on ITO coated transparent substrates were used for SCM characterization. Surface capacitance of the sample is obtained by using a Cr/Pt coated conducting tip (Multi-75E, Resonant frequency: ω_R = 75 kHz) which senses force proportional to surface capacitance variation (dC/dz). SCM retrace measures the capacitive force using lock-in amplitude at ω_R, while tip is driven at $\omega_R/2$ in hover mode (40 nm). To estimate the dipole response, poling of dielectric surface was performed using an in-built sinusoidal source (7 $V_{p\text{-}p}$) in the range of 100 Hz to 50 MHz applied through the tip. The connections to the device were impedance matched till 2 GHz. SCM was then performed on the biased area to measure the difference of electrostatic force (or the surface capacitance) with poling and obtain the average polarization contrast (dP). Frequency response of the surface dipoles was obtained as the frequency at which $dP/d\omega$ undergoes a slope change. SCM measurements showed that the surface impedance response of these poled FE films extends up to ~ 10 MHz (**Figure: 5.8b**). Hence, a distribution in the frequency response from 10^5 in the bulk to 10^7 in surface

exists along the cross-section of the pre-poled FE layers. The effective polarization response of a FE dielectric layer thus originates from the linear combination of $C(\omega)$ behavior from different layers.

5.4.6 Temperature dependent switching response

$t_{switch}(T)$ provides considerable insight into the switching mechanism. These measurements were performed for FE-FETs (**Figure: 5.10a & b**) with channel lengths: $L > L_{trans}$ and $L < L_{trans}$.

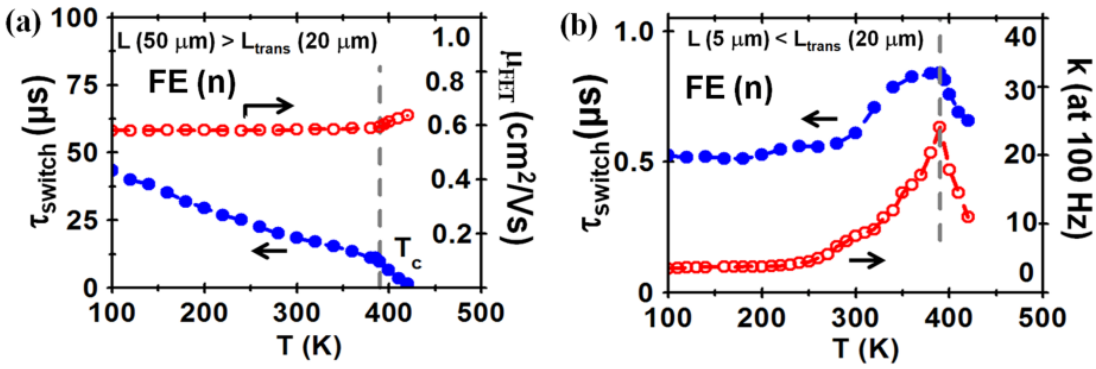


Figure 5.10: *Static and dynamic characterization with T for FE-FETs revealing the crossover behavior in switching mechanism. (a) $t_{switch}(T)$ and $\mu_{FET}(T)$ for n-type N2200 based FE-FETs with PVDF-TrFE dielectric (200 nm). (b) Small channel (L ~ 5 μm) $t_{switch}(T)$ response for FE-FETs from N2200 semiconducting layer (50 nm); also shown is the k(T) behavior for PVDF-TrFE in MIM structure. T_c (390 K) indicates the FE-PE phase transition in PVDF-TrFE. Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

Interestingly, the device response of FE-FETs varies significantly with channel length for both *n*-FETs and *p*-FETs. For devices with $L > L_{trans}$, $t_{switch}(T)$ follows an activated behavior similar to that of $\mu_{FET}(T)$ with low magnitude of E_A ~ 14 meV (**Figure: 5.10a**) [20]. However, in the devices with $L < L_{trans}$, $t_{switch}(T)$ follows a quadratic trend similar to $k(T)$ behavior (**Figure: 5.10b**). This proves that for FE-FETs with small L ($< L_{trans}$), the switching dynamics is primarily controlled by slow dielectric relaxation. It was also observed that beyond the phase transition of PVDF-TrFE from FE to PE phase at $T > T_c$, $t_{switch}(T)$ becomes activated for all L values with E_A ~ 0.4 eV. These T dependent measurements give a clear evidence of the change in switching mechanism for FE-FETs from dielectric limited processes to semiconductor transport limited processes.

5.4.7 PE-FET switching

For PE dielectrics (α- PVDF), t_{switch} could be fitted with exponent $\phi \sim 2$ in the complete range of L for both *n*-FETs and *p*-FETs as shown in **Figure: 5.11a**. Devices fabricated from these dielectrics have characteristic time scales as: $t_{dielectric}$ (10^{-9} secs) << $t_{transit}$ and $t_{switch} \approx t_{transit} + t_{interface}$ (for $L \geq 5$ µm). In general, t_{switch} for high-*k* PE based PFETs is lower than pre-poled FE-FETs. This behavior can be directly correlated to the ordered interface obtained with FE dielectrics compared to high-*k* PE-FETs. Additionally, even though the magnitude of *k* does not vary significantly between PVDF-HFP ($k \approx 13.5$) and α-PVDF ($k \approx 14$), the switching response for PVDF-HFP ($t_{switch} \approx 250$ µs) based *p*-FETs is observed to be slower than α-PVDF ($t_{switch} \approx 120$ µs). This is because of the heterogeneous molecular dipoles at the transport interface in *r*-PE based PFET which have distinctively different response time. These random dipoles can substantially contribute to the interface disorder affecting the charge transport and the associated dynamics. Additional clue for the dominance of interface dynamics in the switching response of PFETs fabricated with *r*-PE dielectric layer comes from different values of exponent ϕ for different semiconductors. The magnitude of ϕ attains a value of 1.8 - 2 for N2200 whereas it takes a value of 1.5 for P3HT based PFETs. This is because in N2200 the conjugated core is decoupled from the dielectric induced dipolar disorder due to the long alkyl chains attached to the conjugated core. Hence switching in *n*-FETs is weakly affected by the interface disorder from the dielectric layer compared to *p*-FETs.

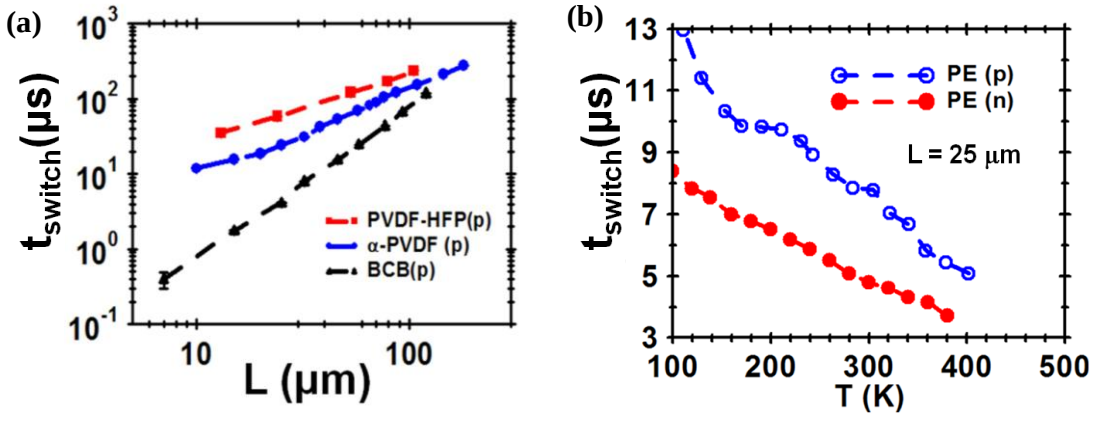


Figure 5.11: *Dynamic response of PE-FETs fabricated with N2200 (n) and P3HT (p) active layer. (a) t_{switch}(L) in log-log scale with PE dielectric layers; (b) t_{switch}(T) for PFETs with α-PVDF (200 nm) dielectric. Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

It is also observed that in the case of PE-FETs dielectric layer plays a minimal role and $t_{switch}(T)$ exhibits an activated behavior which is identical to $\mu_{FET}(T)$ [7a]. The limiting mechanism for switching in these PFETs is the transit time of the charge carriers between the electrodes (i.e. $t_{switch} \approx t_{transit}$). The magnitude of E_A estimated from $t_{switch}(T)$ for N2200 devices is in the range of 47 – 62 meV which is marginally lower than that of P3HT based devices (81- 120 meV) (**Figure: 5.11b**). In case of FETs fabricated with *r*-PE dielectric layer, the observed lower value of t_{switch} originates from low mobility which translates to a higher magnitude of E_A ~ 150 meV (PVDF-HFP/P3HT based PFETs). These analyses highlight the inherent differences in the transient response for various classes of PE dielectrics and the role of semiconductor.

5.5 Drain Pulse Switching Response

Drain pulse voltage in the presence of finite V_g introduces a transient drain current with characteristic profiles which depend on the transport mechanisms. The presence of a finite V_g ensures that the dielectric factors minimally contribute to the transient response. Typical drain-transient profile in response to a square-drain-pulse is shown in **Figure: 5.13a** (β-PVDF/N2200 based PFET). The transient switching time (t_{ds}) is obtained from the effective drain current by taking the difference between the two recorded profiles obtained in the ON (V_g = 80 V) and OFF state (V_g = 0 V) of the PFET in the presence of a pulsed ΔV_{ds} = |80| V or |40| V.

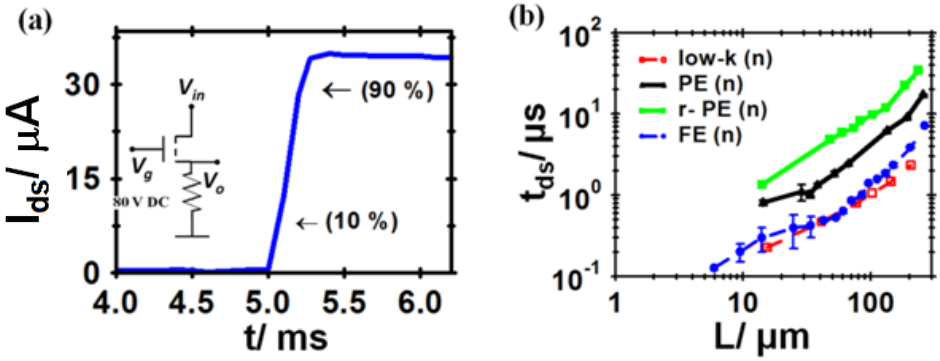


Figure 5.12: *Drain transient response (t_{ds}) for different dielectrics in n-FETs. (a)Typical response for N2200 based FE-FET (L = 60 µm and W =1 mm) with β-PVDF dielectric layer (200 nm). Inset shows the circuit diagram. (b) $t_{ds}(L)$ for n-FETs fabricated from different dielectric layers. Parasitic capacitance from the electrode overlap was maintained at ~ (0.5± 0.1) pF for all L values and W = 1 mm for all devices. Error bars indicate the mean deviation obtained from (3-5) devices at each channel length. Similar analysis was performed for p-FETs with P3HT as active layer. Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

The time required for switching-on the drain current at a constant V_g is determined by the transit delay time of charge carriers ($t_{transit}$) and the charging duration of the semiconductor sheet capacitor governed by the interface conductivity [21]. Simulation of the dynamic electric field distribution in the device during the transient measurement is shown in **Figure: 5.12**. This dynamic response was arrived at by solving the Poisson's equation and drift-diffusion model under appropriate boundary conditions of an operating FET (**Figure: 5.12**).

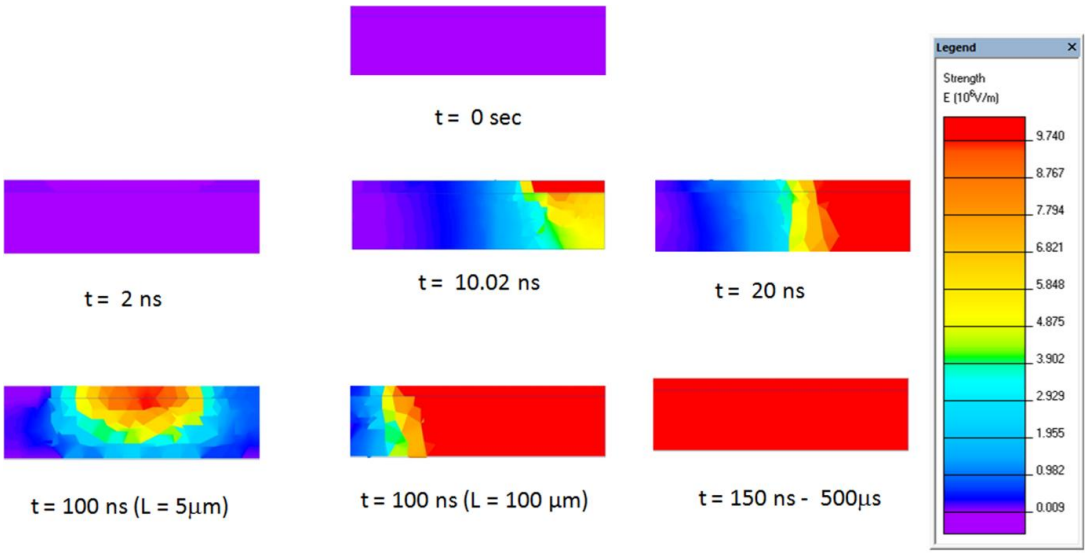


Figure 5.13: *Simulation of electric field distribution at different time duration when drain-source is pulsed at V_g = |80 V| and V_d = |80 V|. The device is a top-contact bottom gate structure with L = 10 μm and W = 1 mm. Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

Complete analysis of the dynamic response obtained from varied V_{ds} and V_g bias brings out the factors contributing to t_{ds}. In a simplistic approach, $t_{ds} \approx t_{transit} + t_{interface}$ with appropriate weighted factor for each process. To distinguish the interface dynamics of different dielectrics and semiconductors, t_{ds} was measured with varying channel lengths (**Figure: 5.13b)** and fitted as a power law (L^{δ}). It is expected that $t_{ds} \sim L^2$ for devices involving lateral transit of charge carriers [22]. If the introduction of dielectric layer (of PFET) does not significantly affect the lateral transport in the semiconductor then the square law behavior is retained. So, PFETs fabricated from low *k* dielectrics with an ordered interface followed L^2 dependence. Similarly, in the case of FE-FETs with ordered transport interface (E_A = 14 meV for PVDF-TrFE/P3HT transistor) typical L^2 response was

obtained. However, if the dielectric layer introduces disorder in the semiconductor a deviation from L^2 behavior is seen.

$t_{ds}(L)$ indicated a trend of lower δ value with increase in k of the dielectric layer and lowest value of δ ($\approx$ 1.6) was obtained for PFETs using r-PE as dielectric layer. Additionally, it was also seen that treatment of SAM layers like HMDS on the dielectric surface modifies the interface and δ increases (from 1.5 to 1.7 for r-PE/P3HT devices). From these measurements, it can be concluded that the value of δ is a measure of disorder at the interface with lower value implying higher degree of interface disorder. This can be understood from the fact that, as L increases the spatial access to disordered sites in the semiconductor increases. Hence, more traps needs to be filled up to attain channel conduction. So for a disordered interface weaker dependence of L is obtained. Activation energy ($E_{A,DC}$) estimation independently obtained from the T dependent DC transconductance measurement followed a trend similar to the variation of the parameter δ (**Figure: 5.14a & b**). It was interesting to observe that the lowest δ value was obtained for r-PE based PFETs indicating maximum interfacial disorder. The origin of high degree of disorder in r-PE based PFETs can be attributed to the existence of randomly oriented heterogeneous dipoles at the transport interface. In summary, all the above observations corroborates that the variation of δ has no contribution from geometric parameters due to electrode overlap or contact resistance rather correlates directly to the interface energetics.

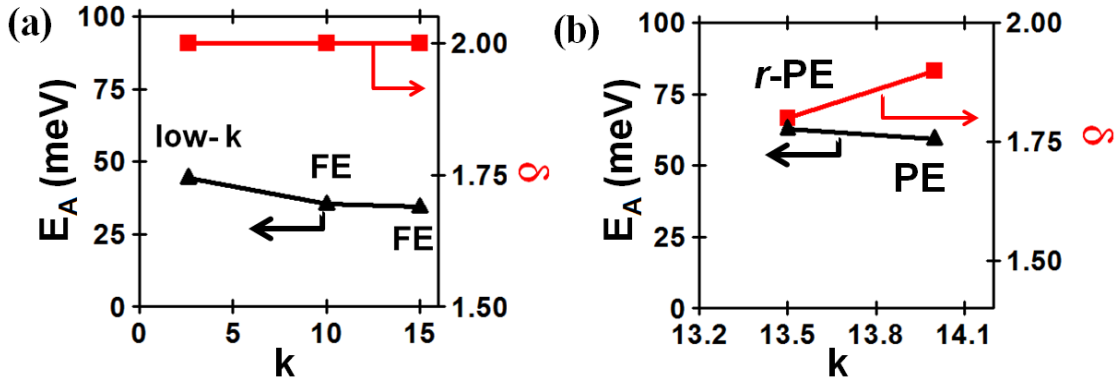


Figure 5.14: *Plot of E_A and the interface parameter (δ) with k for different dielectrics. δ is extracted from power law fits to $t_{ds}(L)$,i.e., $t_{ds} \sim L^{\delta}$. (a) Plot showing low degree of interface disorder which corresponds to $\delta \approx 2$ obtained in the case of both low-k and FE dielectrics. (b) Plot showing correlation between E_A and δ for α-PVDF(PE) and PVDF-HFP (r-PE) dielectric based FET. Similar behavior is observed for p-FETs with different class of dielectrics as well. Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

5.6 Analysis of Interface Parameters

Further insight into the wide range of results can be obtained from the exponent-parameter ϕ (obtained in **section 5.4.3:** $t_{switch} \sim L^{\phi}$) whose magnitude is indicative of the limiting processes. Our analysis shows that ϕ is dependent on μ_{FET}, $E_A(\delta)$ and $\omega_{dielectric}$, (= $1/t_{dielectric}$) as shown in **Figure: 5.15**. The trends in ϕ over a range of materials can map the dynamic response of PFETs which can be used as a figure of merit for switching behavior of PFETs. This parameter for different combination of dielectric and semiconductors is summarized in **Figure: 5.15**. The graph summarizes that, for any class of polymers if the PFET structure uses a low-*k* dielectric, then the switching dynamics is transport limited. If FE dielectrics are used, a dielectric dependent behavior is obtained and for devices with high-*k* dielectric layer, interface disorder limits the switching performance.

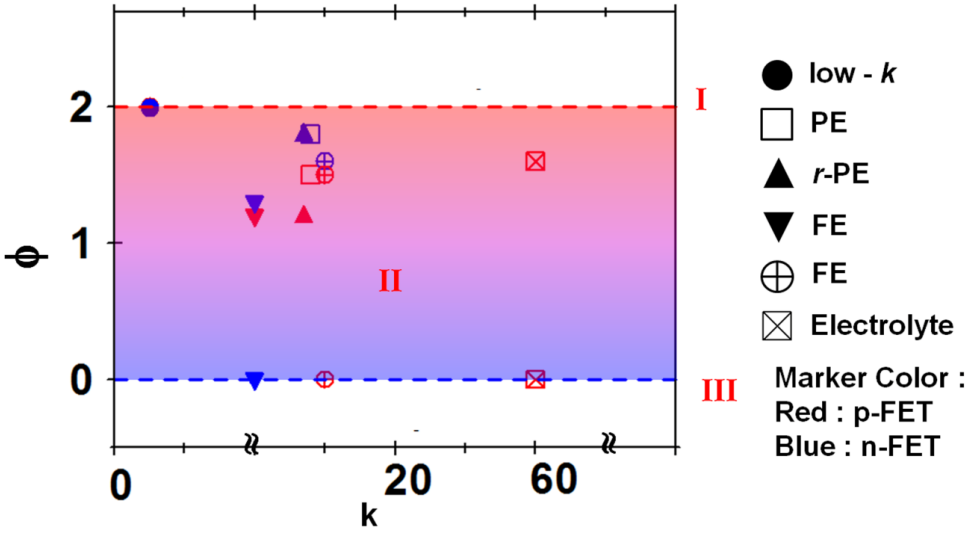


Figure 5.15 : *Universal map of dynamic response from the plot of parameter ϕ (extracted from $t_{switch} \sim L^{\phi}$) for different materials. Regime I (ϕ = 2) corresponds to semiconductor transport limited dynamics ($t_{switch} \approx t_{transit}$), regime III ($\phi$ = 0) corresponds to dielectric relaxation limited switching mechanism ($t_{switch} \approx t_{dielectric}$), region II (1< ϕ < 2) corresponds to the contribution from all the factors ($t_{switch} = at_{transit} + bt_{dielectric} + ct_{interface}$). Error bars indicate mean deviation from 3 sets of measurements. Electrolyte response is obtained from reference 3. Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

t_{switch} of PFETs can be expressed as a sum of independent physical processes. So, $t_{switch} = at_{transit} + bt_{dielectric} + ct_{interface}$. The weighted factors are introduced since each of the

processes are not completely independent of each other. Empirically, $t_{transit}$ and $t_{interface}$ which depend on the interface properties can be expressed as,

$$t_{transit} \approx \frac{2\pi L^2}{\mu_{FET} V_d} \qquad \text{……..(5.1)}$$

$$t_{interface} \approx \frac{2\pi L^{\delta}}{k'(\chi+1)(V_g - V_t)^2} \qquad \text{……..(5.2)}$$

where k' is related to the ease of hopping, which gives the interfacial properties (like interfacial roughness, interface width due to de-mixing and polymer film morphology on the dielectric), χ is related to the characteristic temperature T_0 which gives the broadening of density of state. k' and χ were used as free parameters in the fitting of $t_{switch}(L)$ using the empirical relationships. It is possible to combine together $t_{transit}$ and $t_{interface}$ to obtain a single time scale for transport. However, the possibility to distinguish different class of materials becomes more evident by separating the time scales for semiconductor transport ($t_{transit}$) and interface related properties originating from the modification of the interface due to polarity of the dielectric layer ($t_{interface}$). The expression for $t_{interface}$ is derived directly by assuming a power law dependence of μ_{FET} and charge density and also considering the dipolar induced disorder at the interface. In the expression, the parameter χ obtained from the dynamic measurements and given by:

$$\chi = \frac{T_o}{T} - 1 \qquad \text{……..(5.3)}$$

Similalrly,

$$k' = \left[\frac{e^2}{kT} f(\chi)\right] \xi N_t^{\frac{1}{3}} \eta^{(-3\chi+3)} \qquad \text{……..(5.4)}$$

was used to obtain the frequency of hopping ξ and the effective wave function overlap parameter η, which is proportional to the disorder at the transport interface and the σ of the polymer.

In general, $t_{dielectric}$ is independent of L for PE and low-k dielectrics due to random distribution of dipoles. However, in the case of FE dielectrics, $t_{dielectric}$ is expected to vary with L. This relaxation dynamics of FE can be expressed empirically as a modified form of Merz's law:

$$t_{dielectric} = \sum t_{\infty} \exp\left(-\frac{\gamma}{\boldsymbol{E}}\right) f(T)\, f(\boldsymbol{E}_{dep}) \qquad \text{……..(5.5)}$$

where t_{∞} is the ultimate switching speed of domains and dipoles, *E* is the applied field, γ is the activation field, *f(t)* is the distribution function of the dipole relaxation time and $f(E_{dep})$ is the measure of the depolarizing effect on the FE layer. This explains the role of domain distribution, depolarizing field and response of FE dipoles to the applied bias. The values obtained from the fit of $t_{switch}(L)$ compare well with the trends in the σ of N2200 and P3HT active layer. k' and χ which are related to interfacial properties and extracted from dynamic measurements match E_A and μ_{FET} obtained from DC transconductance measurements. A small deviation in the fitting parameters originates since, the weight factors *a*, *b*, *c* in the empirical relation were not considered for fitting. Nevertheless, these parameters give inherent evidence for the consistency of the empirical relation.

Table 1. *Parameters extracted from fitting of t_{switch} (L) and transconductance measurements of PFETs with different dielectrics and semiconductors. Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

Polymer	Dielectric	$k' \times 10^{-9}$ (cm^2/s)	χ	E_A (meV)	μ_{FET} ($cm^2V^{-1}s^{-1}$)
P3HT	BCB	4.48	1.25	56	0.08
	α - PVDF	1.16	1.66	86	0.014
	PVDF-HFP	0.632	1.75	116	0.04
N2200	BCB	6.57	1.2	45	0.5
	α - PVDF	2.07	1.46	60	0.12
	PVDF-HFP	1.84	1.5	63	0.15

5.7 Dynamic characterization of all polymer inverters

Complementary inverters were fabricated as top-contact bottom gate architecture with P3HT as the *p*-channel and N2200 as the *n*-channel. For demonstrating all polymer

circuits PEDOT:PSS (EL 3145 from Orgacon Transparent Conductive Screen printing Ink with $R_s \approx 240\ \Omega/\square$) was used as electrodes. To improve the noise margin width of the electrodes were varied in the range of (0.5 - 3) mm. It was ensured that the fabrication of one transistor does not affect or degrade the performance of the other transistor. Interconnects between the transistors were coated by thermal evaporation of Au after the fabrication of individual transistors. Channel width of the load (W_L) and driver (W_D) PFETs were varied and ratio of W_L/ W_D was maintained in the range of ~ 1 - 6. Inverters were characterized by using two Keithley 2400 source meter for V_{in} and V_{dd}. V_{out} was obtained using high impedance Keithley 6514 Electrometer for different values of V_{in}, in both hole (V_{dd} and $V_{in} < 0$) and electron transport regime (V_{dd} and $V_{in} > 0$), with P3HT and N2200 transistors as the load respectively (**Figure: 5.16a**). Typical voltage gain of 35 was obtained when *n*-FETs were used as load and 15 when *p*-FETs were used as load with FE dielectric *β*-PVDF. Interestingly the gain curves indicate less influence of the dielectric layer when *n*-FETs are used as load. It should be noted that gain of an inverter is related to the sub-threshold slope of the transistor and better threshold characteristics are obtained for a trap free transport interface. Hence, the relative independence of voltage gain on the dielectric layer could be related to the trap free transport in N2200 and isolated conjugated core from the static disorder.

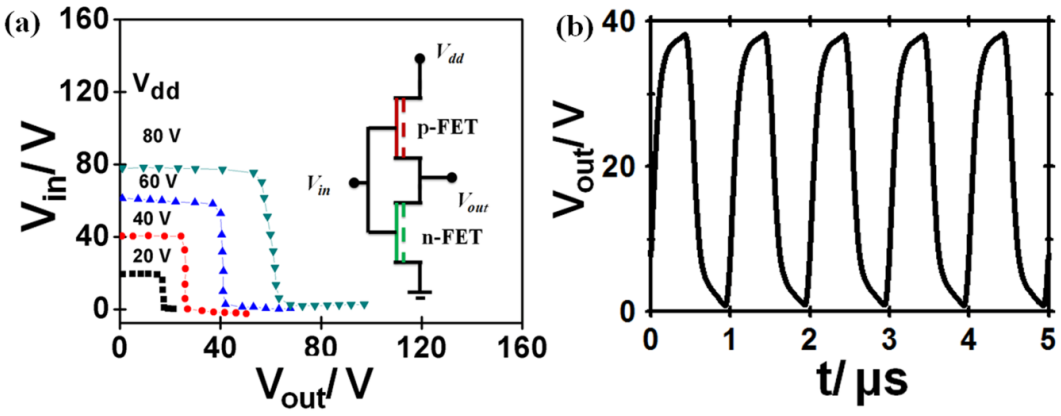


Figure 5.16: *Static and dynamic characterization of polymer inverters (L = 5 μm and W = 1 mm) with N2200 (50 nm) based n-FETs as load and P3HT (50 nm) based p-FETs as driver. (a) Typical transfer voltage curve with β-PVDF (200 nm) as the dielectric layer. Inset shows the schematic electrical connections. (b) Switching response of the same inverter at input frequency (ω_{in}) of 1 MHz and V_{dd} = 40 V. These curves represent that the devices can be operated at even higher frequency. Similar curves were also obtained from different dielectrics and also with p-FETs as load. Reproduced with permission from Advanced Functional Materials, 24 (22), 3324-3331,2014.*

To obtain the maximum switching frequency, square pulses of different frequency were applied and the output was monitored using Lecroy 6100A Oscilloscope (input capacitance of 5.5 pF). The cut-off frequency is the frequency above which the output signal does not completely follow the input signal. Optimized device geometry and interface parameters were utilized to obtain all-polymer complementary circuits operating at 4 MHz frequency (**Figure: 5.16b**), which is the best response obtained till date. Such high frequency response (~ 4 MHz) for all-polymer logic circuits opens up opportunities for more complex electronic architectures with polymers.

5.8 Conclusion

In conclusion, this chapter summarizes the strategies to obtaining fast-switching printable low-cost PFETs by understanding the limiting factors in the switching mechanism. Dynamic response of PFETs is a manifestation of time scales originating from processes such as dielectric polarization, structural relaxation and transport via disordered-interfacial states. Transport measurements from a range of dielectric and semiconducting materials demonstrate the possibility of systematic control and enhancement in the switching response of PFETs by dipole and device engineering. These strategies were implemented to obtain an enhancement of switching speed by three orders of magnitude (from 300 μs to 400 ns) at channel lengths which can be accessed by low cost printing methods. Thus, the prerequisites for fast switching polymer circuits include: polymers with higher conductivity and isolated conjugated core, dielectric layer which supports high transverse field and co-operative dipole switching, and optimum disorder free interface. Implementing these requisites all polymer complementary logic circuits with switching frequency > 1 MHz were demonstrated. This method of enhancing the switching speed of PFETs is universally applicable to all classes of disordered ferroelectric (FE) materials and broadens the utility of solution processable disordered materials to obtain faster printed circuits.

References

1. (a) Klauk, H., Organic thin-film transistors. *Chem. Soc. Rev.* **2010,** *39* (7), 2643-2666; (b) Sekitani, T.; Yokota, T.; Zschieschang, U.; Klauk, H.; Bauer, S.; Takeuchi, K.; Takamiya, M.; Sakurai, T.; Someya, T., Organic Nonvolatile Memory Transistors for Flexible Sensor Arrays. *Science* **2009,** *326* (5959), 1516-1519.

2. Herlogsson, L.; Noh, Y.-Y.; Zhao, N.; Crispin, X.; Sirringhaus, H.; Berggren, M., Downscaling of Organic Field-Effect Transistors with a Polyelectrolyte Gate Insulator. *Adv. Mat.* **2008,** *20* (24), 4708-4713.

3. (a) Kanimozhi, C.; Yaacobi-Gross, N.; Chou, K. W.; Amassian, A.; Anthopoulos, T. D.; Patil, S., Diketopyrrolopyrrole–Diketopyrrolopyrrole-Based Conjugated Copolymer for High-Mobility Organic Field-Effect Transistors. *J. Am. Chem. Soc.* **2012,** *134* (40), 16532-16535; (b) Hamadani, B. H.; Gundlach, D. J.; McCulloch, I.; Heeney, M., Undoped polythiophene field-effect transistors with mobility of 1 cm[sup 2] V[sup -1] s[sup -1]. *Appl. Phys. Lett.* **2007,** *91* (24), 243512.

4. (a) Di, C.-a.; Yu, G.; Liu, Y.; Xu, X.; Song, Y.; Wang, Y.; Sun, Y.; Zhu, D.; Liu, H.; Liu, X.; Wu, D., Noncoplanar organic field-effect transistor based on copper phthalocyanine. *Appl. Phys. Lett.* **2006,** *88* (12), 121907; (b) Wang, J. Z.; Zheng, Z. H.; Sirringhaus, H., Suppression of short-channel effects in organic thin-film transistors. *Appl. Phys. Lett.* **2006,** *89* (8), 083513.

5. Noh, Y.-Y.; Zhao, N.; Caironi, M.; Sirringhaus, H., Downscaling of self-aligned, all-printed polymer thin-film transistors. *Nat Nano* **2007,** *2* (12), 784-789.

6. (a) Sirringhaus, H.; Brown, P. J.; Friend, R. H.; Nielsen, M. M.; Bechgaard, K.; Langeveld-Voss, B. M. W.; Spiering, A. J. H.; Janssen, R. A. J.; Meijer, E. W.; Herwig, P.; de Leeuw, D. M., Two-dimensional charge transport in self-organized, high-mobility conjugated polymers. *Nature* **1999,** *401* (6754), 685-688; (b) Rivnay, J.; Toney, M. F.; Zheng, Y.; Kauvar, I. V.; Chen, Z.; Wagner, V.; Facchetti, A.; Salleo, A., Unconventional Face-On Texture and Exceptional In-Plane Order of a High Mobility n-Type Polymer. *Adv. Mat.* **2010,** *22* (39), 4359-4363; (c) Schuettfort, T.; Huettner, S.; Lilliu, S.; Macdonald, J. E.; Thomsen, L.; McNeill, C. R., Surface and Bulk Structural Characterization of a High-Mobility Electron-Transporting Polymer. *Macromolecules* **2011,** *44* (6), 1530-1539.

7. (a) Senanayak, S. P.; Guha, S.; Narayan, K. S., Polarization fluctuation dominated electrical transport processes of polymer-based ferroelectric field effect transistors. *Phys. Rev. B* **2012,** *85* (11), 115311; (b) Guo, Y.; Yu, G.; Liu, Y., Functional Organic Field-Effect Transistors. *Adv. Mat.* **2010,** *22* (40), 4427-4447.

8. (a) Klauk, H.; Zschieschang, U.; Pflaum, J.; Halik, M., Ultralow-power organic complementary circuits. *Nature* **2007,** *445* (7129), 745-748; (b) Yoon, M.-H.; Facchetti, A.; Marks, T. J., σ-π molecular dielectric multilayers for low-voltage organic thin-film transistors. *Proc. Natl. Acad. Sci. USA* **2005,** *102* (13), 4678-4682.

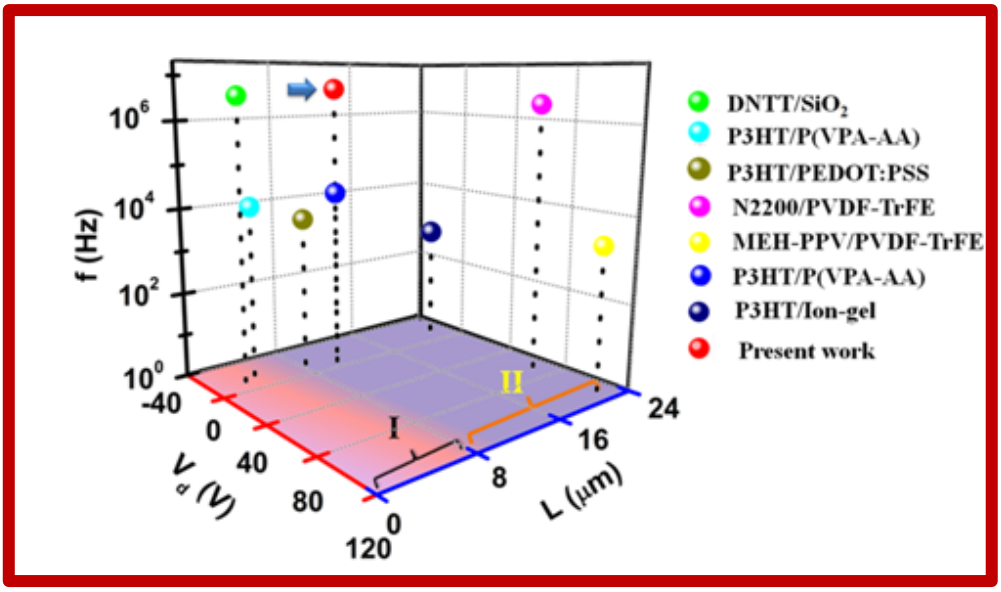
9. (a) Kang, S. J.; Park, Y. J.; Bae, I.; Kim, K. J.; Kim, H.-C.; Bauer, S.; Thomas, E. L.; Park, C., Printable Ferroelectric PVDF/PMMA Blend Films with Ultralow Roughness for Low Voltage Non-Volatile Polymer Memory. *Adv. Funct. Mat.* **2009,** *19* (17), 2812-2818; (b) Park, Y. J.; Kang, S. J.; Park, C.; Kim, K. J.; Lee, H. S.; Lee, M. S.; Chung, U.-I.; Park, I. J., Irreversible extinction of ferroelectric polarization in P(VDF-TrFE) thin films upon melting and recrystallization. *Appl. Phys. Lett.* **2006,** *88* (24), 242908.

10. Naber, R. C. G.; Tanase, C.; Blom, P. W. M.; Gelinck, G. H.; Marsman, A. W.; Touwslager, F. J.; Setayesh, S.; de Leeuw, D. M., High-performance solution-processed polymer ferroelectric field-effect transistors. *Nat Mat.* **2005,** *4* (3), 243-248.

11. Merz, W. J., Domain Formation and Domain Wall Motions in Ferroelectric BaTiO_{3} Single Crystals. *Phys. Rev.* **1954,** *95* (3), 690-698.
12. Vizdrik, G.; Ducharme, S.; Fridkin, V. M.; Yudin, S. G., Kinetics of ferroelectric switching in ultrathin films. *Phys. Rev. B* **2003,** *68* (9), 094113.
13. Yan, H.; Chen, Z.; Zheng, Y.; Newman, C.; Quinn, J. R.; Dotz, F.; Kastler, M.; Facchetti, A., A high-mobility electron-transporting polymer for printed transistors. *Nature* **2009,** *457* (7230), 679-686.
14. Suemori, K.; Kamata, T., Response delay caused by dielectric relaxation of polymer insulators for organic transistors and resolution method. *Appl. Phys. Lett.* **2012,** *101* (8), 083307.
15. Burgi, L.; Friend, R. H.; Sirringhaus, H., Formation of the accumulation layer in polymer field-effect transistors. *Appl. Phys. Lett.* **2003,** *82* (9), 1482-1484.
16. Cho, J. H.; Lee, J.; Xia, Y.; Kim, B.; He, Y.; Renn, M. J.; Lodge, T. P.; Daniel Frisbie, C., Printable ion-gel gate dielectrics for low-voltage polymer thin-film transistors on plastic. *Nat. Mat.* **2008,** *7* (11), 900-906.
17. (a) Scott, J. F., Switching of Ferroelectrics Without Domains. *Adv. Mat.* **2010,** *22* (46), 5315-5317; (b) Zhang, L., Field-induced phase transitions and dielectric energy density in poly(vinylidene fluoride-trifluoroethylene-chlorofluoroethylene) terpolymer. *EPL* **2010,** *91* (4), 47001.
18. Asadi, K.; Bruyn, P. d.; Blom, P. W. M.; Leeuw, D. M. d., Origin of the efficiency enhancement in ferroelectric functionalized organic solar cells. *Appl. Phys. Lett.* **2011,** *98* (18), 183301.
19. (a) Genenko, Y. A.; Zhukov, S.; Yampolskii, S. V.; Schütrumpf, J.; Dittmer, R.; Jo, W.; Kungl, H.; Hoffmann, M. J.; von Seggern, H., Universal Polarization Switching Behavior of Disordered Ferroelectrics. *Adv. Funct. Mat.* **2012,** *22* (10), 2058-2066; (b) Jiang, A. Q.; Lee, H. J.; Hwang, C. S.; Scott, J. F., Sub-Picosecond Processes of Ferroelectric Domain Switching from Field and Temperature Experiments. *Adv. Funct. Mat.* **2012,** *22* (1), 192-199.
20. Dunn, L.; Dodabalapur, A., Temperature dependent transient velocity and mobility studies in an organic field effect transistor. *J. Appl Phys.* **2010,** *107* (11), 113714.
21. (a) Dunn, L.; Basu, D.; Wang, L.; Dodabalapur, A., Organic field effect transistor mobility from transient response analysis. *Appl. Phys. Lett.* **2006,** *88* (6), 063507; (b) Fujieda, I.; Street, R. A., Transient drain current of polymer transistors. *J. Appl. Phys.* **2009,** *105* (5), 054503.
22. Dost, R.; Das, A.; Grell, M., Time-of-flight mobility measurements in organic field-effect transistors. *J. Appl Phys.* **2008,** *104* (8), 084519.

Chapter 6

Low voltage Fast-switching Polymer Field Effect Transistors



Chapter 6

Low voltage Fast-switching Polymer Field Effect Transistors

6.1 Introduction

The performance of a transistor is mainly governed by the field effect mobility (μ_{FET}), switching speed and power consumption. As shown in previous chapters, polymer field effect transistors (PFET) performance has been vastly improved and exhibits $\mu_{FET} > 1$ $cm^2V^{-1}s^{-1}$ and switching speed of 400 ns. However, these devices are limited by high operating voltages (60 V – 80 V)[1], dielectric related bias stress[2] and high power consumption[3]. Appropriate downscaling strategies are required to utilize the PFETs in the low-voltage regime. A general guideline to decrease the operating voltage of PFETs is by increasing the capacitance (C) of the gate dielectric such that substantial charge density ($n_G \sim 10^{19}$ cm^{-3}) can be obtained at low gate bias (V_g) [4]. Use of ultra-thin dielectric layer[5] or using materials with high-k is a natural route to resolve this issue[6]. However, ultra-thin dielectric layers fabricated from low-k polymer dielectric materials is generally prone to high leakage current (I_g), easy rupture of the thin films and poor device to device reproducibility[5]. Similarly, the presence of high-k dielectrics in organic FETs results in broadening of density of states (DOS) or polarization induced increase in the effective mass of charge carriers which drastically reduces the μ_{FET} [7]. Apart from these strategies, ultra-low voltages PFETs have also been demonstrated from ion gels or electrolytes and structures with β-Aluminate [4b, 8]. However, these devices suffer from limitation of hysteresis due to the possibility of electrochemical doping and slow responses, since the switching response of these devices is ultimately dependent on the movement of ions [4a, 9]. A brief analysis of the scientific literature in the field indicates that electrolyte gated n-type PFETs are rare. These factors have been a hindrance in the field of polymer electronics. Moreover, it should also be ensured that the strategy for decreasing the operating voltage does not affect the static and dynamic performance of the PFETs.

Printable PFETs which fall in channel lengths (L) of > 10 microns are generally associated with slow switching response[10]. Based on traditional MOSFET technology, the switching time (t_{on} or t_{off}) which scales as L^2/μ, [10] has been decreased for PFETs both by increasing the μ_{FET} with novel materials[1] or by downscaling of channel by various lithographic techniques[11]. However, lowering L to short-channel regime can introduce deviation in saturation behavior,[12] and hence it is essential that the channel length should be at least four times the dielectric thickness[5]. Therefore, proper downscaling strategy for a PFET will also involve obtaining reliable ultra-thin dielectrics with minimal leakage. In addition, fast switching PFET structures also require: ordered dipoles, trap free transport interface and semiconducting polymers with proven high μ_{FET} [10, 13]. Hence, for the usage of PFETs in day to day electronic applications it is essential to develop and design optimum dielectric materials such that the device demonstrates properties like low operating voltages, high μ_{FET} and minimal switching time. In this line of pursuit, a reliable downscaling technique is demonstrated which satisfies the pre-requisite for low power applications without compromising on the static and dynamic performance of the PFETs.

6.2 Self-Assembled Nano-Dielectric Layers (SAND)

Organic-inorganic hybrid materials are of interest for electronic applications since they can combine advantageous properties of both types of materials[14]. These materials provide excellent mechanical, electrical and environmental durability of the inorganic material as well as mechanical flexibility and tenability of organic materials[15]. Hence these hybrid materials have been utilized as dielectric layers in FET structures for a range of semiconducting materials which include metal di-chalocgenides, nano-tubes[16], graphene[17] and amorphous oxides[18]. Low voltage FETs from organic molecules have also been demonstrated using hybrid dielectric layers. However, most of the device structures are limited by: high temperature processes (T > 400 °C), restricted to bi-layers and involve low-k organic dielectric layers (SAMs or PMMA) for interface passivation[3, 19]. The utilization of SAM's (k ~ 2.5) or low-k polymer dielectric layer (k ~ *4*) in the bi-layer hybrid dielectric structures limit the overall capacitance, leakage behavior and the control on scaling of the dielectric structure[14a, 20]. Recognizing these drawbacks, π-conjugated dielectric layers based on polar groups are used as the organic layer in our self-assembled dielectric thin films. Highly polarizable groups in these self-assembled nano-dielectric (SAND) structures result in capacitance (C_{SAND}) comparable or better than other solution

grown high-*k* dielectrics. Furthermore, the self-assembly technique for fabricating dielectric structures provide a facile control over the thickness, capacitance and the interface disorder which is utilized in a PFET geometry to obtain $\mu_{FET} > 2.0$ $cm^2V^{-1}s^{-1}$ at input voltages of |1 V|.

In this chapter, the usage of one such hybrid self-assembled nano-dielectric (SAND) structures is highlighted which satisfy both the criteria for downscaling to dielectric thickness of ~ 8 nm as well as ordered dipoles. Both these conditions satisfy the pre-requisites for low operating voltage and fast switching PFETs.

6.3 SAND Fabrication

Traditionally, the usage of SAND was limited to Si/SiO_2 based substrates which reduced its applicability in fast switching circuits due to high parasitic capacitance from overlapping electrodes[2a, 14b, 21].Taking note of this problem, a novel strategy to obtain patterned and aligned PFETs with SAND dielectric is developed that demonstrate switching time as low as 150 ns for printable channel length of 10 μm. This approach consists of combining conformal coating of the primer layer on ultra-smooth patterned metal electrodes followed by the growth of solution processed multilayered dielectric structure. This method of fabricating SAND based devices have opened up the usage of local embedded metal electrodes with SAND structures for designing high performance circuits. Typical growth of the SAND structure is shown in **Figure: 6.1**.

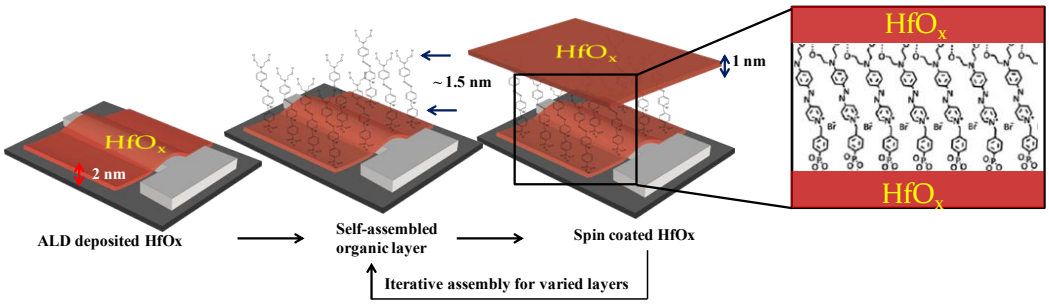


Figure 6.1: *Schematic of the self-assembly procedure adopted for the SAND (~ 5 nm - 18 nm) growth.*

The procedure involves a structure consisting of ALD grown conformal coating of HfO_x layer (2.1 nm) on metal electrodes. This was followed by self-assembly of the 4-[[4-[bis(2-hydroxyethyl)amino]phenyl]diazenyl]-1-[4-(diethoxyphosphoryl)benzyl]pyridinium bromide: π-PAE and sol-gel coated HfO_x layer in an iterative fashion as follows. The substrates were then immersed in a preheated ~ 3 mM solution of PAE for 1 h at 60 °C.

Then the substrates were sonicated and blow dried under nitrogen flow. After the growth of PAE layer, HfO_x was introduced by spin coating within the NuAire Class 10 HEPA-filtered clean hood at 5000 rpm for 30 secs and baked at 150 °C for 1 hr. The sol-gel precursor for HfO_x is obtained from a 0.03 M of ethanolic solution of $HfCl_4$ under ambient. Concentrated HNO_3 is subsequently added to the cloudy dispersion in a 10:1 molar ratio (HNO_3:$HfCl_4$) as a hydrolysis catalyst. The buffer solution is stirred at 60 °C for 4 - 5 hrs and then diluted to the desired concentration before coating. After the growth of required layers of SAND, a thin layer of $HfCl_4$ (0.2 mM) was spin coated (5000 rpm for 30 secs) on top as a capping layer and annealed at 150 °C for 1 hr. Multilayered variants of the SAND dielectric structure were obtained by controlling the number of bi-layers for HfO_x and PAE. In this chapter the number of bilayer are referred by the index *n*.

The thickness of these multi-layered dielectric structures were estimated by obtaining a step edge marked with a probe tip of 1 μm diameter as shown in **Figure: 6.2**.

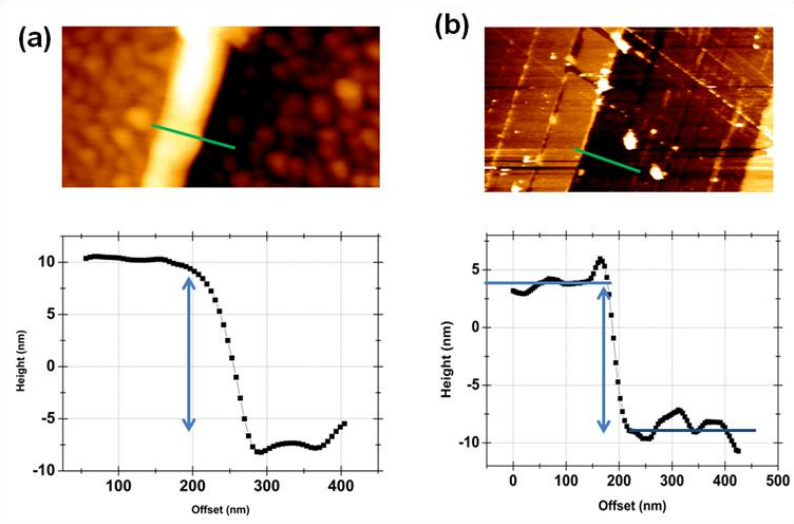


Figure 6.2: *Step-edge measurement for determining the thickness of the SAND dielectric layers (a) 6L SAND (b) 4L SAND coated on Al metal electrodes.*

Complete removal of the SAND dielectric layer is ensured by electrical shorting of the ITO electrodes. The imaging of the step edge is obtained using, JPK Nanowizard 3 by using a Cr/Pt coated conducting tip (F = 40 N/m, Resonant frequency, ω_R = 300 kHz) in the non-contact mode.

6.4 Electrical Characterization of SAND

The electrical characterization of the SAND super-lattice structures were performed by fabricating patterned metal-insulator-metal (MIM) based capacitor structures. Measurements were performed on these MIM structures to estimate the *C(f)*, loss response, leakage current density and breakdown strength.

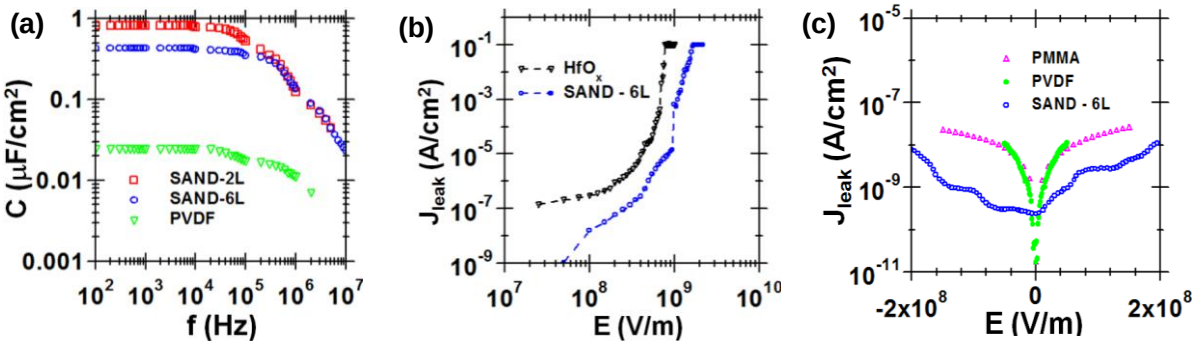


Figure 6.3: *(a) Frequency response of SAND-2L (8 nm), SAND-6L (~ 18 nm) and high-k PVDF (~ 200 nm) at V_{rms} ~ 50 mV. (b) Breakdown strength estimation (J_{leak} v/s E) for SAND dielectric layer and ALD grown HfO_x (~ 40 nm) layer. (c) J_{leak} estimation for a polymer dielectrics films PVDF and PMMA compared with SAND.*

The measurements indicate C_{SAND} (at 100 Hz) to be in the range of (0.4 ± 0.1) μF/cm^2 with k_{eff} ~ 10 for six layered (SAND-6L) structures which was tuned to C_{SAND} (at 100 Hz) ~ (0.8 + 0.09) μF/cm^2 and k_{eff} ~ 6 for two layered SAND structures. This corresponds to a thickness variation of SAND in the range of 10 – 18 nm. It is to be noted that such magnitude of capacitance is comparable to the Debye layer of electrolytes and is rarely observed for polymer dielectric films. High magnitude of C_{SAND} corroborates with rationale design of SAND which comprises highly polarizable-π groups. The magnitude of C_{SAND} obtained from these local-gated SAND super-lattice structures is lower than the values obtained from SAND grown on Si/SiO_2 substrates[14b]. This can be related to the difference in the surface properties of the substrates which can affect the self-assembly to modify the dipole density, polarization and breakdown field. As seen in **Figure: 6.3 (a)**, $C_{SAND}(f)$, is retained until a frequency > 0.5 MHz. The frequency response of SAND is about two orders of magnitude higher than those of solution processable high-*k* polymer dielectrics (C ~ 50 nF/cm^2) and electrolytes (C ~ 1 μF/cm^2) where the frequency response is limited to ~ 10 kHz[4a]. The slow relaxation of polymer dielectrics and electrolytes severely restricts its use in high frequency FET circuits. However, the self-assembly technique

adopted for growing dielectric layer results in ordered and aligned dipoles which can easily respond to fast switching electric fields, similar to the switching observation with poled ferroelectric dielectrics[10, 13a, 22]. Hence, SAND based dielectrics are excellent candidate in the design of high frequency polymer circuits.

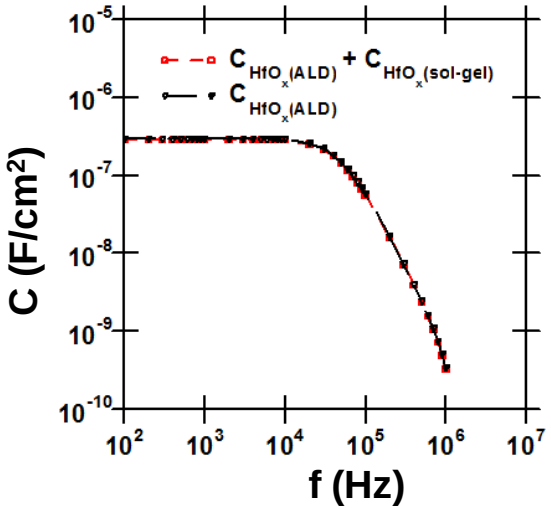


Figure 6.4: *MIM characterization of the HfO_x grown by ALD (40 nm) and HfO_x (ALD – 40 nm) + HfO_x (Sol-gel – 2 nm).*

The capacitive response of the SAND super-lattice structure was modeled as a series capacitor of the constituent layer: $C_{SAND}^{-1} = C_{Al_xO_y}^{-1} + C_{HfO_x,ALD}^{-1} + n.\left(C_{PAE}^{-1} + C_{HfO_x}^{-1}\right)$ where n is the number of layers. The thickness of native Al_xO_y ~ 1 nm and combined thickness of one layer of SAND (PAE and HfO_x) ~ 2.5 nm was estimated from AFM measurement which were comparable to the earlier reports[14b]. ALD grown HfO_x and solution grown HfO_x were characterized by independent set of capacitance measurement as shown in **Figure: 6.4** and k was obtained to be 13.5 and 13 respectively. From the expression for series capacitance k_{PAE} is obtained to be ~ 14.2 which is comparable to the value reported earlier[14b]. Maximum displacement field is estimated from the following expression: $D_{max} \sim \varepsilon_o k_{eff} E_{bd}$ (where E_{bd} is the dielectric breakdown field). The E_{bd} is estimated from the onset of non-linear current flow in the MIM device structure. As seen from **Figure: 6.3b**, E_{bd} was obtained to be ~ 7×10^8 V/m for ALD grown HfO_x dielectric layer (~ 40 nm) and ~ 9×10^8 V/m for SAND super-lattice structure (~ 18 nm). This translates to a $D_{max,SAND}$ ~ 7.9 μC/cm^2 which is comparable to the state of art ALD grown HfO_x [23] with $D_{max,HfOx}$ ~ 8.4 μC/cm^2. Based on this metric, it is evident that the leakage property of the SAND structure is not compromised in spite of increased capacitance and

the multilayer architecture. The sizable values of E_{bd} and D_{max} which is comparable to inorganic oxides point to the advantage of a hybrid self-assembled structure. Self-assembled technique enhances the dipole density and consequently increases E_{bd} and k_{eff}[24]. This is also reflected in the leakage current density estimated from metal-insulator-semiconductor (MIS) structures. J_{leak} as low as 10^{-8} – 10^{-9} A/cm^2 was obtained for with SAND based MIM structures (**Figure: 6.3c**) which translate to an effective leakage current of 0.1 pA in patterned PFET structures. This magnitude of leakage is comparatively lower than the J_{leak} of 1 A/cm^2 ($\pm$ 2 $\times$ 10^8 V/m)[14b] obtained with native SiO_2 and J_{leak} of 5 $\times$ 10^{-8} A/m^2 ($\pm$ 1 $\times$ 10^8 V/m) for other polymer dielectrics.

6.5 Microscopic Characterization of SAND

Morphological analysis of the SAND dielectric surface was performed to understand its suitability for large area polymer circuits. AFM of the SAND dielectric structures show uniform coverage with average roughness of ~ 4.5 Å (**Figure: 6.5a, b**). Small area scans were also obtained along with large area scans to provide an insight into the intricate features of the SAND surface on the metal electrodes. The typical average roughness for these large area scans were obtained to be in the range of 4.7 - 5 Å. Scanning capacitance microscopy (SCM) measurements were performed on SAND structures to determine the spatial uniformity of the capacitive property. As evident from the SCM measurements, the SAND films are electrically smooth.

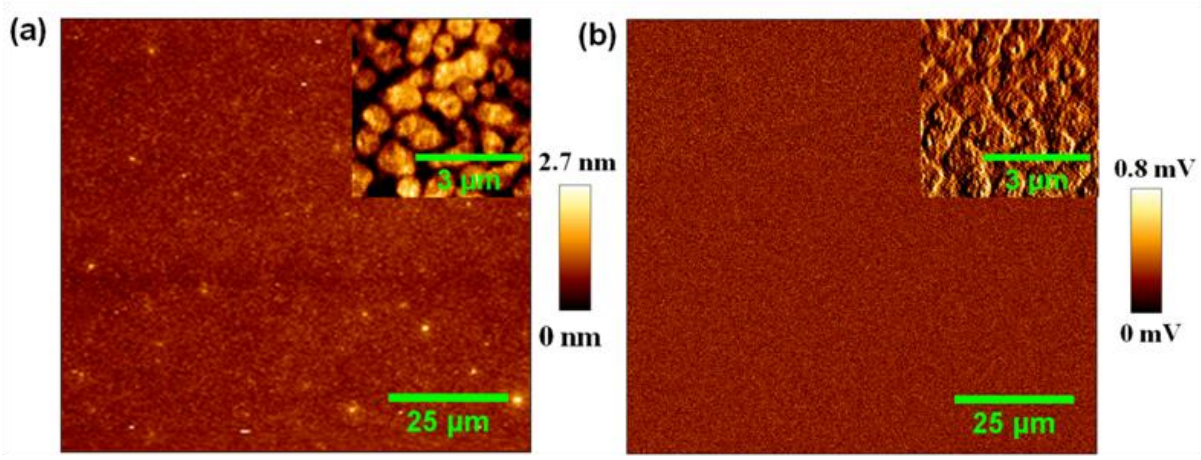


Figure 6.5: *Surface characterization of SAND layer grown on the metal gate electrodes.(a) Height and (b) SCM images (90 μm × 90 μm) indicating uniform surface topography and electrical properties over large area. Inset shows the zoomed image (5 μm× 5 μm).*

Furthermore, SAND structures grown on hydrophilic glass substrates were also characterized to estimate the surface properties. The AFM images of the SAND surface grown on the glass substrates demonstrate smaller island like features, with average roughness of 7 – 9 Å over a 10 μm × 10 μm area (**Figure: 6.6**).

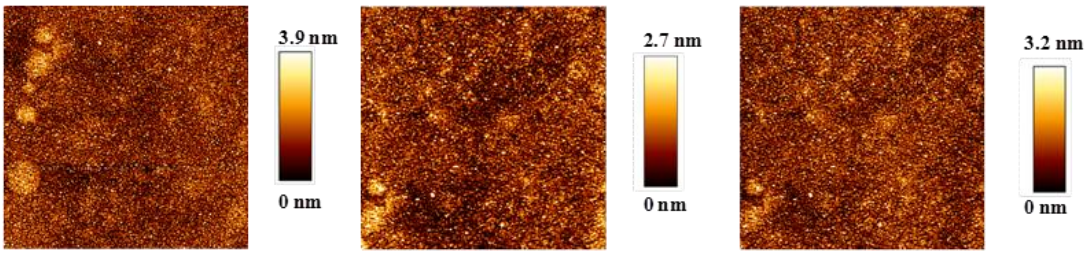


Figure 6.6: *AFM topographic image for SAND structures grown on RCA treated hydrophilic glass substrates (10 μm × 10 μm). Typical r.m.s roughness was estimated to be in the range of 7 - 9 Å.*

In general, the smoothness and surface features of the SAND dielectric layer is comparable to commercially grown oxide films and is an order of magnitude lower than other solution processable high-*k* dielectric layers like PVDF (**Figure: 6.7**). This exceptional smoothness is favorable for well-defined interface and improves the dielectric breakdown characteristics[24]. The measured electrostatic force variation due to surface capacitance change for SAND structure was obtained to be in the range of 100 μV (**Figure: 6.5b**) as compared to ~ 3 - 5 mV in case of PVDF based solution processable dielectrics (**Figure: 6.7c**).

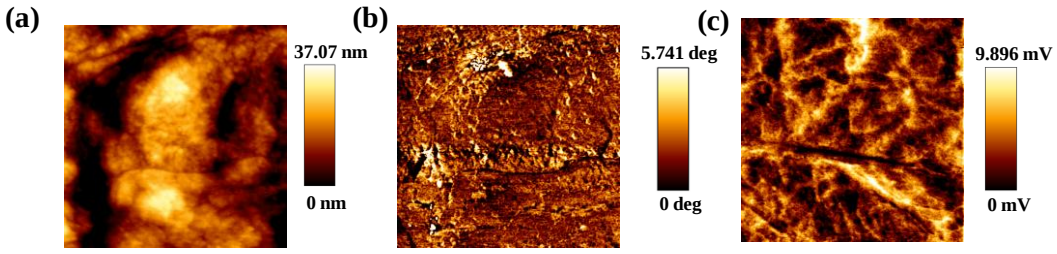


Figure 6.7: *(a) Height, (b) phase-AFM and (c) SCM image for PVDF based dielectric films coated on ITO glass substrates obtained over a region of 10 μm × 10 μm area.*

Polymer layers were further coated on the dielectric layer and the morphology was studied. Dialkoxy bi-thiophene based *p*-type PBTOR films showed crystallite formation with typical size ~ 20 nm and r.m.s roughness of 2 nm. In the case of *n*-type N2200 films

interconnected network of polymer structure was obtained with r.m.s roughness of 0.5 nm (**Figure: 6.8**).

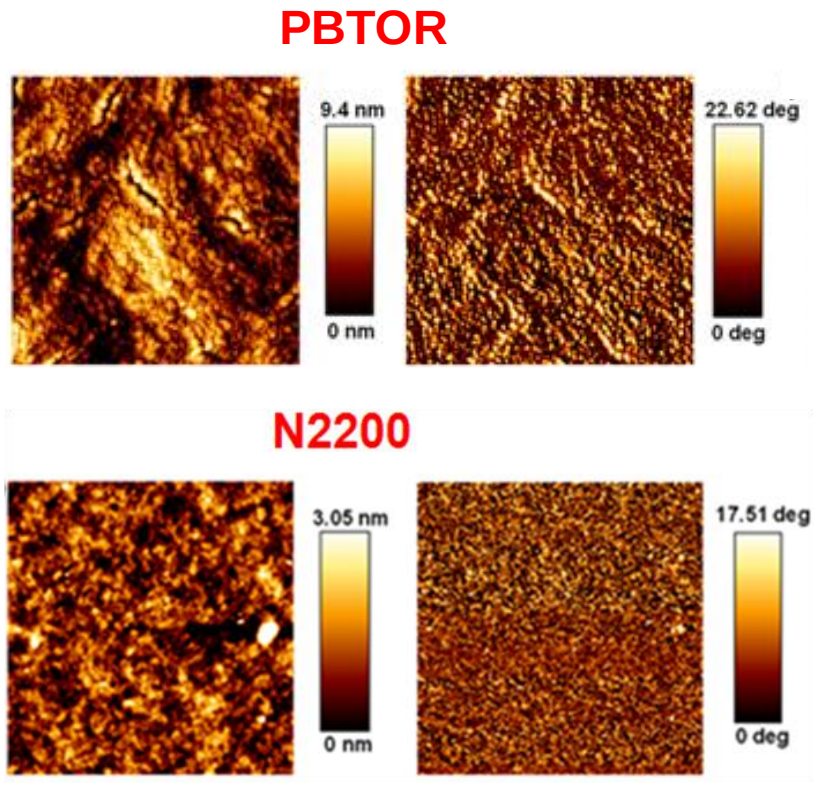


Figure 6.8: *Height and phase image of PBTOR (~ 20 nm) and N2200 (~ 20 nm) surface on SAND dielectric layer (1 μm × 1 μm).*

6.6 SAND Devices

6.6.1 PFETs

Bottom-gated top-contact field-effect transistors were fabricated with both *n*-type (N2200) and *p*-type (PBTOR) semiconducting layers. The fabrication procedure involved growing the multi-layered Hf-SAND structures. The surface of the Hf-SAND layer is modified by self-assembled monolayer (SAMs) of ODPA. Phosphonic acid based SAM's were prepared by immersing the SAND coated substrates in a 2mM ethanolic solution of ODPA overnight, rinsing in EtOH and drying under a nitrogen stream. Polymer active layers (20 nm) PBTOR and N2200 were spin coated from a 5 mg/ml solution in chlorobenzene at 1000 rpm for 1 min. It was observed that SAND dielectric is compatible with both classes of semiconducting polymers: the hole conductor PBTOR and the electron conductor P(NDI2OD-T2) or N2200. The active layers were annealed in nitrogen atmosphere at 110 °C for 30 mins. This was followed by coating patterned aligned Au S-D

electrodes (10^{-6} mbar, 1 Å/s, 30 nm thick) to complete the device fabrication. The physical mask for the S-D electrodes was aligned mechanically under a microscope. The channel lengths for the devices were chosen depending on the dimensions of the gate electrode to obtain minimum overlap and extremely low parasitic capacitance (1 pF/cm^2). The channel width (W) was 1 mm for the PFETs and L was varied over 5 μm to 250 μm range. Typical image of the patterned aligned electrodes are provided in the **Figure: 6.9**.

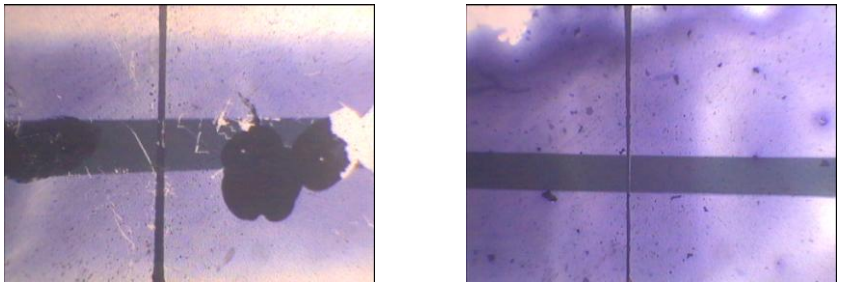


Figure 6.9: *Typical image of the patterned electrode PFETs*

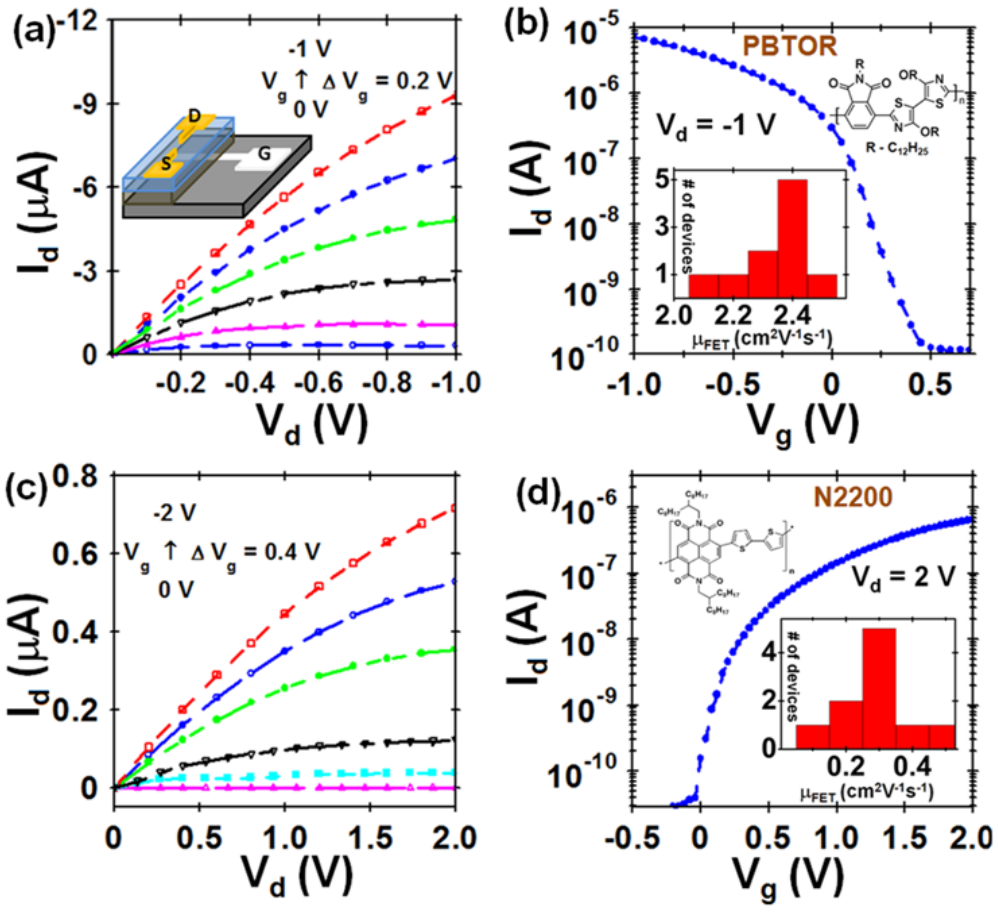


Figure 6.10: *Output and transconductance curves for SAND (~ 8 nm) based PFETs with (a & b) p-type PBTOR (~ 20 nm) semiconductor and (c & d) n-type N2200 (20 nm) semiconducting layer. Typical L = 60 μm, W = 1mm. Inset b & d shows the statistical distribution of the mobility. The width of the bar indicates error in the range of 5 – 10 % originating from a constant systemic error.*

The PFET devices with SAND dielectric layer and PBTOR (*p*-FETs) or N2200 (*n*-FETs) polymers operate at V_g and V_d ~ |1 V| with well-defined linear and saturation regime (**Figure: 6.10**) and negligible hysteresis. The performance parameters estimated from the standard transconductance equation are as follows: μ_{FET}^{h} ~ 2 – 2.5 $cm^2V^{-1}s^{-1}$, μ_{FET}^{e} ~ 0.1 - 0.5 $cm^2V^{-1}s^{-1}$ respectively and I_{on}/I_{off} ~ 10^4 – 10^5. In total, 15 devices were fabricated for the DC measurement with a 95 % working devices. Typical μ_{FET} statistics of the devices are shown in inset **Figure: 6.10b & d**. These μ_{FET} values are comparable to several state-of-art PFETs operating at high voltages[25]. In addition, $|V_{th}|$ ~ ± 0.05 V and *SS* ~ 100 - 500 mV/dec were obtained for these devices indicating the low voltage required to switch on the device.

These performance parameters are retained for four weeks in the devices (**Figure: 6.11**).

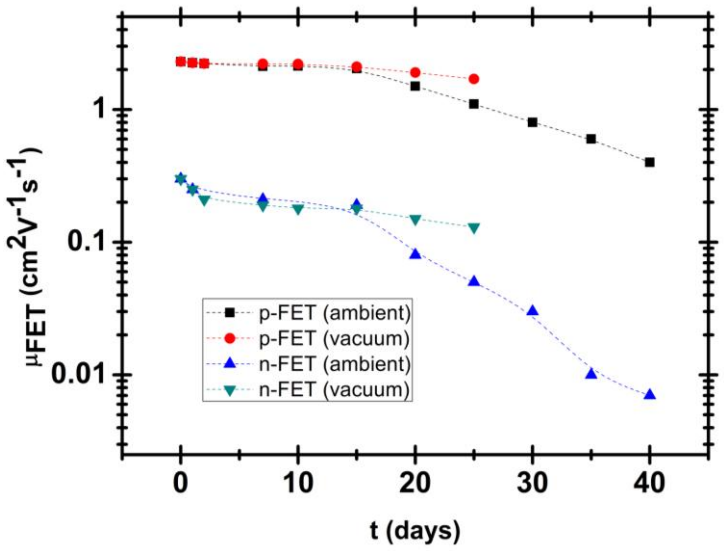


Figure 6.11: *Typical μ_{FET} variation with time when the devices are operated under vacuum and under ambient condition for the p-FETs and n-FETs (L = 60 μm, W = 1mm) fabricated with SAND based dielectric layer (~ 18 nm) and PBTOR (~ 20 nm) or N2200 (~ 20 nm) based semiconducting active layer.*

Bias stress measurements were performed on these devices by applying continuous bias of |1 V| for up to ~ 10^4 s (**Figure: 6.12**). The transfer curves showed little difference with bias stress indicating the relative stability of the dielectric layer and the transport interface.

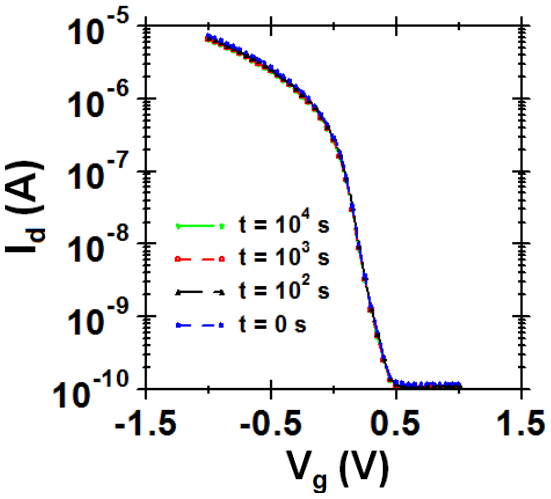


Figure 6.12: *Typical time variation of the transconductance measurement obtained for a PFET (L = 60 μm, W = 1mm) with SAND based dielectric layer (~ 18 nm) and PBTOR (~ 20 nm) as the semiconducting active layer.*

6.6.2 Interface Energetic

Understanding of the SAND-polymer interface is obtained by comparing the performance of SAND-based devices with PFETs fabricated from a range of polymer dielectric layers such as BCB: k ~ 2.6, PMMA: k ~ 3.6 and PVDF: k ~ 8. For the sake of comparison, bottom-gate top-contact *p*-FET and *n*-FET structures with aligned electrodes were also fabricated using these polymer dielectric materials. PFETs fabricated with PBTOR semiconductor and BCB or PMMA dielectric layer exhibited much lower μ_{FET}. BCB dielectric layer based PFETs demonstrated μ_{FET} in the range of 0.1 – 0.3 $cm^2V^{-1}s^{-1}$ while, PFETs with PMMA dielectric layer had a μ_{FET} ~ 0.05 – 0.1 $cm^2V^{-1}s^{-1}$ at V_g = - 80 V. In essence, there is a significant increase of μ_{FET} in SAND based PFETs compared to PFETs fabricated with low *k*-polymer dielectric layer. However, *n*-FETs fabricated with SAND or PMMA dielectric layer exhibit comparable values of μ_{FET} (≈ 0.2 – 0.4 $cm^2V^{-1}s^{-1}$) with marginally higher performance for the SAND based devices.

Consequently, transport measurements at variable temperatures (**Figure: 6.13a & b**) were carried out to estimate the energetic disorder at the transport interface and understand the underlying mechanism. **Table 1** summarizes the temperature dependent measurements for both *p*-FETs and *n*-FETs with different dielectric layers. Arrhenius fits to the $\mu_{FET}(T)$ data obtained from *p*-FETs yield a lower activation energy ($E_{A,SAND}$) ~ 65 meV compared to 95 meV obtained for devices with PMMA dielectric layer. Similarly, *n*-FETs

exhibit lower E_A (53 meV) for devices fabricated with SAND as compared to devices with PMMA dielectric layer (78 meV). These magnitudes of E_A are consistent with the high $|V_{th}|$ ~ 5 - 10 V and SS ~ 7 - 11 V/dec obtained for BCB and PMMA based PFETs compared to $|V_{th}|$ ~ ± 0.05 V and SS ~ 100 - 500 mV/dec obtained in the case of SAND based PFETs.

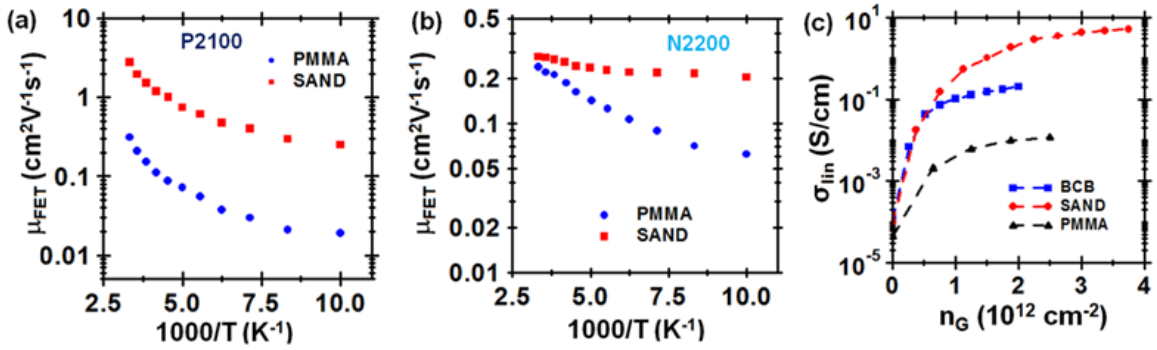


Figure 6.13: *Variation of charge transport with T and n_G. Plot of μ_{FET} with 1/T for (a) p-FETs (PBTOR) and (b) n-FETs (N2200) fabricated with SAND (~ 18 nm) and PMMA (~ 400 nm) dielectric layer. (c) Log scale plot of σ_{lin} as function of n_G for p-FETs fabricated from different dielectric layers. Typical device dimensions were maintained at L = 60 μm, W = 1mm.*

The E_A magnitude of less than 0.1 eV is indicative of low energetic disorder at the interface thus supporting the high μ_{FET} in SAND based PFETs. However, the fact that *n*-FETs exhibit lower μ_{FET} and lower E_A, which is an opposite trend as compared to a higher μ_{FET} and higher E_A seen for *p*-FETs, needs an interpretation. This result is attributed to a combination of two factors: the isolation of the conjugated core of N2200 from the polar dielectric layer[25a] and the high degree of structural disorder and grain boundaries evident from the crystallite morphology of PBTOR molecule[26]. In N2200 based *n*-FETs owing to the edge-on stacking the long alkyl-chains isolate the conjugated core from the electrostatic dipolar disorder of the dielectric layer, which is reflected in lower E_A. However, in case of devices fabricated with *p*-type PBTOR semiconductor, the underlying dielectric layer strongly affects the transport as evident from **Figure: 6.13a**. This can originate from the predicted face-on stacking structure [25b, 27]. Morphological analysis of PBTOR films on SAND dielectric layer indicates a crystallite structure (**Figure: 6.8**) with grain boundaries which is known to hinder inter-crystallite hopping thus resulting in higher E_A. On the other hand, N2200 films demonstrate interconnected structures more tolerant to disorder and

favor chain to chain hopping. This $\mu_{FET}(T)$ trend for the *n*-FET and *p*-FET points to a general consistency of the transport trends in polymer semiconductors obtained by correlating disorder, aggregation and charge transport[26].

Further quantitative understanding of the SAND-polymer interface is obtained from the evaluation of the interface trap density. The density of interfacial trap states for different dielectric-semiconductor interface was estimated by the equation:

$$N_{ss}^{max} = \left[SS \times \frac{\log(e)}{\frac{kT}{q}} - 1 \right] \times \frac{C}{q^2} \qquad \text{……..(6.1)}$$

where, q is the unit electronic charge and *C* is the capacitance per unit area of the dielectric layer[3, 24]. Trap density for *p*-FETs fabricated with low-*k* dielectrics were obtained to be in the range of 5×10^{12} $cm^{-2}eV^{-1}$ which increases to 10^{13} $cm^{-2}eV^{-1}$ for high-*k* dielectrics. In comparison SAND based devices demonstrated N_{ss}^{max} of 10^{12} $cm^{-2}eV^{-1}$ much lower than other dielectric layer based devices. These results corroborate with the trends of low E_A and higher μ_{FET} for SAND based devices compared to PFETs with other dielectric layer. The FET conductivity (σ_{lin}) in the linear regime of FET transport was analyzed as a function of gate induced charge density (n_G) to understand the trend of observed high μ_{FET} for devices fabricated with high-*k* dielectric layer .

As shown in the **Figure: 6.13c**, σ_{lin} increases with the n_G for all dielectrics. It is observed that, at low magnitude of n_G, σ_{lin} magnitudes are comparable for PFETs fabricated with different dielectrics. However, as n_G increases σ_{lin} increases more rapidly for SAND based PFETs compared to other polymer dielectric based PFETs. This relation between the transport parameters and n_G can be understood using the mobility edge (ME) model with exponential DOS, given by $g(E) \sim \exp(-E/E_o)$, where E_o is the width of DOS[24, 28]. As per the ME model polymer semiconductors are in general associated with disordered localized states and charge carriers in these states have negligible contribution to the effective σ_{lin}. Hence, charge transport involves thermal excitation to the transport level (E_t) with an energy E_A. As the charge density increases the quasi-Fermi level E_F is lowered and $E_A \sim E_F - E_t$ decreases. In other words, as the charge density increases the effective number of localized states decrease which in turn is observed as lower density of trap states. Thus, the high μ_{FET} and low trap density manifests itself as high channel current density in the SAND PFETs.

Table 1: *T dependent transport characterization for PFETs fabricated with PBTOR and N2200 as semiconducting layer and different dielectric layers. Typical channel dimension of the devices is maintained at L = 60 – 100 μm, W = 1mm.*

Polymer	Dielectric	C (nF/cm^2)	μ_{FET} (at 300K) ($cm^2V^{-1}s^{-1}$)	E_A (meV)	SS (V/dec)
PBTOR	BCB	4	0.3	72	5
	PMMA	7.9	0.1	95	11
	SAND	215	2.5	65	0.1
N2200	PMMA	4	0.2	78	12
	α-PVDF	15	0.12	95	17
	SAND	202	0.4	53	0.8

6.6.3 Switching Measurements

The switching performance of these SAND based PFETs was then estimated to test its usability in high frequency applications. PFET dynamic performance is determined by the transit time of charge carriers across the electrodes, dielectric relaxation time and charging duration of the parasitic capacitance due to overlapping electrodes[10]. As evident from the analysis above, SAND provides an ordered interface for improved charge transport. In addition, the dielectric super-lattice structure supports efficient dipole relaxation and retains the capacitance of ~ 70 nF/cm^2 up to a frequency of 10^7 Hz. The high-*k* of SAND dielectric structure makes it suitable for obtaining high transverse field at low V_g. This combination of microscopically ordered interface, high transverse field and fast dielectric relaxation can assist in improving the dynamic performance of SAND based PFETs.

The switching response of the SAND based PFETs were obtained by monitoring the $I_{ds}(\Delta V_g)$ profile in response to an input square pulse ΔV_g = 5 V (rise time of 10 ns). $I_{ds}(t)$ profile is obtained by taking the difference between the recorded profiles corresponding to $|V_d|$ = 4 V and $|V_d|$ = 0 V. The OFF state profile originates from parasitic capacitance due to overlapping electrodes whereas the ON-state has an additional component from channel current. In order to minimize the contribution from the geometrical parasitic capacitance,

devices were fabricated with aligned S-D-G electrode. Typical parasitic capacitance was obtained to be in the range of (~ 1 pF/cm^2 – 1 nF/cm^2) from the RC fitting to the off-state response. It was ensured that the *RC* time constant of the external circuitry is 50 times lower than the best response time obtained from these printable FETs. The on-time (t_{on}) and off-time (t_{off}) is defined as the duration over which I_{ds} changes from 10% to 90%. Typical, dynamic response of a SAND based *p*-FET in response to an input square pulse $|\Delta V_g|$ = 5 V is shown in **Figure: 6.14**.

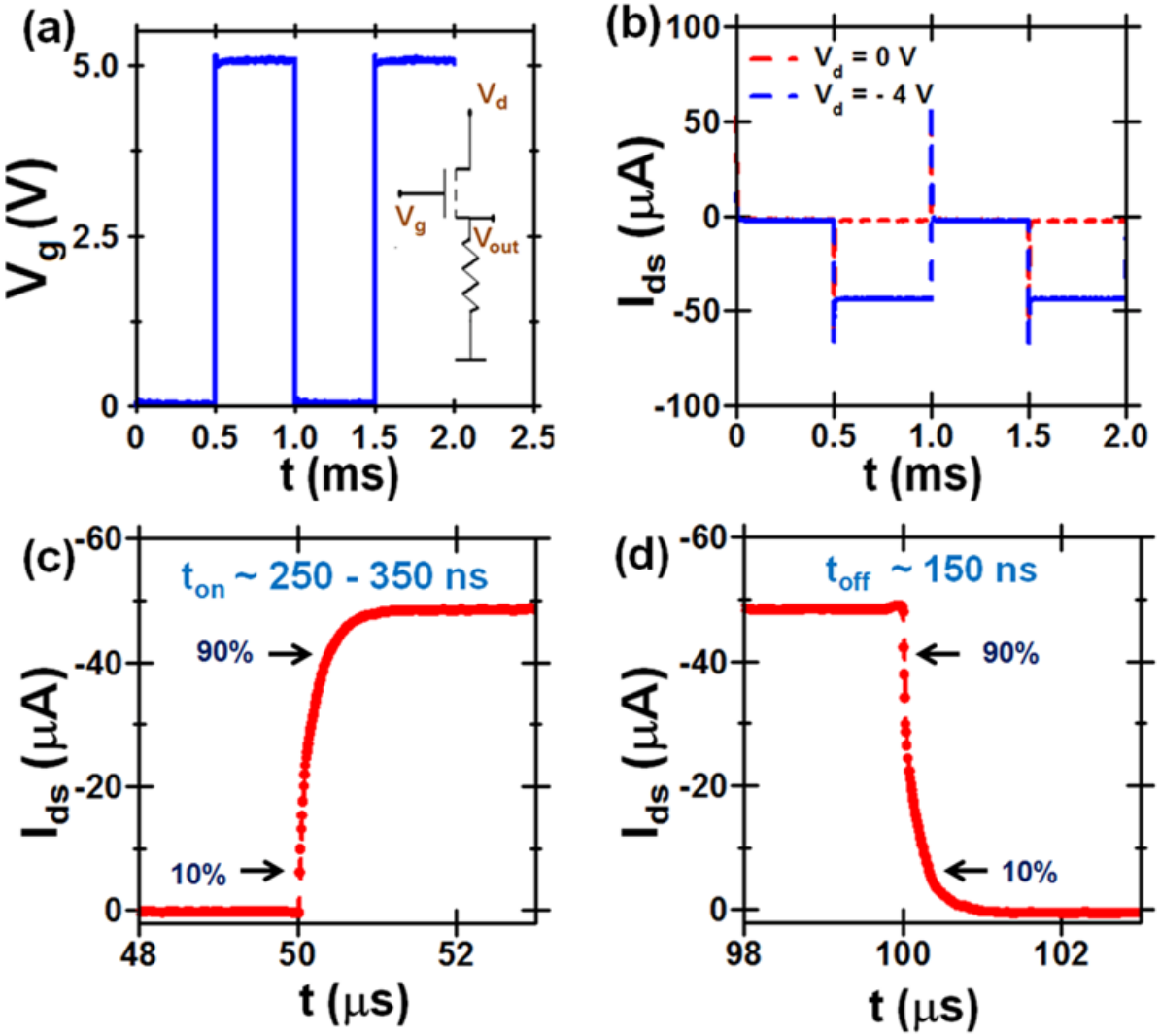


Figure 6.14: *Switching behavior of p-FETs (L = 10 μm, W = 1mm) fabricated with PBTOR (~ 20 nm) semiconductor and SAND (~ 18 nm) dielectric layer in response to a square pulse $|\Delta V_g|$ = 5 V. (a) Input pulse (inset circuit schematic). (b) Measured I_{ds} through the resistor (R ≈ 1–10 KΩ) at V_{ds} = - 4 V and V_{ds} = 0 V. (c & d) Zoomed switching profile of $I_{ds}(t)$ indicating the manner in which "on time: t_{on}" and "off time: t_{off}" was estimated.*

PFETs with channel length ($L \approx 10$ μm) and SAND dielectric structures switch in nanosecond timescale at an operating voltage of |4 V|. Typical magnitude of t_{on} and t_{off} was obtained to be 250 ns and 150 ns respectively, for PFETs with PBTOR active layer and SAND dielectric structure at an operating voltage of V_d = - 4 V. The switching time increases to 2 μs when the operating voltage is decreased to V_d = - 1 V. In comparison, PFETs fabricated with polymer dielectric demonstrated higher t_{on} > 1.5 μs for an operating voltage of – 40 V. In these devices t_{on} can be estimated from:

$$t_{on} \sim \frac{2\pi L\,(L+2\Delta L)}{\mu_{FET} V_d} \qquad \text{……..(6.2)}$$

where ΔL is the overlap length of the electrodes. This estimate gives the magnitude of t_{on} ~ 500 ns for μ_{FET} ~ 2.5 $cm^2V^{-1}s^{-1}$ and ΔL ~ 0. The variation in the observed and estimated switching time can be correlated to the high μ_{FET} magnitude obtained from the switching measurements[13c]. During the switching process, the effective number of localized trap states decreases which get reflected in the higher channel current (**Figure: 6.14c**). This results in higher dynamic μ_{FET} and explains the observed mismatch in the experimental and estimated t_{on} for SAND based PFETs. The enhanced dynamic performance of SAND based PFETs can thus be attributed to a favorable combination of interface energetics, ordered dipoles and high transverse field.

6.6.4 Logic Circuits

p-FETs and *n*-FETs fabricated with SAND dielectric layers are utilized to construct arrays of low voltage and low power polymer logic circuits (PLC). Inverters (**Figure: 6.15a**) and universal NAND logic circuits (**Figure: 6.15c**) were fabricated and characterized by standard input-output (V_{in} - V_{out}) transfer characteristics and gain curves. Both NAND and NOT logic circuits demonstrate the expected output as evident from **Figure: 6.15a & c**. The logic circuits exhibit voltage gain of ~ 38 and current gain of 10^5 - 10^6 with near-ideal *Z*-type response. The low voltage gain of these PLC's can be attributed to the imbalance in the electron and hole transport observed for N2200 and PBTOR semiconductors, respectively. One of the ways to improve the output curves and the gain margins of these circuits is by tuning V_{th} with different metal electrodes and also by modifying the device geometry. Typical static power dissipation ($V_{dd} \times I_{leakage}$) was obtained to be in the range of 1 - 10 nW for a maximum $|V_{in}| = 1$ V. In comparison, PVDF

based inverters demonstrate much higher power dissipation in the range of 0.4 μW – 1 μW for maximum $|V_{in}|$ = 80 V. It is observed that the inverter circuits deviate from the ideal response at high bias. This could be attributed to bias dependent trap density which ultimately governs the $\mu_{FET}(V_g)$ trends affecting the balance in charge transport.

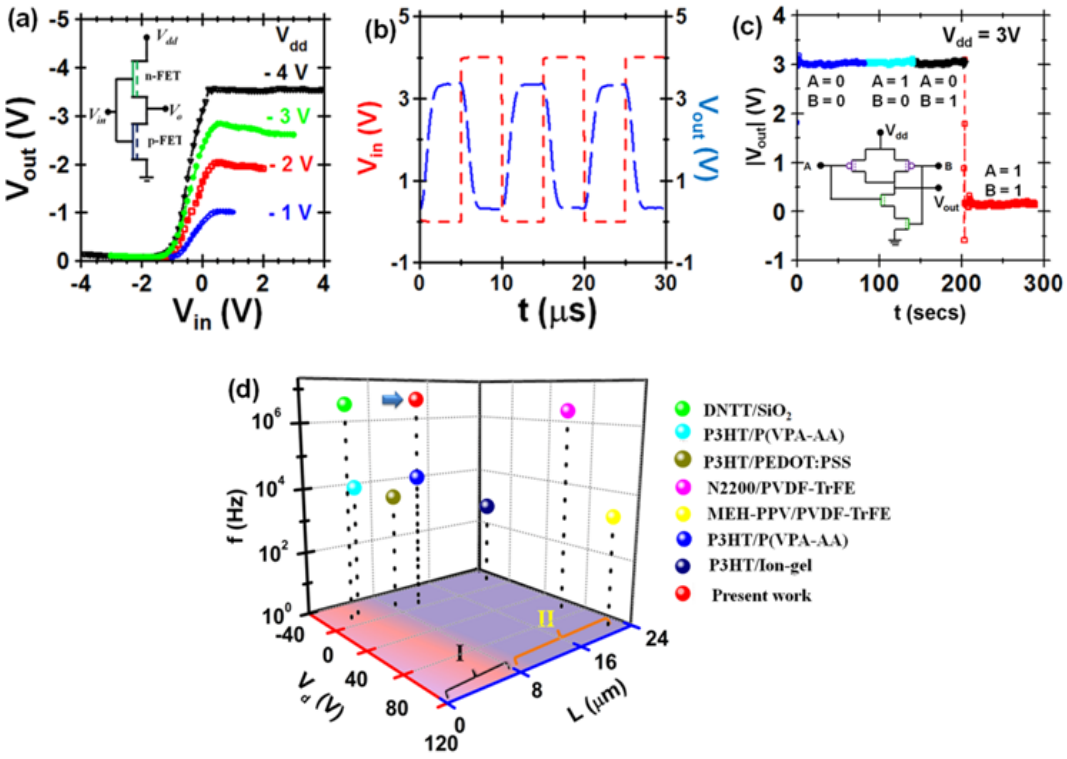


Figure 6.15: *Static and dynamic characterization of SAND (18 nm) based logic circuits fabricated with PBTOR based p-FETs as load and N2200 based n-FETs as driver. (a) Typical transfer voltage curves for polymer inverters (L = 10 μm, W = 1mm). Inset shows the typical circuit diagram. (b) Representative switching response of the same inverter for a square pulse V_{in} = - 4 V and V_{dd} = - 4 V. These curves represent that the devices can be operated at much higher frequency. (c) NAND circuit output response for different combinations of input voltages. Input voltages of -3 V and +3 V are considered as logic "0" and "1" respectively. (d) Comparison of dynamic response from various PFET structures with a range of dielectric and semiconducting materials. Region I indicates non-printable regime for PFETs and region II is in the regime corresponds to channel length which are printable.*

Operating frequencies of these arrays of logic circuits were obtained to be ~ 1 MHz, as measured by comparing the output pulse with the input pulse at various frequencies for printable large channel (~ 10 μm) devices and had a typical gain bandwidth product of 5 MHz. A comparison between the frequency behavior of polymer transistors reported earlier and this work is given in **Figure: 6.15d**. Demonstration of such low power, low voltage PLC with high frequency response opens up the opportunity for the usage of these devices in a range of flexible circuits, active matrix displays and flexible bio-sensors.

6.7 Polarization of SAND

Information on the SAND-semiconductor interface can be obtained from the nature of hysteresis and its variation with *T*. In order to understand the origin of low interface disorder and high performance of the SAND based PFETs, it is essential to probe the origin of polarization in SAND. The SAND structure is a hybrid structure consists of multi-layered structures of HfO_x and PAE molecule. Thus, the effective polarization (P_{eff}) has contribution from the atomic dipoles of HfO_x, molecular dipoles of π-PAE molecule and the ionic polarization of the Br^- ion. Each of the polarization components has a distinctive signature on the transport energetic which can be varied by external parameters like temperature and light.

6.7.1 Temperature dependent study

Temperature dependent transport measurements were performed on SAND based *p*-FETs and the hysteresis was measured.

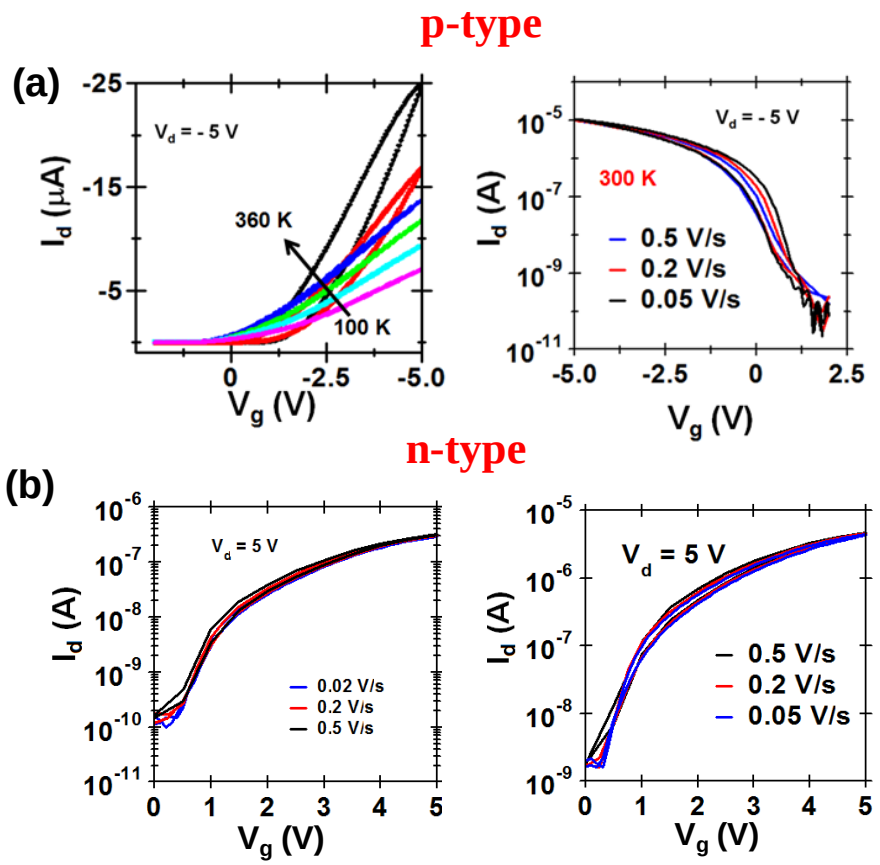


Figure 6.16: *Transconductance hysteresis plots with T and sweep rate for SAND PFETs fabricated with (a) PBTOR and (b) N2200 semiconducting layer. Typical device dimensions were L = 60 μm, W = 1 mm, SAND thickness ~ 18 nm.*

In general, if the transport is trap dominated then the hysteresis decreases with *T*. This is because, as the *T* increases, the charge carriers have enough energy to be activated to the transport levels. Hence, minimal hysteresis is obtained in the forward and backward sweep of the V_g. However, if the traps originate due to ionic contribution, then with increase in *T* more ions start contributing to the P_{eff} and hence hysteresis increases with *T* (**Figure: 6.16a**). The highlights of the *T* dependent hysteresis for the SAND-PFETs are: (i) increase in the area under hysteresis with *T*; (ii) increased hysteresis with slower scan rate (iii) change in the direction of hysteresis from clockwise at low *T* to anticlockwise as *T* approaches 300 K.

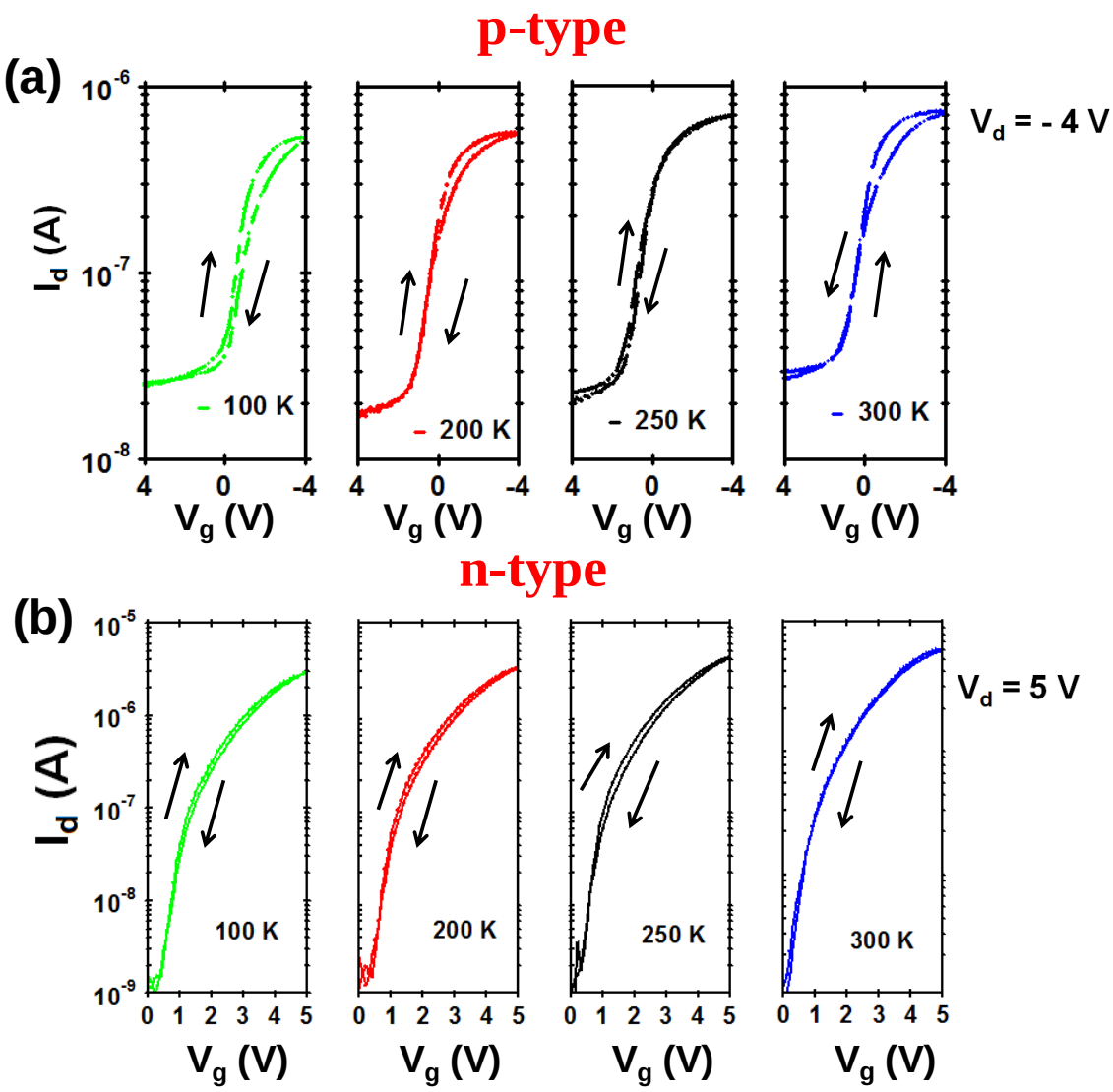


Figure 6.17: *Transconductance hysteresis plots with T showing the change in the direction of hysteresis for SAND PFETs fabricated with (a) PBTOR and (b) N2200 semiconducting layer. Typical device dimensions were L = 60 μm, W = 1 mm, SAND thickness ~ 18 nm.*

Increase in hysteresis with *T* and slower scan rate indicates the existence of dominant contribution of the ionic polarization at the transport interface for SAND based PFETs (**Figure: 6.16a**). It is informative to analyze the direction of hysteresis in transconductance to further understand the interface transport mechanism. A change in the direction of hysteresis with *T* points to the modification of the transport mechanism with polarization variation of the dielectric. At low *T*, the hysteresis follows a clock-wise direction and a transition to anticlockwise direction of hysteresis is observed as the *T* increases (**Figure: 6.17a**). This trend can be attributed to the variation in the source of interface disorder from electrostatic potentials to ionic potentials. Thus, the Br^- ions in the PAE plays a significant role in the effective dielectric constant for T > 280 K. The observed variation of area and direction of the hysteresis observed for SAND based *p*-FETs is not observed for *n*-FETs fabricated with N2200 semiconducting layer. This indicates no signature of ionic contribution in the hysteresis of the transconductance plots (**Figure: 6.16b**) which can be correlated to the inherent bulkiness of the PAE group.

6.8 Functional Interface

Polymer electronics has an added advantage of embedding multiple functionalities to the device structure which is relevant for circumventing issues originating from scaling of nano-electronic devices[28]. These functional PFETs have great technological relevance and can be utilized for light sensing, light emission, signal storage and sensors for medical diagnostics[28]. In this regard, several devices like: photo-transistors, memory transistors and light emitting transistors have been demonstrated[29]. The general strategy used for introducing functionalities in PFETs is by blending active semiconducting polymer or dielectric with photo-chromic materials[28]. However, the control of the electrical and optical properties in such blended systems is challenging. In addition, there are instances of self-assembled photo-chromic (SAP) layers at electrode or semiconductor interface which modulate the device performance[28]. However, the usage of SAP is limited to single layer and limited to devices with semiconductors which are vacuum deposited. Hence, there is a need to develop strategies to implement functionalities in a controlled manner for effective solution processed printable PFET devices. In this regard, a rationally designed self assembled nano-dielectric (SAND) structure is discussed as the functional moiety in the PFET device architecture.

The polarization in SAND structures has contribution from the atomic dipoles (P_{atom}) of HfO_x, molecular dipoles (P_{mol}) of PAE group and the ionic polarization (P_{ion}) from the native charge on the PAE group (**Figure: 6.18**). Moreover, the photoactive nature of the SAND dielectric layers opens the possibility to tune the interface conductance and charge density by external stimuli which has a significant impact on the device properties. The photo-chromic nature of the polar PAE molecule to switch between the isomeric cis (3.9 D) or trans-state (12.5 D) is utilized to follow the trends of polarization variation with illumination.

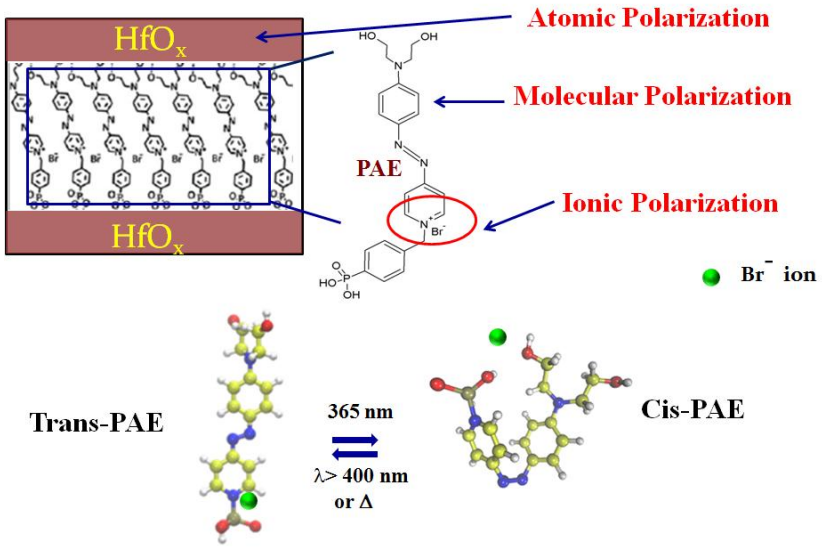


Figure 6.18: *Schematic showing the origin of different types of polarization in the SAND dielectric material.*

6.8.1 Photo-active capacitors

To study the effect of photo-excitation on SAND polarization, MIM capacitors were fabricated with transparent ITO coated glass electrodes and Au counter electrode. The capacitance of the 6L-SAND structures was monitored in dark and under illumination. Typical capacitance of the 6L-SAND structures at 100 Hz was obtained to be 0.2 $\mu F/cm^2$ in dark condition which increases to 0.5 $\mu F/cm^2$ upon UV ($\lambda \sim 365$ nm) illumination for 30 mins (**Figure: 6.19**). The capacitance change introduced by UV illumination can be restored back to its original magnitude of 0.25 $\mu F/cm^2$ upon visible ($\lambda \sim 400$ nm) illumination for 30 - 35 mins. This reversible cycling of the capacitance can be retained for 10^2 cycles without significant degradation of the capacitance properties.

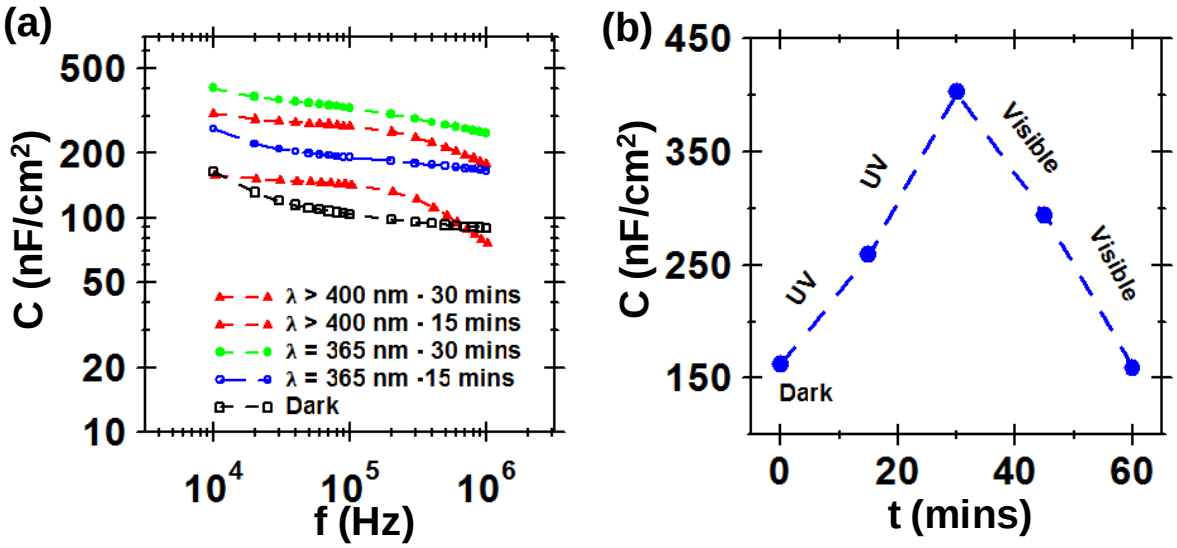


Figure 6.19: *Variation of the (a) C-f behavior and (b) capacitance for SAND-6L with illumination.*

This feature can be explained from the photo-isomerization of the azo-moiety. The isomerization of the PAE from the thermodynamically stable trans-state to the cis-state under UV illumination allows free movement of the Br^- ions. This increases the ionic contribution at the SAND-semiconductor interface, which gets reflected in the increased capacitance with UV illumination. Visible illumination results in the reversible isomerization to the trans-state of PAE and a decrease in ionic contribution which results in lower capacitance of the SAND. To further confirm the isomerization of the SAND dielectric structure absorption spectra was monitored under UV and visible illumination. The spectrum indicates a decrease in the absorption for $\lambda < 400$ nm upon UV illumination, indicating the possibility of isomerization. Visible excitation results in regaining the original spectra which relates to the trans-state of the PAE molecule.

6.8.2 Functional PFETs

The photo-tunability of the SAND structure is utilized to fabricate functional PFETs. Optically responsivity of the SAND-PFETs provides an access to modify the channel conductance and charge density without gate bias. Transparent ITO gate, based bottom gate top contact structures were fabricated to carry out photo-excitation measurements. The SAND dielectric structure was self-assembled using the procedure as explained in section 6.4 earlier. This was followed by coating both PBTOR semiconducting layer for *p*-FETs and N2200 for *n*-FETs. PFETs were then completed by coating Au S-D

electrode on the semiconducting layer. These SAND based PFETs showed well defined linear and saturation response with the performance parameters are as follows: μ_{FET}^{h} ~ 2 – 2.5 $cm^2V^{-1}s^{-1}$, μ_{FET}^{e} ~ 0.1 - 0.5 $cm^2V^{-1}s^{-1}$ respectively and I_{on}/I_{off} ~ 10^4 – 10^5.

Photo-excitation experiments were then performed on these PFET devices. The transconductance plots were monitored with photo-illumination (**Figure: 6.20**). Photo-excitation of dielectric layer at 300 K with UV illumination increases the area under hysteresis which can be reversed using visible illumination. This can be directly attributed to increased ionic polarization at the interface due to the isomerization process. As the ionic contribution at the transport interface increases, hysteresis in the transconductance plot increases. In addition, ions at the interface can also introduce defects in the semiconducting layer which can also result in hysteresis[30]. However, at low (T ~ 150 K) when the ionic motion is restricted no change in hysteresis is observed with the photo-excitation of the dielectric layer (**Figure: 6.20**).

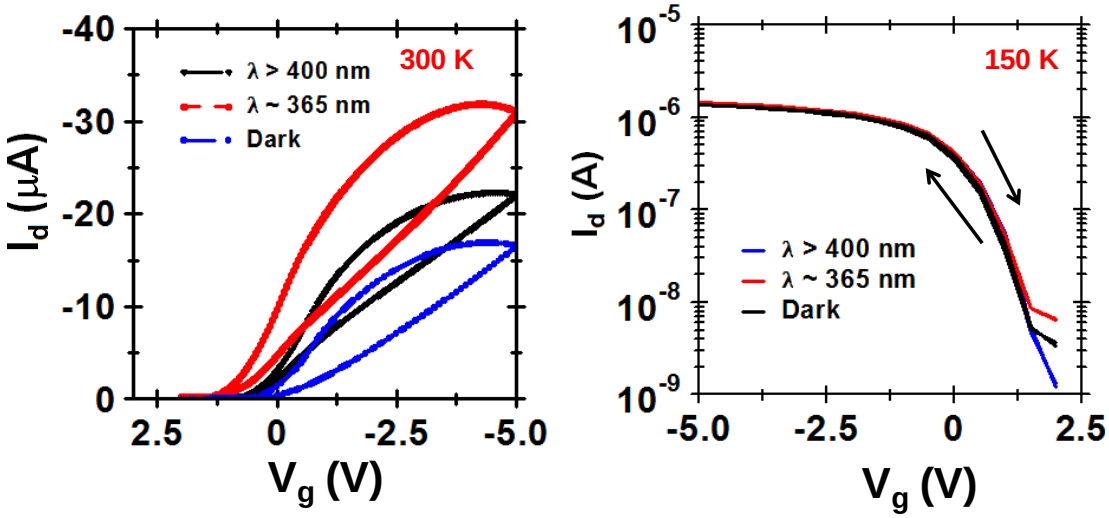


Figure 6.20: *Variation of the transconductance plot with illumination of UV (λ ~ 365 nm) , visible (λ > 400 nm) and dark conditions.*

Furthermore, the observed variation in direction of hysteresis with change in *T* is due to the different type of interface disorders originating from electrostatic potential or ion induced defects. Similar, measurements performed under illumination, indicate the hysteresis reversal occurring at lower *T* (~ 240 K) indicating more contribution from ionic polarization to the effective dielectric constant of the SAND structure. This ability of interface modulation with light and bias was utilized to obtain flip-flop memory circuits

with the capability of digitally commuting between optical and electrical memory (**Figure: 6.21**). In the optical domain, the SAND based flip-flop circuits operate in three states corresponding to UV illumination (+1), visible illumination (0) and dark (-1). Similarly, precise control on the threshold shift of the hysteresis and the area under the hysteresis was also obtained by electrical control.

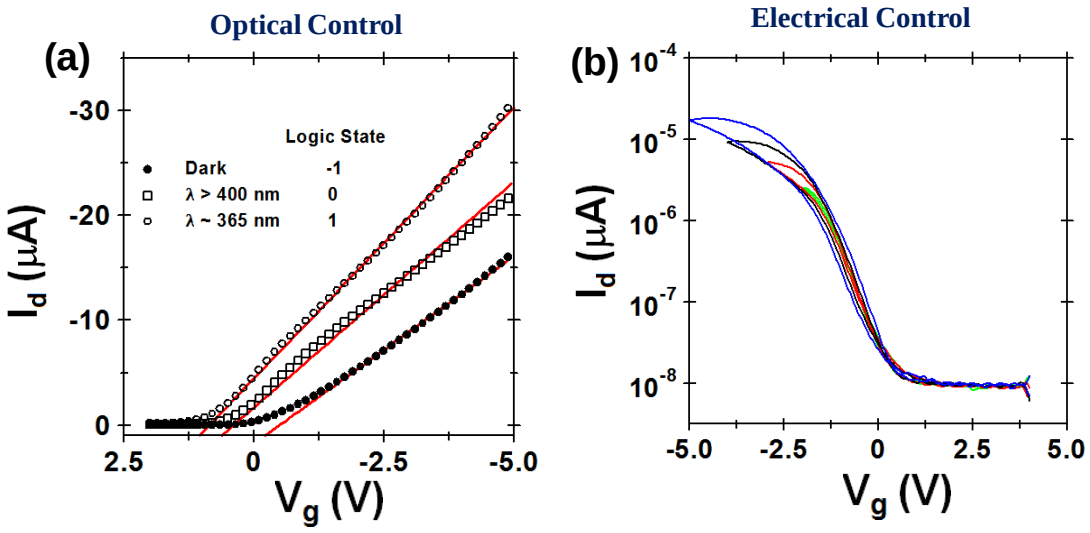


Figure 6.21: *Demonstration of memory in the SAND based PFET devices (a) Optical memory and (b) electrical memory with different magnitude of V_g.*

6.9 Conclusions

In summary, this chapter describes a technique for wafer scale integration of SAND dielectrics based polymeric transistors, logic circuits and optoelectronic memory. The SAND dielectric structures consisting of densely packed ordered dipole results in improved polarizability, enhanced relaxation dynamics and minimal leakage current which are well suited for optimal device operations. The corresponding PFETs exhibit μ_{FET} > 2.0 $cm^2V^{-1}s^{-1}$, switching-speed of 150 ns and operating-voltage of |1 V|. Temperature dependent transport studies provide considerable insight on the disorder dynamics which can be correlated to the microscopic structure and aggregation. The large area uniformity of the dielectric layer is utilized to develop fast switching (~ 5 MHz) low power arrays of PLC. High performance of these polymer circuits is attributed to a combination of factors originating from self-assembled ordered dipoles of the dielectric which supports high

frequency relaxation of the dielectric layer and appropriate interface which enhances the inherent transport.

Furthermore, this study demonstrates a unique approach of reversible photo-control of the interfacial properties with rationally designed dielectric structures. The present study reveals a novel approach for controlled installation of desired functionalities onto electronic devices, which is difficult and rare so far. This ability to engineer the interface is demonstrated in the observed crossover in disorder mechanism from electrostatic dipolar disorder to ion induced disorder in the transistor characteristics. The tunable interface is then utilized to obtain optoelectronic memory circuits.

References

1. (a) Kanimozhi, C.; Yaacobi-Gross, N.; Chou, K. W.; Amassian, A.; Anthopoulos, T. D.; Patil, S., Diketopyrrolopyrrole–Diketopyrrolopyrrole-Based Conjugated Copolymer for High-Mobility Organic Field-Effect Transistors. *J. Am. Chem. Soc.* **2012,** *134* (40), 16532-16535; (b) Li, J.; Zhao, Y.; Tan, H. S.; Guo, Y.; Di, C.-A.; Yu, G.; Liu, Y.; Lin, M.; Lim, S. H.; Zhou, Y.; Su, H.; Ong, B. S., A stable solution-processed polymer semiconductor with record high-mobility for printed transistors. *Sci. Rep.* **2012,** *2*.

2. (a) Yoon, M.-H.; Kim, C.; Facchetti, A.; Marks, T. J., Gate Dielectric Chemical Structure−Organic Field-Effect Transistor Performance Correlations for Electron, Hole, and Ambipolar Organic Semiconductors. *Journal of the American Chemical Society* **2006,** *128* (39), 12851-12869; (b) Ortiz, R. P.; Facchetti, A.; Marks, T. J., High-k Organic, Inorganic, and Hybrid Dielectrics for Low-Voltage Organic Field-Effect Transistors. *Chemical Reviews* **2009,** *110* (1), 205-239.

3. Luzio, A.; Ferré, F. G.; Fonzo, F. D.; Caironi, M., Hybrid Nanodielectrics for Low-Voltage Organic Electronics. *Advanced Functional Materials* **2013**, n/a-n/a.

4. (a) Herlogsson, L.; Noh, Y.-Y.; Zhao, N.; Crispin, X.; Sirringhaus, H.; Berggren, M., Downscaling of Organic Field-Effect Transistors with a Polyelectrolyte Gate Insulator. *Adv. Mat.* **2008,** *20* (24), 4708-4713; (b) Cho, J. H.; Lee, J.; Xia, Y.; Kim, B.; He, Y.; Renn, M. J.; Lodge, T. P.; Daniel Frisbie, C., Printable ion-gel gate dielectrics for low-voltage polymer thin-film transistors on plastic. *Nat. Mat.* **2008,** *7* (11), 900-906.

5. Noh, Y.-Y.; Zhao, N.; Caironi, M.; Sirringhaus, H., Downscaling of self-aligned, all-printed polymer thin-film transistors. *Nat Nano* **2007,** *2* (12), 784-789.

6. Li, J.; Sun, Z.; Yan, F., Solution Processable Low-Voltage Organic Thin Film Transistors with High-k Relaxor Ferroelectric Polymer as Gate Insulator. *Advanced Materials* **2012,** *24* (1), 88-93.

7. (a) Veres, J.; Ogier, S. D.; Leeming, S. W.; Cupertino, D. C.; Mohialdin Khaffaf, S., Low-k Insulators as the Choice of Dielectrics in Organic Field-Effect Transistors. *Adv. Funct. Mat.* **2003,** *13* (3), 199-204; (b) Senanayak, S. P.; Guha, S.; Narayan, K. S., Polarization fluctuation dominated electrical transport processes of polymer-based ferroelectric field effect transistors. *Phys. Rev. B* **2012,** *85* (11), 115311; (c) Hulea, I. N.; Fratini, S.; Xie, H.; Mulder, C. L.; Iossad, N. N.; Rastelli, G.; Ciuchi, S.; Morpurgo, A. F., Tunable Frohlich polarons in organic single-crystal transistors. *Nat. Mat.* **2006,** *5* (12), 982-986.

8. Zhang, B.; Liu, Y.; Agarwal, S.; Yeh, M.-L.; Katz, H. E., Structure, Sodium Ion Role, and Practical Issues for β-alumina as a High-k Solution-Processed Gate Layer for Transparent and Low-Voltage Electronics. *ACS Applied Materials & Interfaces* **2011,** *3* (11), 4254-4261.

9. Herlogsson, L.; Crispin, X.; Tierney, S.; Berggren, M., Polyelectrolyte-Gated Organic Complementary Circuits Operating at Low Power and Voltage. *Adv. Mat.* **2011,** *23* (40), 4684-4689.

10. Senanayak, S. P.; Narayan, K. S., Strategies for Fast-Switching in All-Polymer Field Effect Transistors. *Advanced Functional Materials* **2014**, n/a-n/a.

11. (a) Austin, M. D.; Chou, S. Y., Fabrication of 70 nm channel length polymer organic thin-film transistors using nanoimprint lithography. *Appl. Phys. Lett.* **2002,** *81* (23), 4431-4433; (b) Di, C.-a.; Yu, G.; Liu, Y.; Xu, X.; Song, Y.; Wang, Y.; Sun, Y.; Zhu, D.; Liu, H.; Liu, X.; Wu, D., Noncoplanar organic field-effect transistor based on copper phthalocyanine. *Appl. Phys. Lett.* **2006,** *88* (12), 121907.

12. Hirose, T.; Nagase, T.; Kobayashi, T.; Ueda, R.; Otomo, A.; Naito, H., Device characteristics of short-channel polymer field-effect transistors. *Applied Physics Letters* **2010,** *97* (8), -.

13. (a) Genenko, Y. A.; Zhukov, S.; Yampolskii, S. V.; Schütrumpf, J.; Dittmer, R.; Jo, W.; Kungl, H.; Hoffmann, M. J.; von Seggern, H., Universal Polarization Switching Behavior of Disordered Ferroelectrics. *Adv. Funct. Mat.* **2012,** *22* (10), 2058-2066; (b) Jiang, A. Q.; Lee, H. J.; Hwang, C. S.; Scott, J. F., Sub-Picosecond Processes of Ferroelectric Domain Switching from Field and Temperature Experiments. *Adv. Funct.*

Mat. **2012,** *22* (1), 192-199; (c) Dunn, L.; Dodabalapur, A., Temperature dependent transient velocity and mobility studies in an organic field effect transistor. *J. Appl Phys.* **2010,** *107* (11), 113714.

14. (a) Yoon, M.-H.; Facchetti, A.; Marks, T. J., σ-π molecular dielectric multilayers for low-voltage organic thin-film transistors. *Proc. Natl. Acad. Sci. USA* **2005,** *102* (13), 4678-4682; (b) Everaerts, K.; Emery, J. D.; Jariwala, D.; Karmel, H. J.; Sangwan, V. K.; Prabhumirashi, P. L.; Geier, M. L.; McMorrow, J. J.; Bedzyk, M. J.; Facchetti, A.; Hersam, M. C.; Marks, T. J., Ambient-Processable High Capacitance Hafnia-Organic Self-Assembled Nanodielectrics. *Journal of the American Chemical Society* **2013,** *135* (24), 8926-8939.

15. (a) DiBenedetto, S. A.; Facchetti, A.; Ratner, M. A.; Marks, T. J., Molecular Self-Assembled Monolayers and Multilayers for Organic and Unconventional Inorganic Thin-Film Transistor Applications. *Advanced Materials* **2009,** *21* (14-15), 1407-1433; (b) Ha, Y.-G.; Everaerts, K.; Hersam, M. C.; Marks, T. J., Hybrid Gate Dielectric Materials for Unconventional Electronic Circuitry. *Accounts of Chemical Research* **2014**.

16. Sangwan, V. K.; Ortiz, R. P.; Alaboson, J. M. P.; Emery, J. D.; Bedzyk, M. J.; Lauhon, L. J.; Marks, T. J.; Hersam, M. C., Fundamental Performance Limits of Carbon Nanotube Thin-Film Transistors Achieved Using Hybrid Molecular Dielectrics. *ACS Nano* **2012,** *6* (8), 7480-7488.

17. Sangwan, V. K.; Jariwala, D.; Everaerts, K.; McMorrow, J. J.; He, J.; Grayson, M.; Lauhon, L. J.; Marks, T. J.; Hersam, M. C., Wafer-scale solution-derived molecular gate dielectrics for low-voltage graphene electronics. *Applied Physics Letters* **2014,** *104* (8), -.

18. Everaerts, K.; Zeng, L.; Hennek, J. W.; Camacho, D. I.; Jariwala, D.; Bedzyk, M. J.; Hersam, M. C.; Marks, T. J., Printed Indium Gallium Zinc Oxide Transistors. Self-Assembled Nanodielectric Effects on Low-Temperature Combustion Growth and Carrier Mobility. *ACS Applied Materials & Interfaces* **2013,** *5* (22), 11884-11893.

19. (a) Cao, Q.; Xia, M. G.; Shim, M.; Rogers, J. A., Bilayer Organic–Inorganic Gate Dielectrics for High-Performance, Low-Voltage, Single-Walled Carbon Nanotube Thin-Film Transistors, Complementary Logic Gates, and p–n Diodes on Plastic Substrates. *Advanced Functional Materials* **2006,** *16* (18), 2355-2362; (b) Acton, B. O.; Ting, G. G.; Shamberger, P. J.; Ohuchi, F. S.; Ma, H.; Jen, A. K. Y., Dielectric Surface-Controlled Low-Voltage Organic Transistors via n-Alkyl Phosphonic Acid Self-Assembled Monolayers on High-k Metal Oxide. *ACS Applied Materials & Interfaces* **2010,** *2* (2), 511-520.

20. Chidsey, C. E. D.; Loiacono, D. N., Chemical functionality in self-assembled monolayers: structural and electrochemical properties. *Langmuir* **1990,** *6* (3), 682-691.

21. Ha, Y.-g.; Emery, J. D.; Bedzyk, M. J.; Usta, H.; Facchetti, A.; Marks, T. J., Solution-Deposited Organic–Inorganic Hybrid Multilayer Gate Dielectrics. Design, Synthesis, Microstructures, and Electrical Properties with Thin-Film Transistors. *Journal of the American Chemical Society* **2011,** *133* (26), 10239-10250.

22. Scott, J. F., Switching of Ferroelectrics Without Domains. *Adv. Mat.* **2010,** *22* (46), 5315-5317.

23. Sangwan, V. K.; Jariwala, D.; Filippone, S. A.; Karmel, H. J.; Johns, J. E.; Alaboson, J. M. P.; Marks, T. J.; Lauhon, L. J.; Hersam, M. C., Quantitatively Enhanced Reliability and Uniformity of High-κ Dielectrics on Graphene Enabled by Self-Assembled Seeding Layers. *Nano Letters* **2013,** *13* (3), 1162-1167.

24. Sze, S. M., Physics of Semicnoductor devices.

25. (a) Yan, H.; Chen, Z.; Zheng, Y.; Newman, C.; Quinn, J. R.; Dotz, F.; Kastler, M.; Facchetti, A., A high-mobility electron-transporting polymer for printed transistors. *Nature* **2009,** *457* (7230), 679-686; (b) Guo, X.; Quinn, J.; Chen, Z.; Usta, H.; Zheng, Y.; Xia, Y.; Hennek, J. W.; Ortiz, R. P.; Marks, T. J.; Facchetti, A., Dialkoxybithiazole: A New Building Block for Head-to-Head Polymer Semiconductors. *Journal of the American Chemical Society* **2013,** *135* (5), 1986-1996.

26. Noriega, R.; Rivnay, J.; Vandewal, K.; Koch, F. P. V.; Stingelin, N.; Smith, P.; Toney, M. F.; Salleo, A., A general relationship between disorder, aggregation and charge transport in conjugated polymers. *Nat Mater* **2013,** *12* (11), 1038-1044.

27. Rivnay, J.; Toney, M. F.; Zheng, Y.; Kauvar, I. V.; Chen, Z.; Wagner, V.; Facchetti, A.; Salleo, A., Unconventional Face-On Texture and Exceptional In-Plane Order of a High Mobility n-Type Polymer. *Adv. Mat.* **2010,** *22* (39), 4359-4363.

28. Orgiu, E.; Samorì, P., 25th Anniversary Article: Organic Electronics Marries Photochromism: Generation of Multifunctional Interfaces, Materials, and Devices. *Advanced Materials* **2014,** *26* (12), 1827-1845.

29. Zhang, H.; Guo, X.; Hui, J.; Hu, S.; Xu, W.; Zhu, D., Interface Engineering of Semiconductor/Dielectric Heterojunctions toward Functional Organic Thin-Film Transistors. *Nano Letters* **2011,** *11* (11), 4939-4946.

30. Wang, S.; Ha, M.; Manno, M.; Daniel Frisbie, C.; Leighton, C., Hopping transport and the Hall effect near the insulator–metal transition in electrochemically gated poly(3-hexylthiophene) transistors. *Nat Commun* **2012,** *3*, 1210.

Chapter 7

Summary and Future Directions

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Summary and Future Directions

The thesis addresses fundamental issues relating to the performance of flexible microelectronic circuits and implements strategies to make them feasible for practical applications. The performance parameters of these devices are dependent on the functionality of its basic building block: the PFET. Specifically, the thesis presents methods to enhance the field effect mobility (μ_{FET}), switching speed (t_{switch}) and decrease the operating voltage as well as the power consumption of PFETs.

The first part of the thesis discussed the charge transport mechanism in the new class of DPP based high μ_{FET} polymers. With the advent of these new materials the charge transport mechanism was studied within a broader framework which addressed both hopping as well as extended transport in disordered systems. Comprehensive studies performed by different combination of dielectric and DPP semiconductors points to the efficacy of the amphiphillic design in the polymer for enhanced transport. A general equivalence of the μ_{Hall} and μ_{FET} along with the negative coefficient of μ_{FET} indicates the existence of a band-like transport mechanism in this polymer. Combination of factors originating from rationale molecular design, optimum dielectric and transport interface, interconnected aggregates and co-planar conjugated core of the polymer are the general pre-requisites for high μ_{FET} and extended transport.

The next part of the thesis, discussed the origin of disorder in high-*k* dielectric based PFETs. PVDF based dielectric materials which fall in different class of ferroelectric (FE), paraelectric (PE) and random paraelectric (*r*-PE) dielectric, and have similar *k* were utilized in the PFET geometry. A weak activation behavior of 15 meV was observed for FE-FETs which increases to 0.1 – 0.2 eV for PE dielectric based PFETs. In general, the variation in the activation energy of transport is attributed to the broadening of the DOS because of electrostatic disorder. However, the observation of this large variation in activation energy for devices fabricated from dielectric layer with similar *k* led to the conclusion that disorder

at the transport interface of a PFET is dependent on the nature of dielectric material and not the dielectric constant.

In the next section, the issue of slow switching response of printed polymer transistors is discussed. A combination of approach consisting of the ordered interface obtained from FE materials as well as suitable device and dipole engineering resulted in enhancing the transient response of PFETs. The procedure involved: (i) pre-poling the FE dielectric to initiate the domain nucleation and (ii) minimizing the parasitic capacitance by fabricating devices with aligned patterned electrodes. These modified device structures and the corresponding all-polymer logic circuits demonstrate switching frequency of 4 MHz for printable channel length. These studies conclude that the requisites for fast switching polymer circuits are: ordered dielectric dipole, semiconductors with high μ_{FET} and isolated conjugated core.

The final part discussed strategies for obtaining high performing PFETs with low-operating voltage. In general, PFETs are limited by the high operating voltage which limits its usability in portable applications. A strategy based on multilayered self-assembled nano-dielectric structures with precise control on thickness, leakage current (0.1 pA) and capacitance (0.6 $\mu F/cm^2$) were utilized to obtain PFETs operating at |1 V| and typical μ_{FET} ~ 2.4 $cm^2V^{-1}s^{-1}$. These structures were then utilized to obtain large area polymer logic circuits with switching frequency of ~ 5 MHz. The SAND structure provides optimum transport interface with low disorder for enhanced static performance and the densely packed ordered dipoles enhances the dielectric relaxation and the dynamic response of the PFETs. Furthermore, the optical and electrical control of the SAND polarization was utilized to design PFETs with functional interface which were controlled by external stimuli. On a scientific front, the optoelectronic tuning of the transport interface allowed the possibility to probe the origin of polarization in the multi-layered SAND structure, and on the technological side, this feature was utilized to obtain memory circuits with the capability of digitally commuting between optical and electrical memory.

In summary, this thesis reports a combination of efficient strategies to obtain PFETs with performance comparable to a-Si based FETs which is a step towards realizing the full potential envisaged for flexible electronics. These sets of studies open up the possibility for exploring a range of 2D quantum phenomena which are not explored for disordered polymeric materials. These studies would then culminate in obtaining a general theory for charge transport in organic materials by relating different sources of disorder originating

from microscopic and macroscopic properties of these materials. In terms of practical device applications, the PFETs designed from these studies can now be utilized to drive display units with a refresh rate of 1 MHz. Functional PFETs designed from this can also be utilized for bio-sensing and mapping cellular potential which will pave way for novel applications, generally believed to be infeasible with inorganic electronics. A detailed studies of the degradation and reliability of organic-electronic devices can be performed to increase the life-time of these device and enable these devices as an emerging technology option.

Chapter 7: Summary

Appendix 1

Transistor equations derivation for FE-FET:

Basic Assumptions for the derivation -:

1. OFETs with p-type semiconductor and P(VDF-TrFE) / PVDF-TrFE gate dielectric.

2. The ferroelectric layer is not pre-poled by applying $V_S = V_D = 0V$; $V_G < 0V$

3. The FE-FET shows remnant polarization in the transconductance measurements. The remnant polarization, P_r, is attributed to dipoles in the crystalline phase of P(VDF-TrFE). In addition, the total polarization also involves contribution from dipoles in the amorphous phase, which is proportional to the electric field inside the medium.

4. The poling process is assumed to be stable, which means further poling does not have additional effects on P_r; and P_r is considered to be constant under variations of small electric fields.

The polarization due to the ferroelectric dielectric has non-linear contribution in additional to the linear polarization

$$P_{tot} = P_{lin} + P_{nl} = P_{lin} + 2P_r - P_{sat},$$

where, P_{lin} is the linear contribution

P_r is the remnant polarization

P_{sat} is saturation polarization.

In the approximation:

At low T, $P_{tot} = P_{lin} + P_r$ (as $P_r \sim P_{sat}$)

High T, $P_{tot} = P_{lin} - P_{sat}$ (as $P_r << P_{sat}$).

Charge at the semiconductor-dielectric interface is given by

$$Q = \varepsilon_0 \varepsilon_r \frac{(V_i + V_0)}{d}$$

and V_0 comes from

$$P_{nl} = \frac{\varepsilon_0 \varepsilon_r V_0}{d}$$

Since V_i can also be expressed as $(V_g - V_x)$.

$$Q = C\,(V_g + V_0 - V_x)$$

Thus I_{ds} is calculated over the entire channel in the saturation regime with the assumption that semiconductor thickness $d << L$.

$$I_{ds} = \mu W/L \int_0^{V_d} Q dV_x$$

Substituting for Q and with the approximation, $V_d \sim V_g + V_o$

$$I_{ds} = \mu C \frac{W}{L} (V_g + V_0 - V_t)^2$$