Surface Engineering and Lateral Charge Transport Studies in Organic and Hybrid Organic Inorganic Systems

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A Thesis Submitted in Partial Fulfillment of the Requirement for the Degree of

Doctor of Philosophy

by

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Declaration

I hereby declare that the matter embodied in this thesis titled **"Surface Engineering and Lateral Charge Transport Studies in Organic and Hybrid Organic Inorganic Systems"** is the result of investigations carried out by me at the Chemistry and Physics of Materials Unit, Jawaharlal Nehru Centre for Advanced Scientific Research, Bangalore-India under the supervision of Prof. K. S. Narayan and that it has not been submitted elsewhere for the award of any degree or diploma. In keeping with the general practice reporting scientific observations, due acknowledgment has been made whenever the work described is based on the finding of other investigators.

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Certificate

I hereby certify that the matter embodied in this thesis entitled "*Surface Engineering and Lateral Charge Transport Studies in Organic and Hybrid Organic-Inorganic Systems*" has been carried out by Mr. Ashar A.Z at the Molecular Electronics Laboratory, Chemistry and Physics of Materials Unit, Jawaharlal Nehru Centre for Advanced Scientific Research, Bangalore, India under my supervision and that it has not been submitted elsewhere for the award of any degree or diploma.

Prof. K. S. Narayan

(Research Supervisor)

Dedicated to

My Parents, Wife and Arja.

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List of Publications

- A. Z. Ashar, K. S. Narayan, Electric field induced ferroelectric-surface modification for high mobility organic field effect transistors. *Org. Electron.* **2017**, *42*, 8-12.
- A. Z. Ashar**,** Ganesh. N and K. S. Narayan, Hybrid Perovskite Based Position Sensitive Detectors. *Adv. Electron. Mater.* **2017,** 1700362.
- A. Z. Ashar and K. S. Narayan, Electrical Transport and Photocurrent Microscopy Studies in HOIP lateral MSM devices. **2018** (manuscript under preparation).
- Suman Banerjee, A. Z. Ashar, Raaghesh Vijayan, Ganesh. N, Prashant Kumar and K. S. Narayan, Photocurrent imaging of large-area solar cells and modules at micron level spatial resolution, **2017** (manuscript under review).
- Nagesh B. Kolhe, A. Z. Ashar, K. S. Narayan and S. K. Asha, Naphthalene Diimide Copolymers with Oligo(p-phenylenevinylene) and Benzobisoxazole for Balanced Ambipolar Charge Transport. Macromolecules **2014,** *47 (7),* 2296.
- B. Saibal, A. Z. Ashar, R. Nandini Devi K. S. Narayan and S. K. Asha. Nanostructured Donor-Acceptor Self Assembly with Improved Photoconductivity. *ACS Appl. Mater. Interfaces* **2014**, *6 (21),* 19434– 19448
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- Manisha Tomar, A. Z. Ashar, K. S. Narayan and Josemon Jacob. Tuning the HOMO Energy Levels in Quinoline and Biquinoline Based Donor-Acceptor Polymers. *J. Polym. Res.* **2016**, *23 (3),* 1– 9.
- Priya Singla, Nick Van Steerteghem, Navdeep Kaur, A. Z. Ashar, Paramjit Kaur, Koen Clays, K. S. Narayan and Kamaljit Singh. Multifunctional geometrical isomers of ferrocene-benzo[1,2-b:4,5-b′]difuran-2,6-(3H,7H)-dione adducts: second-order nonlinear optical behavior and charge transport in thin film OFET devices. *J. Mater. Chem. C* **2017**, *5 (3),* 697– 708.

Synopsis

A range of devices based on lateral transport parameters in semiconducting polymers and hybrid perovskite materials are studied in this thesis. The strong dependence of dielectric morphology and electrostatics on organic field effects transistors (OFETs) performance are presented. A choice of lateral Metal-Semiconductor-Metal (MSM) device structures of hybrid organic-inorganic perovskites (HOIP) are investigated.

The first part of the thesis discusses strategy for realizing improved charge transport in functional OFETs using an ordered dielectric surface. Semicrystalline, ferroelectric polymer P(VDF-TrFE) is used as the dielectric layer in the OFET. Dielectric polarization properties of the P(VDF-TrFE) are tuneable according to their processing conditions like temperature and external field. Randomly oriented polar domains in ferroelectric dielectric limits the charge transport and switching speed of the OFETs. The dielectric layer surface is modified by applying lateral electric field during the curing of the P(VDF-TrFE) film. Field effect mobility (μ_{FET}) of the semiconductor gets enhanced by a factor >300 % in devices fabricated on pre-poled P(VDF-TrFE) dielectric layer. Measurements using piezo force response microscopy reveals a reduced contrast of in-plane polarization in pre-poled P(VDF-TrFE) dielectrics as compared to non-poled dielectrics. The studies indicate that improvement in the dipolar order at the interface assists in field effect mobility (μ_{FET}) enhancement.

The second part of the thesis focuses on HOIP-based lateral Metal-Semiconductor-Metal (MSM) structures. Current-voltage (I-V) characteristics of MSM

structures with symmetric (Aluminum(Al)–Aluminum(Al), Gold(Au)-Gold(Au)) and asymmetric (Aluminum(Al)-Gold(Au)) electrodes having a varying channel length of 10 μm – 70 μm were studied under dark and light conditions. Symmetric I-V characteristics were observed in the entire set of Au-HOIP-Au devices. Asymmetric I-V characteristics were observed in Al-HOIP-Au small channel length (< 18 μm) devices. Surface potential measurements using Kelvin probe force microscopy of Al-perovskite-Au indicate a higher potential at Al–perovskite interface compared to Au-HOIP interface in an unbiased condition. A marginally higher uniform potential extending to the channel up to ~20 μm is measured at Al-HOIP interface compared to Au-HOIP interface in an asymmetric structure, when a positive voltage is applied to Al electrode. Spatially resolved near-field photocurrent scanning measurement reveals dominant feature in the channel zone near the Al electrode under positive voltage bias. This behavior of local photocurrent is explained in terms of combined effect involving external and built-in fields and carrier diffusion length. The feature of the entire device I-V gradually becoming symmetric with an increase in channel length can be understood from this microscopic observation. Drift-diffusion model in such device configuration is used to understand the I-V behavior and local photocurrent profiles.

Fabrication and characterization of a lateral MSM structure based position sensitive detector (PSD) using hybrid perovskite as the active material are described in the next chapter of the thesis. The lateral device makes use of indium tin oxide as a common back electrode and gold fingers as the counter electrodes. Millimetre size 1D-PSD with very low roughness of the hybrid perovskite active layer is fabricated using additive mixed-antisolvent method. Differential lateral photovoltage between the two arms of the device showed a linear dependence on the position of light illumination.

Apart from the linearity and the large span of position sensing range, the PSD response is also characterized by a sizable responsivity. The results can be understood in the framework of the drift-diffusion model.

In summary, this thesis highlights lateral transport studies on ordered dielectric-semiconductor surface in functional OFET and lateral hybrid organic-inorganic perovskite structures.

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Abbreviations and Symbols

HOMO	Higher Occupied Molecular Orbital
LUMO	Lowest Unoccupied Molecular Orbital
a-Si	Amorphous Silicon
DOS	Density of States
FET	Field Effect Transistor
OFET	Organic Field Effect Transistor
PFET	Polymer Field Effect Transistor
TFT	Thin Film Transistor
FE	Ferroelectric
MSM	Metal-Semiconductor-Metal
HOIP	Hybrid Organic Inorganic Perovskite
PSD	Position Sensitive Detectors
LPV	Lateral Photovoltage
AFM	Atomic Force Microscope
PFM	Piezo response Force Microscopy
KPFM	Kelvin Probe Force Microscopy
NSOM	Near-field Scanning Optical Microscopy
SPCM	Scanning Photo Current Microscopy
XRD	X-ray diffraction

UV/VIS	Ultraviolet/Visible
I-V	Current-Voltage
P-E	Polarization-Electric field
SCR	Space Charge Region
μ_{FET}	Field effect mobility
ΔV_{ph}	Differential Photovoltage
J_{ph}	Photocurrent density
L_d	Carrier decay length
E_g	Bandgap Energy
E_F	Fermi energy level
k_BT	Room temperature thermal energy
ϕ_M	Metal work function
ϕ_S	Semiconductor work function

Chapter 1

Organic and Hybrid Organic Inorganic Semiconductors: An Overview

1.1 Introduction

Conventional electronics rely on inorganic semiconductors *viz.*, silicon, germanium, III-V compounds and oxide dielectrics. The device physics and mechanisms of charge transport in these materials are well understood. However, there has been a quest for new materials which offer other advantages such as mechanical strength, large optical window and ease of processability. The discovery of high electrical conductivity in polyacetylene by Shirakawa, Mcdiarmid, and Heeger in the seventies witnessed a surging interest in the research and development of conjugated polymer materials and devices associated with it.[1] Many forms of organic electronic materials with high performance and stability have emerged since then.[2] Three primary devices: organic light emitting diodes (OLEDs), organic photovoltaics (OPVs) and organic field effect transistors (OFETs) have set the pace of activities in the last two decades in this field which has enabled Organic electronics-based devices increasingly find their place in the commercial space.[3-5]

Lately, hybrid organic-inorganic perovskite (HOIP) materials which bring in the performance levels of inorganic systems and ease of processability of organic systems have been intensely pursued.[6] These materials have been primarily explored as an active semiconductor layer for solar cell devices and field effect transistors.[7-9] The LED applications based on these materials also appear to be promising.[10-12] Devices made

of either organic semiconductor or HOIP system include multiple interfaces which contribute to the factors determining the performance and stability of the device.

This thesis covers certain aspects of lateral transport in both these material systems. The underlying differences in the transport properties and the different approaches to understand and improve these properties form the central theme of the thesis. The effect of multiple factors *viz.*, surface microstructure, functional properties and interfacial energetics on the charge transport properties of these materials are also discussed in this thesis.

A brief summary and introduction to relevant topics pertaining to the thesis problems undertaken are described in the section below.

1.2 Organic Semiconductors

Organic semiconductors made of small of molecules were known for their conductive and photoresponsive properties from the 1950s onwards, but poor charge transport properties and low stability limited their application in electronic devices. This scenario changed with the advent of conjugated polymers in the 1970s.[1] Doped trans-polyacetylene having with conductivity ~10^5 S/m changed the perspective of the scientific community towards polymers and organic materials. The development of undoped polymer semiconductors resulted in new applications leading to potentially important technologies for photovoltaics and consumer electronics.[13] Organic materials offer high optical absorption, large oscillator strength along with the advantages of easy processing, lightweight, large area fabrication, and mechanical flexibility, all of which are highly desirable for electronic devices. Moreover, they are compatible with roll-to-roll processing that could significantly reduce device fabrication

cost, which increases the prospects of commercially using organic semiconductors in electronic devices. Today, the performance of polymer devices has exceeded the benchmark parameters set by a-Si based devices.[14, 15] The issue of material/device stability, which is one of the drawbacks stalling their commercialization has been addressed by new materials and optimized device structures.[16-21] The tremendous development of organic electronics is due to a combination of development of new high-performance materials design and thorough understanding of the transport physics of the materials. The next section provides the overview of charge transport physics in polymer semiconductors.

1.3 Charge Transport in Polymers

The energy levels in the organic semiconductors are different from that of their inorganic crystalline counterparts owing to weak intermolecular forces and poor periodicity. Whereas, the band structure in crystalline semiconductors results from strong covalent bonds between atoms in the lattice, which keep the interatomic spacing short enough to produce wide conduction and valence bands. High periodicity in crystalline structures also produces sharp band edges with a negligible density of states in the band gap. However, in a molecular crystal, the intermolecular van der Waals bonds are much weaker than the intramolecular covalent bonds.[22] Consequently, the resulting bands of molecular crystals are very narrow, with large bandwidths. Thermal vibrations (phonons) reduce the interaction between molecules, reducing the bandwidth even further. As a result of this narrow, vibration-sensitive bandwidth, charge transport in organic crystals is limited compared to that in inorganic solids.[23]

Polymer semiconductors are π-conjugated macromolecules, which contain a large number of repeating monomer units. While the bonds along the chain of each

polymer molecule are covalent, the different macromolecular chains are only linked via much weaker Van der Waals forces. Hence, polymer materials do not show a three-dimensional long-range order, although they can be crystalline over a small length scale (semi-crystalline).

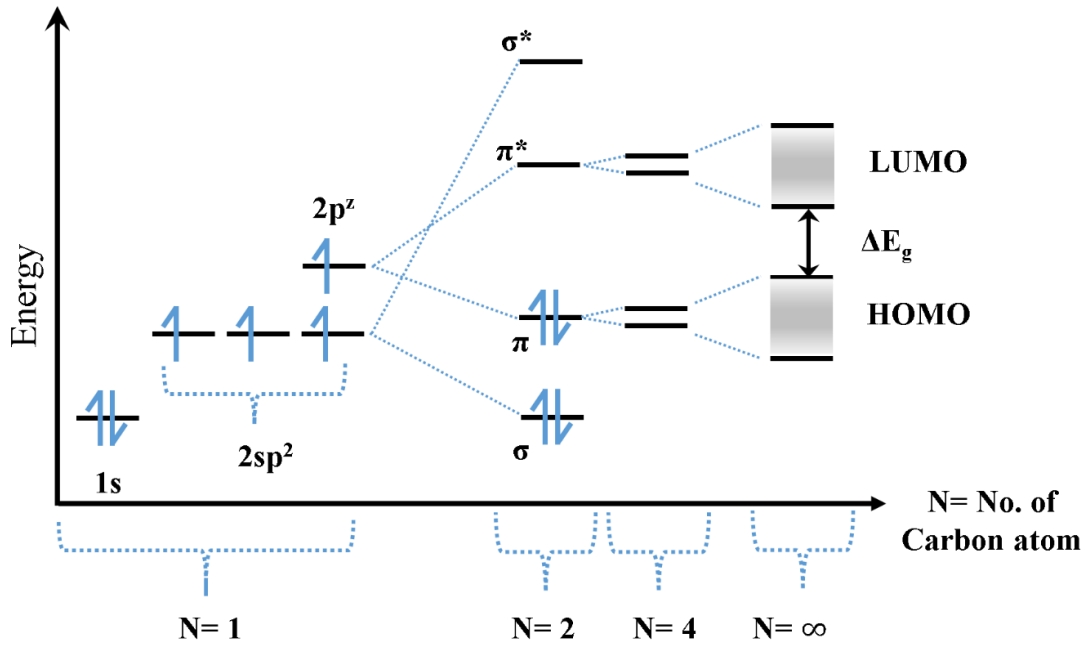

Figure 1.1: *Schematic representation of the energy levels in conjugated molecules. Molecular orbital formed between C=C bond results in bonding (σ & π) and antibonding (σ* & π*) energy levels. Increasing number of C atoms leads to further splitting and the formation of quasi-continuous bands.*

A covalent bond formation can be described using the theory of linear combination of atomic orbitals (LCAO). Alternating single and double bonds of carbon atoms form the backbone of the π-conjugated polymer chains. This configuration is formed by the sp^2 hybridization of C-atomic orbitals where the 2s and two of the 2p of adjacent carbon molecules form strong bonding (σ) and antibonding (σ*) molecular

orbitals. The remaining p_z atomic orbitals overlap to form a relatively weak bonding (π) and antibonding (π^*) molecular orbitals, which forms the frontier orbitals of the molecule enabling the charge conduction along the polymer backbone. The π and π^* molecular orbitals resemble the valence and conduction bands of inorganic semiconductors and are called as Highest occupied molecular orbital (HOMO) and Lowest unoccupied molecular orbital (LUMO) respectively. Relatively weak bonding strength in these orbitals allows the delocalization of the pi-electrons on the entire length of the molecule. The band gap is determined by the energy difference between HOMO and LUMO as shown in **Figure: 1.1**.

Various approaches have been suggested to explain the charge transport in polymeric materials. The transport models for these materials are derived from the observed behavior in disordered or amorphous inorganic materials.[24] These transport models can be classified as microscopic transport models which require atomic levels with first principle modeling and the macroscopic transport models where the device parameters can be directly mapped.

1.3.1 Microscopic Transport Models

Polymer-based soft materials, which are weakly bonded by van der Waals interaction are expected to have transport properties intermediate to hopping based amorphous glasses and covalently bonded crystalline systems.[25-28] The most acceptable theory for transport in polymers is based on the hopping of charges through trap sites. Disorder in polymer chains leads to localization of the states and transport takes place via hopping between the localized states with the assistance of molecular distortion which may be inherent to the system or can have an external origin.

Polarons which originate due to the inherent self-localized excitations involved in the charge transport are called the Holstein polarons and the polarons which originate due to extrinsic factors like the existence of a polarization cloud are called the Froehlich polarons.[24, 29, 30] These polarons can be positively or negatively charged with a ½ spin state. The existence of strong electron-phonon coupling in the polymer semiconductors is responsible for the existence of polarons. The strength of the electron-phonon coupling decides the radius of the polaron. Due to polarons in the semiconducting layer, additional levels are created symmetrical to the Fermi level. Typical energy levels and types of polarons are shown in **Figure: 1.2**. The location of the energy levels is dependent on the length of the polymer chain. The transition between the polaronic levels is governed by selection rules which require parity transformation. The presence of polarons is evident from experiments involving electron spin resonance and transient absorption.[31]

The hopping mechanism of a polaron from one site to another is generally thermally activated and is given by:

$$\mu = \frac{ea^2}{k_b T} \frac{\sqrt{\pi}\, J^2}{h\sqrt{2E_b k_B T}} \exp\left(\frac{-E_b}{k_B T}\right) \qquad \ldots\ldots (1.1)$$

where T is the temperature, J is the nearest-neighbor interaction energy, and E_b is the polaron binding energy.

Two types of hopping processes are observed from polymer transport namely fixed range hopping or the Miller-Abraham hopping (M-A) and variable range hopping (VRH).

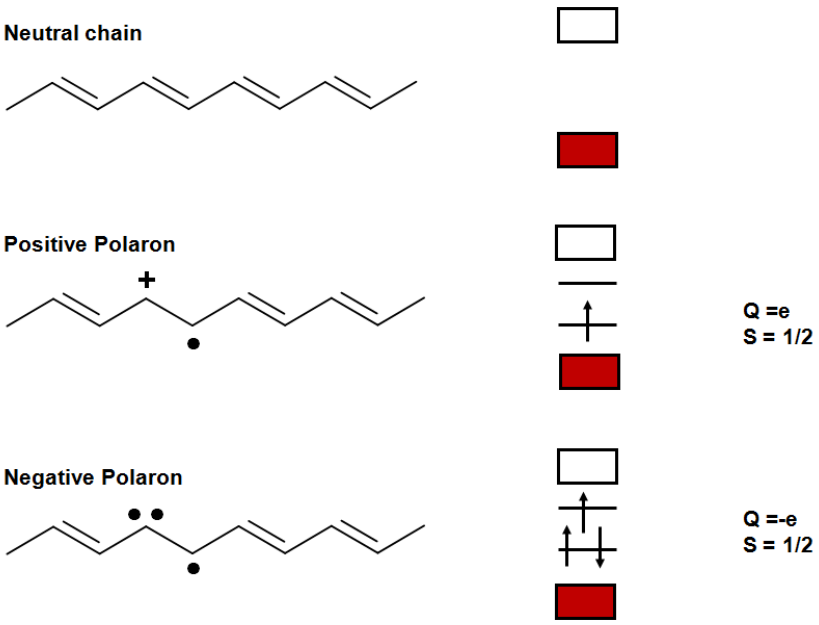

Figure 1.2: *Various types of polarons with their spin and charge state.*

(a) Miller-Abraham Hopping

In the case of fixed range hopping, proposed by Miller and Abraham for lightly doped semiconductors at a low temperature,[32] the hopping rate is given by:

$$\Gamma_{ij} = \vartheta_o \, exp\left(\frac{-2\,R_{ij}}{a}\right) exp\left(-\frac{(E_i - E_j)}{k_B T}\right) \qquad \ldots\ldots (1.2)$$

where, ϑ_o is a constant related to phonon density of states, a is the localization length and R_{ij} is the distance between sites i and j with energy E_i and E_j. The first exponential term expresses the tunneling probability indicating that at low doping levels of the semiconductors, the probability for an electron to jump from one site to another decrease exponentially as the distance between the sites is increased. The second exponential term accounts for the temperature dependence of the hopping rate. Typical transport in hopping mechanism is thermally activated with an activation energy given by the difference in energy between the hopping sites. This treatment of fixed range hopping is useful for describing transport in 1-D fibrillar structures obtained for poly(3-

hexylthiopehene) (P3HT) based systems and systems which obey 1-D transport models like Luttinger-Liquids.[33]

(b) Mott's Variable Range Hopping

If the hopping process between the nearest neighbors is not energetically favorable, charge carriers tend to hop to a larger distance than the nearest neighbor and occupy an energetically more favorable state. This process is referred to as the variable range hopping (VRH). VRH is preferred for homogeneous systems with 2-D or 3-D transport. To have conductance in these solids the spatial distance between the two states has to be optimized. From the Mott's approach,[34] the average energy spacing between states near Fermi energy level is given by:

$$W = \frac{3}{4\pi R^3 N(E_F)} \quad \ldots\ldots (1.3)$$

The average hopping distance can be estimated as

$$R_{avg} = \left[\frac{9}{8\pi\alpha N(E_F)k_B T}\right]^{\frac{1}{4}} \quad \ldots\ldots (1.4)$$

And the conductivity is obtained as

$$\sigma = \sigma_0(T)\exp\left[\left(\frac{T_o}{T}\right)^{\frac{1}{4}}\right] \quad \ldots\ldots (1.5)$$

This expression is the Mott's law for hopping transport in a 3D system. T_o is related to the broadening of density of states (DOS), α is the inverse delocalization radius and $N(E_F)$ is the density of localized states at the Fermi level E_F.

In general, the conductivity of any *d*-dimensional system can be expressed as:

$$\sigma = \sigma_0(T) \exp\left[\left(\frac{T_o}{T}\right)^{\frac{1}{d+1}}\right] \quad \ldots\ldots (1.6)$$

It should be noted that Mott's VRH model is based on several simplified assumptions that the DOS is independent of energy at E_F and no correlation exists between the tunneling process and electron-electron interactions. When the Coulomb interaction between the electrons is strong, a linear gap opens up in the DOS at E_F. In the regime of strong Columbic interaction, the conductivity is given as

$$\sigma = \sigma_0(T) \exp\left[\left(\frac{T_o}{T}\right)^{\frac{1}{2}}\right] \quad \ldots\ldots (1.7)$$

and the broadening of the Gaussian DOS is expressed as:

$$\mathrm{T_o} = 6.2\ \frac{\mathrm{e^2}}{\mathrm{k_B}\varepsilon\xi} \quad \ldots\ldots (1.8)$$

Where ε and ξ are the dielectric constant and the localization length respectively. It has been reported that when VRH is assisted by electron-electron interaction, a universal conductivity factor $\sigma_0 \approx e^2/h$ is obtained which is independent of temperature.[35, 36]

(c) Marcus theory

With the development of new materials and novel device structures, it is possible to achieve transport regimes with high charge density for polymer devices. The M-A approach for hopping fails in the regime of high charge density. In these cases, the activation energy originates from the dynamic disorder due to the local polarization fluctuations which are similar to the observed charge transfer phenomenon.[23, 37] Hence, a treatment based on Marcus electron transfer theory is utilized for understanding the

hopping processes in these systems. The Marcus expression for semi-classical electron transfer rates is given by:

$$k_{it} = \frac{t^2}{\hbar}\left[\frac{\pi}{k_B T}\right]^{\frac{1}{2}} exp\left[\frac{(\lambda_{reorg} + \varepsilon_i - \varepsilon_j)^2}{4\lambda_{reorg} k_B T}\right] \quad . \quad \ldots. (1.9)$$

where, k_{it} is the charge transfer rate, ε_i and ε_j are the respective energies of the hopping levels, and λ_{reorg} is the reorganization energy. The polarization contribution is included in the transition rate between the initial and final state and the re-organization energy. Both the Marcus theory and M-A predicts zero conductivity approach 0 as T→ 0 K which is contrary to many experimental observations where a finite conductivity is extracted upon extrapolating the $\sigma(T)$ data to 0 K. To explain this finite conductivity, the vibrational degrees of freedom are invoked which can drive the tunneling of charge carriers. In such polymeric systems, two regimes of transport exist depending on the carrier potential energy (V_{hop}). In the regime where $eV_{hop} << k_BT$, the transport is T dependent and in the regime where $eV_{hop} >> k_BT$, the transport is superlinear with electric field and is T independent. Such a transition in the transport phenomenon is observed in electrolyte gated devices or ferroelectric FETs, where charge density of 10^{13} cm^{-2} can be attained.

1.3.2 Macroscopic Transport Models

(a) Trap models

Trapping models were initially developed to understand charge transport in amorphous silicon.[38] The charge transport process involves a multiple trapping and de-trapping mechanism through localized defect states as illustrated in **Figure: 1.3.**[39] This type of transport process is referred to as the multiple trap release (MTR) transport. The

motion of charge carriers through the localized states is attributed to the available thermal energy and is governed by an Arrhenius type dependence given by the expression:

$$\mu = \mu_0 \exp\left(\frac{-E_A}{k_B T}\right) \quad \ldots\ldots (1.10)$$

where μ_0 is the mobility at 0 K, and E_A is the activation energy for the charge transport.

As evident from the above expression, at high T the transport is thermally activated and as the T decreases the transport becomes independent of T, which is referred to as the apparent band-like transport in organic systems. Such a phenomenon is generally observed in electrolyte based FETs where at low T, μ_{FET} and σ become weakly dependent on T.[40, 41]

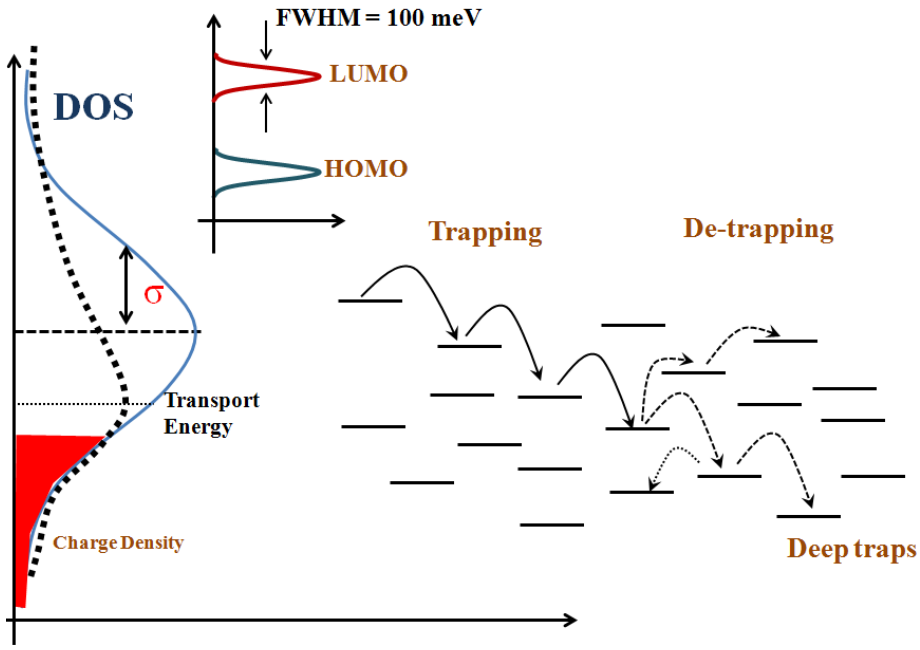

Figure 1.3: *Schematic of charge transport in the framework of Multiple Trap Release model for transport.*

Although the MTR model predicts observation of apparent band-like delocalized transport, the order-disorder transition predicted from this model is not a continuous transition. Hence, a new model for charge transport involving a continuous transition is developed called the mobility edge (ME) model. According to this model, conduction occurs when the charges are excited to the extended transport level referred to as E_t. The DOS is assumed to have an exponential distribution of localized states, and the transport occurs within E_A which is given by the difference in energy between the apparent Fermi level of the system (E_F) and the transport level. In the framework of the ME model, E_A decreases with the increase in V_g. This can be explained by the fact that as V_g increases, the number of induced charges increase and E_F shifts close to E_t which results in lower magnitude of E_A for charge transport. Based on this mechanism a transition from localized trap-limited transport to delocalized extended transport is expected in molecular solids with a very low degree of disorder.

$$\mu = \mu_0 \exp\left[\frac{-(E_t - E_F)}{k_B T}\right] \qquad \ldots\ldots (1.11)$$

This model is extensively used for understanding the temperature dependent charge transport in amorphous silicon-based devices and new generation of high mobility polymer semiconductors.

1.4 Field-Effect Transistors

Field-effect transistors (FET) form the fundamental building blocks of modern microelectronics. Schematic of a Metal insulator-semiconductor FET (MISFET) is shown in **Figure: 1.4a** along with its operating regions in **Figure: 1.4b**.

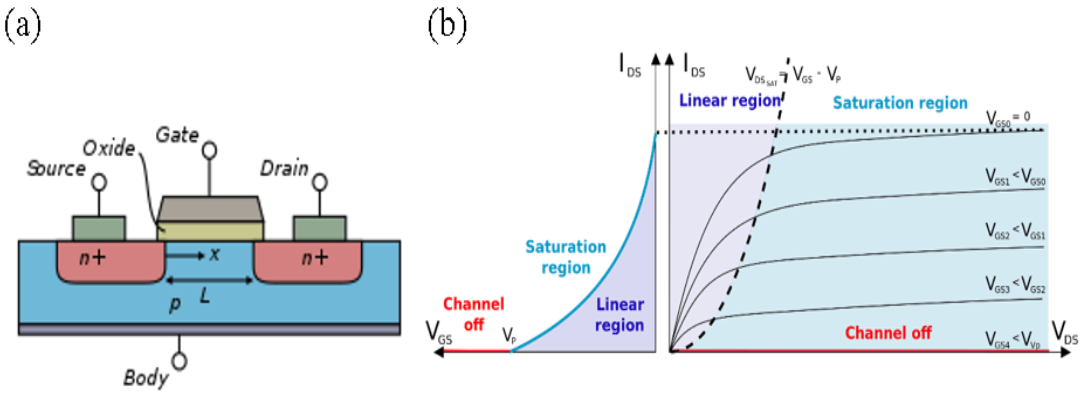

Figure 1.4: *(a) Schematic of an n-type MISFET (b) operating regions of MISFET. (reproduced from Reference [51]).*

A FET is a three terminal device consisting of a source, drain and gate electrode along with a semiconducting layer and a thin layer of dielectric material. The source and drain electrodes form an ohmic contact with the semiconductor. Charge transport occurs through a thin layer at the dielectric-semiconductor interface. The source and drain contact form two extreme ends of the FET channel. In the ideal case, there is no conductance in the channel, and this corresponds to the OFF state of the FET. An electric field between gate and source electrode induces charges in the channel by capacitive coupling (field effect) and hence modifies the conductance at the interface. Once the applied gate voltage (V_{gs}) crosses a threshold value (V_t), a continuous channel is formed between the source and drain electrodes which drives the transistor to ON state. Charges injected from source electrode are then driven through the low resistance channel and collected at the drain electrode. The conductance of the channel can be modified by varying the gate voltage. The operation of an FET can be explained with a metal-insulator-semiconductor (MIS) device energy band diagram as shown in **Figure: 1.5** using a p-type semiconductor.

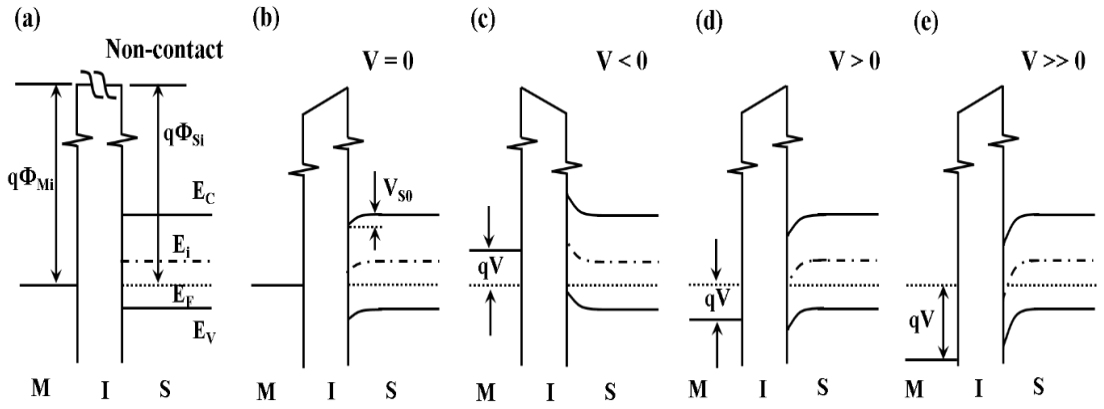

Figure 1.5: *Schematic representation of energy level arrangement in an MIS device under various bias conditions (a) physically separated metal-insulator-semiconductor (b) thermal equilibrium (c) accumulation (d) depletion and (e) inversion.*

An ideal MIS device without any bias has the same work functions for metal (Φ_{Mi}) and semiconductor (Φ_{Si}) w.r.t the insulator conduction band edge. It results in surface band bending (V_{S0}) in semiconductors (**Figure: 1.5b**), the extent of which is longer than that in the metal due to the short screening length of the latter's high electron density. An applied negative voltage ($V < 0$) to the metal electrode reduces its electrostatic potential by supplying excess electrons, also introducing a net equivalent positive charge at the semiconductor-insulator interface. The accumulation leads to excess majority charge carriers at the semiconductor-insulator interface driving the device to accumulation mode **Figure: 1.5c**. The external electric field causes tilting of the insulator energy levels, and the excess holes result in the upward bending of the semiconductor energy levels at the semiconductor-insulator interface. Applying a positive charge ($V > 0$) to the metal increases the potential and changes the Fermi level by qV, where q is the unit of electronic charge. Electrostatically induced excess negative charges at the semiconductor-insulator interface leads to a depletion of holes in the p-

type semiconductor material as shown in **Figure: 1.5d**. A very high positive charge to the metal ($V >> 0$) will result in strong downward bending of the semiconductor energy levels resulting in an inversion mode where a high density of minority carriers forms the semiconductor-metal interface as shown in the **Figure: 1.5e.**

1.5 Polymer Field-Effect Transistors (PFET)

Unlike silicon transistors, which are carved into the surface of single-crystal silicon wafers, organic FETs are fabricated by a "bottom-up" approach where multiple layers are deposited sequentially. OFETs can be fabricated on practically any substrate by depositing the various functional materials, including the semiconductor, in the form of thin, usually amorphous or polycrystalline films. The first successful demonstration of a PFET dates back to 1987. T. Ando and coworkers demonstrated first PFETs using polythiophene as the active layer with a relatively low field-effect mobility (μ_{FET}) of $2x10^{-5}$ $cm^2/(Vs)$.[42] The performance of the PFETs was improved in successive years to reach mobility values up to 10 $cm^2/(Vs)$ and thus achieving parity with amorphous silicon.[43] This impressive performance allowed PFETs to penetrate the consumer electronics space. Also, these materials have allowed fundamental studies of, for example, the degree of wave function delocalization achievable in van der Waals bonded materials,[44] the coupling between charge transport and structural dynamics,[28, 45] studies of transport at two-dimensional charge transfer interfaces,[46] or the role of nuclear tunneling in electron transfer.[37] The improved understanding of charge transport and structure-property relationships has further helped chemists to prepare high performing semiconducting polymer materials for PFETs and solar cells.

1.6 Device Geometry

A PFET is composed of three basic elements: (i) a thin polymer semiconductor film; (ii) an insulating layer; and (iii) three electrodes. Two electrodes, the source, and the drain, are in contact with the semiconductor film at a short distance from one another and the distance between them define the geometrical channel length (L). The third electrode, the gate, is separated from the semiconductor film by the insulating layer. Adversatively to the MOSFET, the source, and drain electrodes are metals, and the organic semiconductor is typically undoped. Commonly employed PFET device architectures are shown in **Figure: 1.6**.

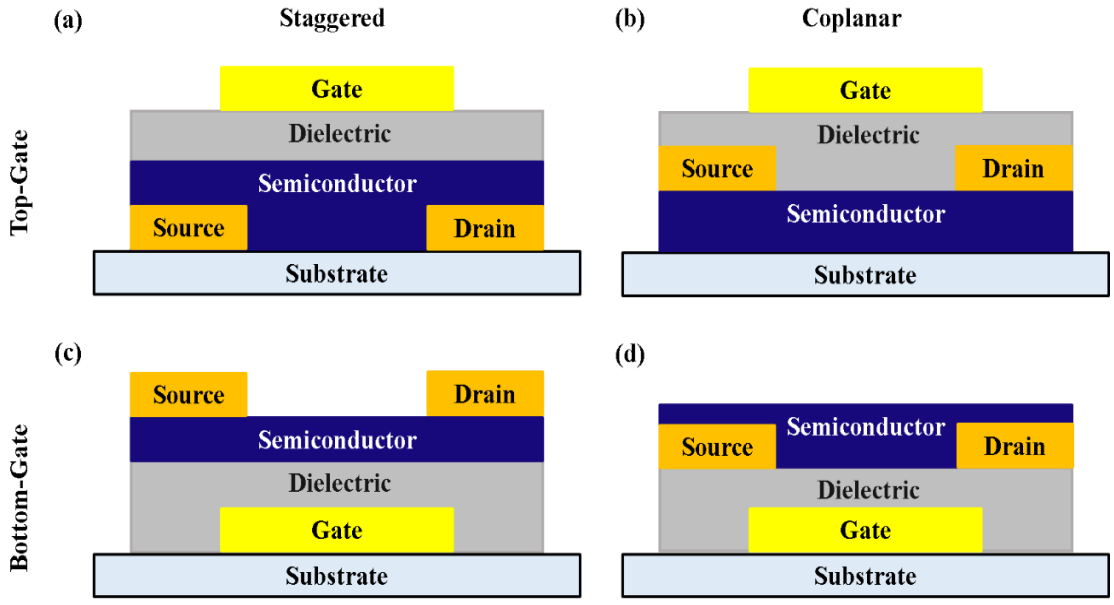

Figure 1.6: *Schematic of different PFET geometries (a) bottom contact-top gate (BC-TG) (b) top contact-top gate (TC-TG), rarely used (c) top contact- bottom gate (TC-BG) and (d) bottom contact- bottom gate (BC-BG).*

In coplanar structures, the drain-source electrodes and the dielectric are located at the same side of the channel, whereas in staggered structures the drain-source

electrodes and the dielectric are placed at opposite sides. These geometries differ in the way the layers are processed and are material dependent. For example, many dielectrics require a post-deposition annealing above 100^0C, which limit the use of top contact-top gate structure (TC-TG) and bottom contact-top gate (BC-TG) structures with a semiconductor having degradation temperature below 100^0C. Moreover, different transistor geometries vary in the quality of the metal-semiconductor and semiconductor-insulator interfaces w.r.to interface morphology and trap states. The charge transport in a PFET is confined to a thin layer (nm) of semiconductor next to the interface to the gate dielectric, and any chemical or structural defects would adversely affect the overall performance of the device. For example, a solution processed bilayer interface could have an intermixed semiconductor-dielectric layer, whereas a thermally evaporated dielectric on semiconductor (or vice versa) could give a much smoother interface. Bottom-contact PFETs may prove to be easy to manufacture at large scale, but their high contact resistance because of the lack of wetting of metal by the semiconductor requires additional chemical treatment on the metal to have a lower charge injection barrier. The position of charge injection at the semiconductor-metal electrode interface also changes with the geometry. In the (BC-BG) geometry, charges are injected directly from the source electrode to the interface, while in the (TC-BG) and (BC-TG) geometries, the charges are injected into the bulk of the undoped semiconductor and need to first travel through several tens of nanometers of semiconductor before they reach the semiconductor-insulator interfaces. Two of the most used geometries are top contact- bottom gate (TC-BG) and bottom contact-top gate (BC-TG). In this thesis, the PFETs are fabricated in (TC-BG) configuration for the ease of preparation in the laboratory.

1.7 Operation of PFETs

Polymer and inorganic FETs differ in their mode of operation and the charge carriers responsible for transport. The PFETs work in accumulation mode and the observation of inversion regime is rarely seen, which can be related to the large time constant involved in the transport of minority carriers in polymer semiconductors. PFETs can be of p-type, n-type or ambipolar depending upon the mobility of charge carriers present in the semiconducting material and judicious choice of gate dielectric and electrodes that can bring out optimal performance from the device.[47-50]

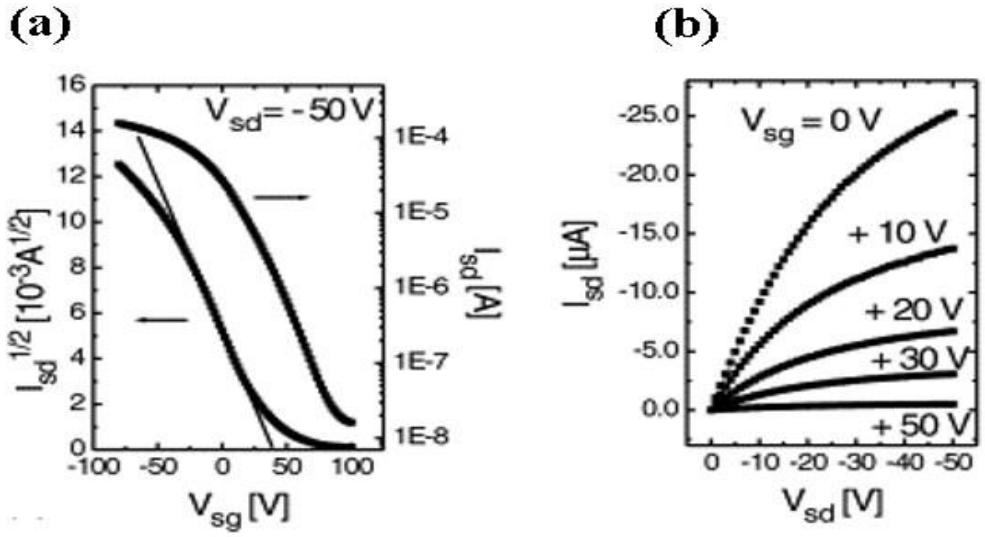

Figure 1.7: *Current-voltage characteristics of a typical rr-P3HT PFET. (a) transfer characteristics and (b) output characteristics. (reproduced from Reference [52]).*

Typical current-voltage characteristics of a p-type PFET with a regioregular-P3HT (rr-P3HT) semiconducting layer and gold electrodes are shown in **Figure: 1.7**. P3HT is a semiconducting polymer which forms microcrystalline regions with characteristic edge-on orientation on the dielectric surface to facilitate a high π-π electron coupling along the direction of charge transport in FET geometry.

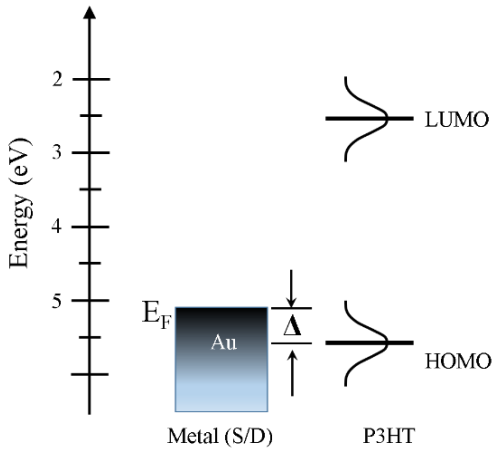

Figure 1.8: *Schematic of Fermi energy level of gold electrode and HOMO/LUMO levels of P3HT.*

The operation of a PFET can be described using the energy level arrangement at the metal-semiconductor junction as shown in **Figure: 1.8**. The Fermi level of gold (Au) and HOMO/LUMO levels of P3HT are shown in the diagram. A voltage is applied to the gate (V_{gs}) to control the amount of current flow between the source and drain (I_{ds}) electrodes. When a positive voltage is applied to the gate, negative charges are induced at the source electrode. As can be seen in **Figure: 1.8**, the Fermi level of gold is far away from the LUMO level, so that electron injection is highly unlikely. Accordingly, no current passes through the P3HT layer, and the small measured current essentially comes from leakage current through the insulating layer. This corresponds to the OFF state of the PFET as seen in **Figure: 1.9a**. When V_{gs} = 0 no charges are introduced in the channel region, hence there will be no band bending in the semiconductor. This is referred to as flat-band condition.[51] When the gate voltage is reversed (V_{gs} < 0), band bending occurs in the semiconductor at the interface which increases the charge density of majority carriers (holes) at the dielectric-semiconductor interface driving the PFET to accumulation mode with a uniform charge density throughout the channel. If the V_{ds}

is zero and both electrodes are identical, the number of charges injected into an ideal, that is, trap-free, polymer semiconductor is proportional to the capacitance per unit area of the dielectric, C_i, and to the gate voltage V_{gs}. Near vicinity of Fermi level of gold to the HOMO level of P3HT can then facilitate the injection of holes to the semiconductor-dielectric interface forming a conducting channel which can drive charges from source to drain by applying a second voltage to the drain (V_{ds}). At low negative V_{ds}, the current increases linearly with the drain voltage (**Figure: 1.9b**), following Ohm's law. It constitutes the linear regime of PFET operation. When the V_{ds} is comparable to the V_{gs}, the voltage drop at drain contact falls to zero, and the conducting channel is pinched off leading the PFET to saturation regime where the current I_{ds} becomes independent of the drain voltage as shown in **Figure: 1.9c**.

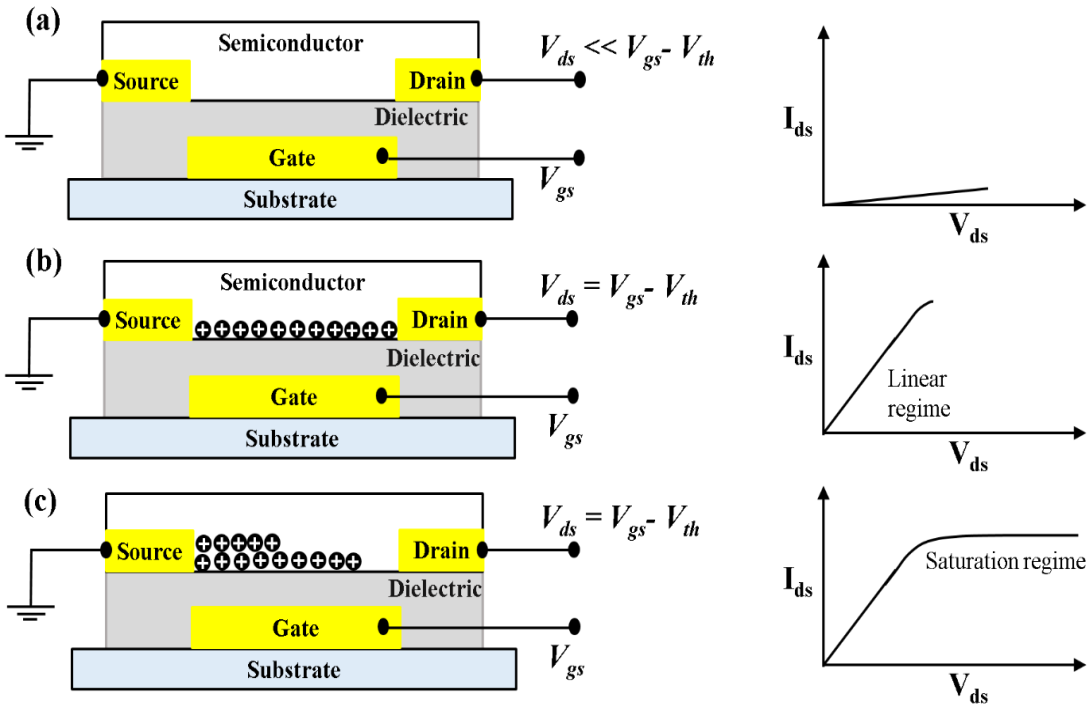

Figure 1.9: *Operation regimes in a PFET under different biasing conditions (a) OFF state (b) linear regime (c) saturation regime.*

Current-voltage characteristics of a PFET can be arrived at by making following assumptions which are similar to the one used for TFTs (i) the transverse electric field perpendicular to the channel is very low compared to electric field along the channel, this demands a very thin dielectric with a thickness $d_d < L/10$ (gradual channel approximation), (ii) no barrier between the energy levels of the semiconductor and Fermi level of the source electrode, (iii) homogenous carrier mobility throughout the channel and (iv) negligible gate leakage current (I_g).[27]

If the V_{ds} is zero and both electrodes are identical, the number of charges injected into an ideal, that is, trap-free, polymer semiconductor is proportional to the capacitance per unit area of the dielectric, C_i, and to the gate voltage V_{gs}. But in practice, any polymer semiconductor contains traps of various degree for charge carriers, so that the first charges injected are used to fill up the traps. This mandates an additional gate voltage called threshold voltage (V_{th}), to establish accumulation layer of mobile charges at the dielectric-semiconductor interface that can make mobile charges in the channel. The total induced charges per unit area (Q_{mob}) in the channel can be expressed as,

$$Q_{mob} = C_i(V_{gs} - V_{th}) \quad \text{….. (1.12)}$$

An applied drain voltage V_{ds} can drive these mobile charges creating a potential gradient along the channel. The potential inside the channel $V(x)$ at any position x varies linearly from source (x = 0) to drain (x = L) leading to the modification of Q_{mob} as shown below,

$$Q_{mob} = C_i(V_{gs} - V_{th} - V(x)) \quad \text{….. (1.13)}$$

Neglecting diffusion, the drain-source current can be written as,

$$I_{ds} = WQ_{mob}\mu_{FET}E(x) \quad \text{..... (1.14)}$$

where W is the width of the channel and $E(x) = dV/dx$ is the electric field at position x in the channel. Substituting for I_{ds} and Q_{mob} modifies the Equation: 1.14:

$$I_{ds}dx = WC_i(V_{gs} - V_{th} - V(x))\mu dV \quad \text{..... (1.15)}$$

The total drain-source current can be calculated by integrating $I_{ds}dx$ over the entire channel length, i.e., from x = 0 to x = L.

$$I_{ds} = \frac{W}{L}\mu_{FET}C_i\left[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2\right] \quad \text{..... (1.16)}$$

Equation 1.16 gives the I_{ds} under gradual channel approximation.

In the linear regime of transistor operation, $V_{ds} << V_{gs}$ and $(1/2)V_{ds}^2$ term can be neglected. The equation can be simplified to

$$I_{ds,lin} = \frac{W}{L}\mu_{FET}^{lin}C_i\left[(V_{gs} - V_{th})V_{ds}\right] \quad \text{..... (1.17)}$$

The above equation states the linear relation between I_{ds} and gate voltage, and field effect mobility in the linear regime can be extracted using the following expression.

$$\mu_{FET}^{lin} = \frac{\partial I_{ds,lin}}{\partial V_{gs}}\frac{L}{WC_iV_{ds}} \quad \text{..... (1.18)}$$

In the pinch off condition of TFT, $V_{ds} = V_{gs} - V_{th}$ and a further increase in the gate voltage has minimal effect on saturation current $I_{ds,sat}$. Hence Equation 1.16 can be modified as:

$$I_{ds,sat} = \frac{W}{2L}\mu_{FET}^{sat}C_i\left(V_{gs} - V_{th}\right)^2 \quad \text{..... (1.19)}$$

And μ_{FET}^{sat} can be deduced as,

$$\mu_{FET}^{sat} = \frac{\partial I_{ds}}{\partial V_{gs}} \frac{L}{WC_i(V_{gs}-V_{th})} \quad \ldots\ldots (1.20)$$

The above equation states that the saturation current and mobility in TFT are independent of V_{ds}. The presence of an external potential V_{ext} can modify the capacitance of the interface, and the earlier equations have to be rewritten to accommodate the additional charge buildup at the interface. External potential can arise from, for example, a remnant polarization present in the dielectric layer of PFET. The modified equation for I_{ds} including the correction factor can be expressed as:

$$I_{ds,sat} = \frac{W}{2L}\mu_{FET}^{sat}C_i\left(V_{gs} - V_{th} - V_{ext}\right)^2 \quad \ldots\ldots (1.21)$$

Other important parameters used to characterize the PFETs are on-off ratio, and switching frequency, both of which linearly depend on the μ_{FET}. On-off ratio is the measure of signal to noise ratio in the transistor. It is calculated as the ratio of channel current in the off state and accumulation mode.

$$On - off\ ratio = \frac{I_{ds,ON}}{I_{ds,OFF}} = \frac{\mu_{FET}}{\sigma}\frac{C_i^2}{Ned_s^2}V_{ds}^2 \quad \ldots\ldots (1.22)$$

where N is the charge density at the interface, σ is the conductivity of the channel and d_s is the thickness of the semiconductor.

Switching frequency f_0 is the maximum frequency at which an FET can operate. Operating above this frequency will result in the output signal being out of phase w.r.to the input signal and the amplitude of the output signal starts to reduce. A crude measure

of the frequency response is the reciprocal transit time, τ_r, of the charge carriers in the transistor channel.

$$\tau_r = \frac{L}{v} \quad \text{..... (1.23)}$$

where v is the velocity of charge carriers, and it can be represented in terms of μ_{FET} as:

$$v = \mu_{FET} E = \mu_{FET} \frac{V_{ds}}{L} \quad \text{..... (1.24)}$$

Hence the f_0 can be represented as:

$$f_0 = \frac{1}{2\pi\tau_r} = \frac{1}{2\pi} \frac{\mu_{FET} V_{ds}}{L^2} \quad \text{..... (1.25)}$$

Both of the above equations (1.22) and (1.25) shows the need to have a high field effect mobility for better performance in PFETs. Following sections discuss various aspects of the dielectric and semiconductor-dielectric interfaces to fabricate a high mobility PFET device.

1.8 Choice of Gate Dielectric

As evident from the previous section, it is clear that the dielectric layer plays a vital role in determining the performance parameters of PFET.[50] An ideal dielectric layer should facilitate the creation of a highly conductive channel in the transistor, while maintaining a zero gate leakage current even with small dielectric film thickness. Also, a high break-down current and low hysteresis are highly sought for the stability of the devices. Thin dielectrics, with high dielectric constant, are required for low voltage operation of PFETs. Surface roughness and traps have to be minimized to avoid the charge trapping and scattering at the semiconductor-dielectric interface.[52] Moreover,

the surface morphology determines the growth of the semiconductor on the top.[53-55] Surface energy matching of the dielectric to that of the semiconductor is required for a good wetting of semiconducting film on the top while casting from a solution.[56] Low-temperature processing close to ambient allows the materials to be used on flexible substrates and roll to roll production lines.

Currently, two types of dielectric materials are commonly used in PFET fabrication, either inorganic metal oxides or polymeric dielectrics.[57] Widely used inorganic dielectric materials are HfO_x, Ta_xO_y, Al_2O_3, SiO_2, etc. which are processed by sol-gel or atomic layer deposition (ALD).[58] While inorganic dielectrics have higher stability and dielectric constant, their polymer counterparts possess high dielectric break-down strength and easy processability. Regularly used polymer dielectrics are poly (methyl methacrylate) (PMMA), poly vinyl alcohol (PVA), polystyrene (PS) and benzocyclobutene (BCB) which are processed via simple solution-based methods. Functional polymers such as polyvinylidene fluoride trifluoroethylene (P(VDF-TrFE)) having a remnant polarization are also used in the fabrication of ferroelectric memory PFETs.[59]

1.9 Ferroelectric Dielectrics

A material is ferroelectric when it exhibits a spontaneous polarization, which can be reversed by application of an electric field. All dielectric materials in the presence of an external electric field *E* cause displacement of the bound charges inside the material, hence inducing a local electric dipole moment. The electric displacement field *D* is defined as

$$D = \varepsilon_0 E + P \qquad \ldots\ldots (1.26)$$

where ε_0 is the dielectric permittivity of free space, and P is the polarization density.

Most dielectrics are satisfactorily described as linear, homogeneous, isotropic and instantaneously responsive to the electric field. In such a case, the polarization P is proportional to the applied field E.

$$P_{lin} = \varepsilon_0 \chi E \quad \text{..... (1.27)}$$

Hence, electric displacement can be expressed as,

$$D = \varepsilon_0 E + \varepsilon_0 \chi E = \varepsilon_0 (1 + \chi) E \quad \text{..... (1.28)}$$

$$D = \varepsilon_0 \varepsilon_r E \quad \text{..... (1.29)}$$

where, ε_r is the relative dielectric permittivity of the materials and χ is the dielectric susceptibility. Hence, D versus E graph forms a straight line through the origin as shown by the dotted line in **Figure 1.10.**

A ferroelectric material exhibits a spontaneous polarization P_{ferro} in addition to P_{lin}, leading to the modification of above equation,

$$D = \varepsilon_0 E + \chi \varepsilon_0 E + P_{ferro} \quad \text{..... (1.30)}$$

Hence the D vs E curve shows a bi-stable hysteresis as shown as the continuous line in **Figure 1.10**. When the applied electric field returns to zero, a remnant polarization P_r remains which is either positive or negative depending on the history of the applied field. The field at which the polarization switches sign is called the coercive field E_c.

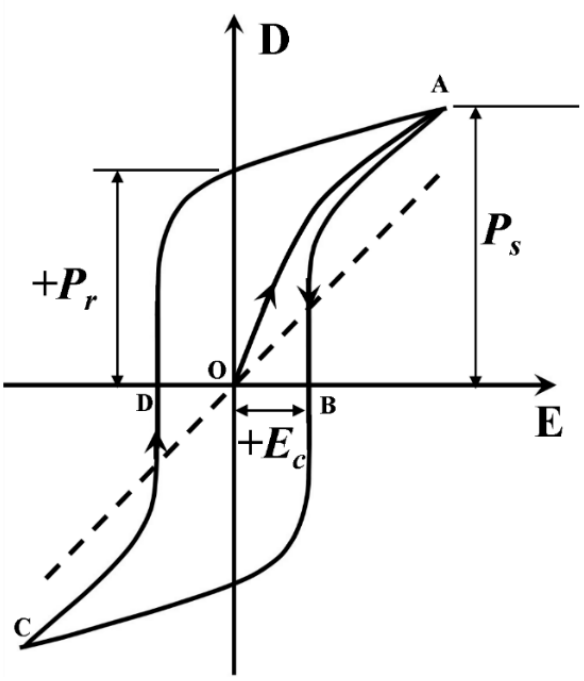

Figure 1.10: *A typical dielectric displacement (D) vs. electric field (E) curve of a dielectric. Dotted curve represents a standard dielectric, while the continuous curve represents a ferroelectric material.*

The field effect mobility, switching speed and on-off ratio are the important parameters defining the performance of an OFET. In the case of a ferroelectric dielectric, the involvement of random dipoles at the surface of the dielectric take a toll on the switching speed of the transistor.[60] So, a novel method using external electric field is introduced in Chapter 4, to align the dipoles of the dielectric during the fabrication process. Special attention should be given to the roughness of the dielectric surface, as higher roughness can reduced charge carrier mobility as a result of high transport activation energies, and larger trap distribution widths.[61] P(VDF-TrFE) offers a relatively rough surface (roughness ~ 6-8 nm) compared to that of PMMA and BCB.[62] Thus processing conditions have to be optimized to keep it under control which is the central theme of Chapter 4.

1.10 Importance of Semiconductor-Dielectric Interface

The semiconductor-dielectric interface plays the most crucial role in PFETs. It controls the electrical performance mainly by (i) determining the morphology of the polymer semiconductor, (ii) the dielectric properties of the insulator layer and (iii) the electronic states at the dielectric-semiconductor interface.

As discussed in the previous section, high dielectric surface roughness can introduce geometrical defects which localizes the charge carriers and hence a smooth interface is preferred. Charge transport in the PFET channel is highly directional and a strong $\pi - \pi$ overlap between the molecules along the transport direction will improve the performance of the devices.[63] It can be achieved by controlling the molecular orientation at the interface. Self-assembled monolayers (SAMs) are often used on oxide dielectric interfaces to control the grain growth and the molecular orientation.[64] Controlling the semiconductor film morphology, molecular conformation and orientation are the other handles used to optimize the charge carrier mobility. Conjugated molecules, in solid films, pack themselves with their long axis parallel to each other to form multilayered structures. They generally form lamella-like ordering taking any of the following molecular stacking (i) edge-on, (ii) face-on and (iii) end-on. For example, the stacking of P3HT molecules in the film is shown in **Figure: 1.11**.[65] Edge-on stacking in the polymer will have π- π stacking along the plane of the substrate making it the favorable orientation for an FET structure, while face-on stacking will have π- π stacking perpendicular to the substrate, making them the ideal molecular configuration for solar cells.[63, 66-68] To improve molecular order, aggregation and (semi-)crystallinity in polymer semiconductor films, a wide range of techniques such as thermal annealing or solvent annealing.[69] choosing solvents with high boiling points

and suitable solubility parameters to induce order during or after spin-coating, [70-72] adding nucleation agents to the solution, [56, 73] to name a few, are used.

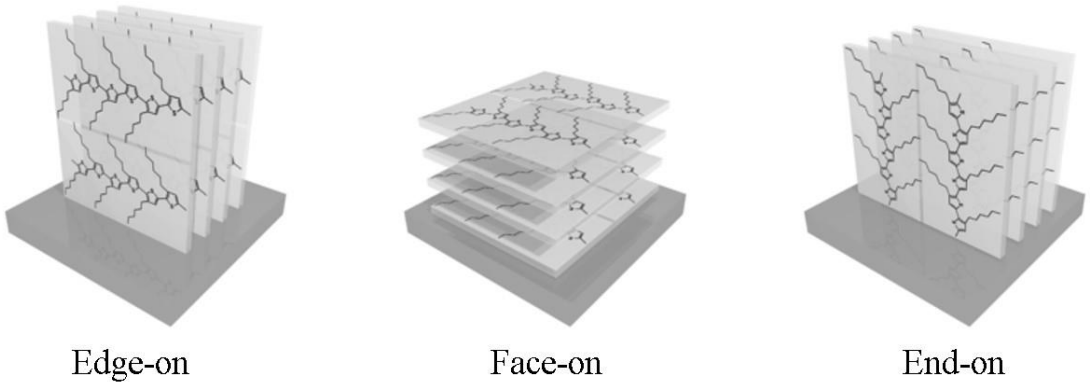

Figure 1.11: *Schematic of P3HT molecular order in thin film (reproduced from Reference[65]).*

Given the fact that charge transport occurs at a thin layer inside the semiconductor, close to the dielectric surface, it very important to consider the effect of polarity of the dielectric layer on the DOS of the semiconductor. Experimental evidence suggests that mobility follows an inverse relationship with the dielectric constant of the insulating layer.[24] It was also observed that the dipolar induced DOS broadening at the interface is related to the nature of the insulating material and not the dielectric constant alone.[60]

Electronic states at the interface play a decisive role in the nature of polarity of PFETs. Impurities or the semiconductor side groups can form interface states which act as electron/hole traps and hinder charge transport.[50] For example, R. H Friend *et al.* demonstrated that the electron traps at the interface could be passivated using a hydroxyl-free gate dielectric such as a bis(benzocyclobutene) derivative (BCB). FETs

fabricated using BCB dielectric exhibited higher n-channel performance from polymers which were previously thought to show only p-channel activity.[47]

1.11 Metal-Semiconductor Interface

A metal-semiconductor interface is one of the most studied topics in device physics as they are obvious junctions in any semiconductor device. The main purpose of the metal-semiconductor (M-S) interface is to facilitate efficient carrier injection (collection) to the (from the) semiconductor. Energy levels of the metal and semiconductor define the interfacial behavior upon contact. A proper set of materials can be used to engineer the interface to achieve either ohmic or rectifying M-S interface.

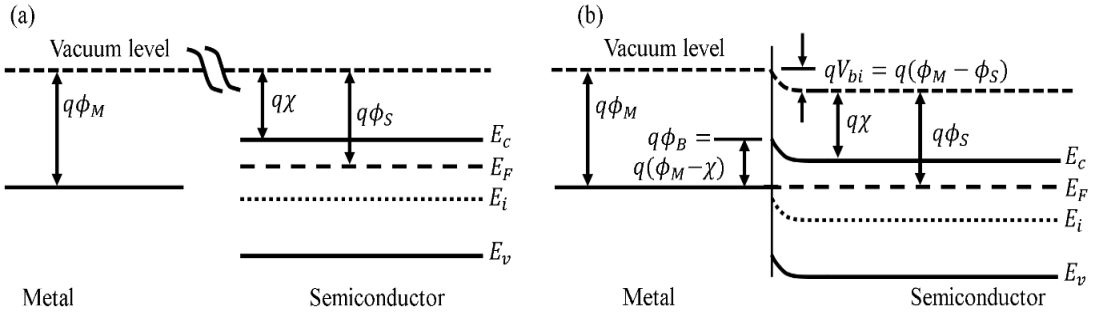

Figure 1.12: *Schematic of the metal-semiconductor junction energy band diagram (a) before and (b) after contact. E_c, E_v, E_F, E_i, ϕ_S, χ, ϕ_M are the conduction band edge, valence band edge, Fermi level and intrinsic Fermi level, work function of semiconductor, electron affinity of the semiconductor and work function of the metal respectively.*

Consider a junction formed between a metal and n-type semiconductor, as shown in **Figure: 1.12.** The Fermi level of the semiconductor is higher than that of the metal. Similar to a metal-metal junction, when the metal-semiconductor junction is formed, the Fermi levels must line up at equilibrium. Electrons in the conduction level

of the semiconductor move towards the metal, filling up the empty energy states above the Fermi level of the metal. This leaves a positive charge on the semiconductor side and due to the excess electrons, a negative charge on the metal side, leading to the band bending of energy levels at the interface. The extent of the band bending on the semiconductor side is longer than that in the metal due to the short screening length of the latter's high electron density. The total system maintains charge neutrality, even though each side is partially polarized due to the initial movement of the charges across the surface. Unlike the work function (ϕ_S), the electron affinity (χ) of the semiconductor does not depend on the applied field. This results in a fixed barrier ϕ_B for the electrons coming from metal side to the semiconductor, and a variable potential barrier V_{bi} for the electron coming from the semiconductor to the metal side. This barrier imposes restriction on the injection and collection of electron across the interface while allowing free flow of holes. However, an external potential can be applied to the interface to raise the Fermi level of the semiconductor effectively eliminating the barrier, and is called positive biasing of the junction. While a reverse bias will lower the Fermi level of the semiconductor, which increases the barrier and reduces the current flow across the interface. This energetics at the interface ensure that the current flows only when high enough forward bias is applied and hence constitutes a schottky barrier.

1.12 Hybrid Organic-Inorganic Perovskite

Hybrid organic-inorganic perovskite (HOIP) materials belongs to a class of crystal with chemical formula ABX_3. In HOIP, the A cation is organic (methylammonium = $CH_3NH_3^+$ or formamidinium = $HC(NH_2)^{2+}$) and the B cation is a divalent metal (Pb^{2+}, Sn^{2+} or Cu^{2+}), and the X site is occupied by one of the halides (I^-, Br^-, or Cl^-).[74] HOIP takes cubic structure at room temperature with cations A and B

are coordinated by 12 and 6 anions X, respectively and tetragonal and orthorhombic structures at lower temperatures.[75] The structural equilibrium is maintained by ionic and hydrogen bonding, which make them soft materials compared to inorganic perovskite materials.[76]

HOIP materials have been under researcher's radars since 1990s, but studies were focused on their electronic properties.[77] Early reports from David B. Mitzi examined the characteristic of the hybrid organic-inorganic framework using (n-fluorophenethylammonium)$_2$SnI$_4$ (n = 4, 3,2).[9, 78] The interface characteristics studied using these materials showed potential for applications in thin film transistors (TFT) and light-emitting diodes (LED). HOIP remained mostly unnoticed by the photovoltaic community until the achievement of 3.8% power conversion efficiency from MAPbI$_3$ absorber and liquid-electrolyte based dye-sensitized solar cell by T. Miyasaka and team in 2009.[79] A focused approach was followed towards the research and development of various HOIP systems.[80] The understanding of charge transport from research community resulted in a rapid growth in performance of HOIP devices.[81, 82] Long carrier diffusion lengths and lifetimes, high absorption coefficient, low monomolecular recombination rates and ease of processablity make HOIP promising materials for optoelectronic applications.[83-86]

1.13 Transport in hybrid semiconductors

Hybrid materials can be examined with models used for polycrystalline direct-gap semiconductors. HOIPs have shown to exhibit large carrier lifetime, significant diffusion length and sizable mobility.[83, 84] The absorption coefficient ($\alpha(E)$) of HOIP materials is comparable to that of organic semiconductors (~10^5 cm^{-1}), requiring thin

layers (~300 nm) for efficiently harvesting major portion of the incident solar radiation.[85, 87, 88] These materials have largely been probed using planar (sandwich) configurations, i.e., with electrodes and buffer layers to facilitate charge injection. There have been only a few studies on examining the transport in detail using lateral geometries.[89, 90] The low interfacial contact area with associated barriers, low carrier density, and larger interelectrode distances are issues associated with this geometry. Nevertheless, higher diffusion length and possibility of ordered crystalline growth on the substrate make HOIP to be used in lateral geometry.[91-93]

Crystalline periodicity and lower trap density allow the use of drift-diffusion formalism for HOIPs.[94] The electron and hole current densities can be represented as:

$$J_n = q\mu_n nE + qD_n \nabla n \quad \ldots\ldots (1.31)$$

$$J_p = q\mu_p pE - qD_p \nabla n \quad \ldots\ldots (1.32)$$

where q is the electronic charge, E is the applied electric field, n and p are electron and hole concentrations, $\mu_{n(p)}$ is the electron (hole) motilities which satisfy $\mu_{n(p)} = {}^{v_d}/_{E}$ for the drift velocity v_d and, $D_{n(p)}$ is the electron (hole) diffusion constants, which satisfy the Einstein relation $D_{n(p)} = {}^{\mu_{n(p)} k_B T}/_{q}$. The continuity equation for two carriers can be written as:

$$q\frac{\partial n}{\partial t} = \nabla . J_n + q(G - R) \quad \ldots\ldots (1.33)$$

$$q\frac{\partial p}{\partial t} = \nabla . J_p + q(G - R) \quad \ldots\ldots (1.34)$$

where G is the generation rate and R is the recombination rate in the material.

Electric field from the carrier concentration can be written using Poisson's equation

$$\varepsilon_r \nabla . E = q(p - n + N_d) \quad \ldots\ldots (1.35)$$

where ε is the (homogeneous) permittivity of the medium and N_d is concentration of any dopants, impurities or trapped carriers, weighted by their relative charges.

These semiconductor equations (equations (1.33), (1.34) and (1.35)) constitute a coupled nonlinear set. It is not possible, in general, to obtain a solution directly in one step, rather a nonlinear iteration method is required, and it depends on a number of details related to the particular device under study.[94] A special case of the laterally displaced parallel electrode on a hybrid semiconductor is described in Chapter 5. There are in general three possible choices of variables used in the above equations for the semiconductors,

1.13.1 Natural variable formulation (ϕ, n, p)

Using equations (1.33), (1.34) and (1.35) and $E = -\nabla\phi$, where ϕ is the electrostatic potential, the transport equations can be expressed as,

$$\frac{\partial n}{\partial t} = \nabla . (D_n \nabla n + \mu_n n \nabla \phi) + (G - R) \quad \ldots\ldots (1.36)$$

$$\frac{\partial p}{\partial t} = \nabla . (D_p \nabla p - \mu_p p \nabla \phi) + (G - R) \quad \ldots\ldots (1.37)$$

$$\nabla . (\varepsilon_r \nabla \phi) = q(p - n + N_d) \quad \ldots\ldots (1.38)$$

And the steady state drift-diffusion for both the carriers can be expressed as:

$$-\nabla.\begin{pmatrix} D_n\nabla n + \mu_n n\nabla\phi \\ D_p\nabla p - \mu_p p\nabla\phi \\ -\varepsilon_r\nabla\phi \end{pmatrix} = \begin{pmatrix} G-R \\ G-R \\ p-n+N_d \end{pmatrix} \quad \ldots\ldots (1.39)$$

1.13.2 Quasi-Fermi level formulation (ϕ , ϕ_p, ϕ_n)

Under a non-equilibrium condition in the semiconductor, for example non-uniform photogeneration, a quasi-Fermi level is established where each type of carrier population (*n*/*p*) reach thermal equilibrium with themselves, while electrons and holes don't reach thermal equilibrium with each other and have separate Fermi level of their own. Under a continuous excitation, this steady state is retained. If the system is non-degenerate, we can use following equations to express the carrier concentration in terms of individual quasi-Fermi levels of electrons and holes,

$$n = N_c \exp\left(\frac{E_c - q\phi_n}{k_B T}\right),\ N_c = 2\left(\frac{m_c k_B T}{2\pi\hbar^2}\right)^{\left(\frac{3}{2}\right)} \quad \ldots\ldots (1.40)$$

$$p = N_p \exp\left(\frac{q\phi_p - E_v}{k_B T}\right),\ N_v = 2\left(\frac{m_c k_B T}{2\pi\hbar^2}\right)^{\left(\frac{3}{2}\right)} \quad \ldots\ldots (1.41)$$

where $m_{c(v)}$ is the effective mass of the carrier in its respective band. Under equilibrium condition $\phi_n = \phi_p$, hence, the product is

$$np = n_i^2 = N_c N_v exp\left(\frac{-E_g}{k_B T}\right) \quad \ldots\ldots (1.42)$$

which is the intrinsic carrier concentration. In the limit of no doping, in thermal equilibrium, charge neutrality requires $n = p = n_i$. If the charge carriers are not in thermal equilibrium but are nondegenerate to employ Boltzmann statistics for both carrier types, then we have

$$n = n_i \exp\left(q\ \frac{\phi - \phi_n}{k_B T}\right) \quad \ldots\ldots (1.43)$$

$$p = n_i \exp\left(q\ \frac{\phi_p - \phi}{k_B T}\right) \quad \ldots\ldots (1.44)$$

provided we set the absolute level of $\phi = 0$ when the system is in equilibrium with no net charge. This is required for the Fermi level to be in the middle of the bandgap so the system has no net charge. If the system is doped, an offset is required. This relation enables the quasi-Fermi level formulation of the drift-diffusion equations. The convenience of this formulation is that, if we make the assumption that the Einstein relationship is valid, then using equations (1.31), (1.32), (1.43) and (1.44) we can write,

$$J_n = q(-\mu_n n \nabla\phi + \frac{D_n q}{k_B T} n(\nabla\phi - \nabla\phi_n) = -q\mu_n n \nabla\phi_n = \sigma_n E \quad \ldots\ldots (1.45)$$

$$J_p = q(-\mu_p n \nabla\phi - \frac{D_p q}{k_B T} p(\nabla\phi_p - \nabla\phi) = -q\mu_p n \nabla\phi_p = \sigma_p E \quad \ldots\ldots (1.46)$$

where $\sigma_{n(p)} = q\mu_{n(p)} n(p)$ is the electron(hole) conductivity in the material.

1.13.3 Slotboom formulation (Φ , ϕ_p, ϕ_n)

Slotboom variables are the reformulated version of carrier density with a thermal voltage scaling factor *i.e,*

$$n = \rho_n \exp\left(-\frac{q\phi_n}{k_B T}\right) = \rho_n \exp\left(-\frac{\phi_n}{V_T}\right) \quad \ldots\ldots (1.47)$$

$$p = \rho_p \exp\left(\frac{q\phi_p}{k_B T}\right) = \rho_p \exp\left(-\frac{\phi_p}{V_T}\right) \quad \ldots\ldots (1.48)$$

where $V_T = \frac{k_B T}{q}$ is the thermal energy.

Hence equations (1.33) and (1.34) can be written as,

$$J_n = -qD_n e^{\phi} \nabla \rho_n \quad \ldots\ldots (1.49)$$

$$J_p = -qD_p e^{\phi} \nabla \rho_p \quad \ldots\ldots (1.50)$$

This drift-diffusion current density in a semiconductor is a purely diffusive flux of new kind of carrier with a properly modified diffusion constant.

This formalism of drift-diffusion models play a very important role in the analysis of HOIP lateral transport results.

1.14 Objectives and Outline

This thesis is focused on certain aspects of lateral charge transport in device geometries which are relevant to solution-processed organic field effect transistors and lateral solar cells. Well established materials were chosen for the fabrication of devices. This thesis is divided into six chapters.

It is essential to understand the properties and the bottlenecks governing the performance of devices studied so far. Thus, an overview of the fundamental principles of the charge transport in organic semiconductors and hybrid organic-inorganic perovskite systems are described in Chapter 1.

A key parameter to consider during the fabrication of the device is the right choice of materials and their processing conditions. Solution processability, mutual compatibility and high charge mobility are the parameters considered for the choice of the embedded material in the device. A detailed description of the chemical structure and optoelectronic properties of the materials are discussed in Chapter 2. It also discusses various characterization setups used in this thesis.

A ferroelectric polymer dielectric based OFET is demonstrated using (semi-)crystalline polymers in Chapter 3. One of the fundamental limiting factors which restrict the fast charge transport and switching speed in OFET comes from the highly disordered dipolar interface at the semiconductor-dielectric interface. It is particularly important in the case of ferroelectric dielectrics as they have high dipolar moments. This issue is addressed in the next chapter.

Chapter 4 discusses an external electric field induced surface modification procedure utilized to enhance organic field effect transistor (OFET) characteristics using inherent spontaneous polarization in ferroelectric-dielectric polymer PVDF-TrFE. Accounts of analysis of high-resolution scanning microscopy measurements are presented to understand the structure-property relationship in the light of the realization of high-performance OFETs. The increase in the carrier mobility of the electric-field (EF) poled device correlates with the (EF) magnitude and evolution of dielectric microstructure and exhibits an enhancement beyond 300%. The enhanced interfacial transport property appears to have its origin in the dipolar orientation and nanostructure evolution at the interface.

In Chapter 5, channel length dependent current-voltage characteristics of lateral MSM devices using HOIP with symmetric (Au-Au & Al-Al) and asymmetric (Al-Au) electrodes are studied under light and dark conditions. Asymmetric current-voltage characteristics of Au-Al devices are systematically probed using scanning photocurrent microscopy. Highly localized photo generation near the Al-contact under reverse bias is explained using HOIP electronic properties and metal-semiconductor energetics. Analysis of the spatial variation and bias dependence of the local photocurrent allows

the mechanisms of photo carrier transport and collection to be identified in hybrid systems.

In Chapter 6, a light dependent position sensitive detector (PSD) using an active layer of organic inorganic halide perovskite is demonstrated. The lateral device is fabricated using indium tin oxide coated glass as common back electrode and gold as the top electrode. Apart from the linearity and the large span of position sensing range, the PSD response is characterized by a sizable responsivity. The device geometry for PSD also permits a high spatial resolution and transient signal mapping of the lateral photo voltage. The results can be understood in the framework of drift-diffusion model and offers another valuable utility from hybrid perovskite systems.

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Chapter 2

Materials and Methods

2.1 Introduction

The properties of a material, its processing conditions and fabrication procedure have a high impact on the device performance. The key parameters to consider during the selection of materials and fabrication processes are (i) the use of high mobility, stable semiconductors (ii) energy level compatibility between adjacent layers and with electrodes to avoid the formation of energy barriers which are futile to the charge injection (iii) solution processability.[1-4] Also, the orthogonality of solvents is to be ensured to prevent the formation of morphological defects and intermixed layers at interfaces.[5-7] This chapter discusses polymer semiconducting and dielectric materials used for OFET fabrication and hybrid perovskite material used for lateral MSM device and position sensitive detectors.

2.2 Polymer Semiconductor

2.2.1 P3HT

P3HT is a polythiophene derivate, whose properties are widely studied in the last two decades, which make it a model system for fundamental studies on charge transport.[8] Also, it has been used in wide variety of applications such as photovoltaics,[9] PFETs and photodetectors.[10, 11] P3HT can be easily prepared using standard cross-coupling chemistry with a controlled molecular weight, regioregularity, and precise end-group functionality and the hexyl chains on either sides of the thiophene subunits gives high solubility to the molecule in common organic solvents such as

chloroform and chlorobenzene.[12] Earlier section: 1.10 described the importance of molecular ordering and orientation in charge transport mechanism. An edge-on orientation (**Figure: 1.11a**) of molecules is preferred for a favorable charge transport in FET system, since it will offer an extended π-π coupling along the transport pathway.[13] Regioregular P3HT (rr-P3HT), which have a head-to-tail arrangement as shown in **Figure: 2.1** along the chain can stack together to form a predominantly edge-on configuration.[14] rr-P3HT from American Dye Corporation having following specifications was used in the device fabrication (i) molecular weight(MW) ≈ 87000 g/mol, (ii) poly dispersity index (PDI) =1.2, and (iii) regioregularity > 98%. 10 mg/ml solution of rr-P3HT in anhydrous chlorobenzene (CB) was used for film fabrication. Thin films were prepared on dielectric via static dispense spin coating using 60µl of the P3HT solution. Post-annealing of the films was carried out at 90^0C for 30 min. in an inert atmosphere, to improve the crystallinity, packing and to remove any residual solvents in the film.

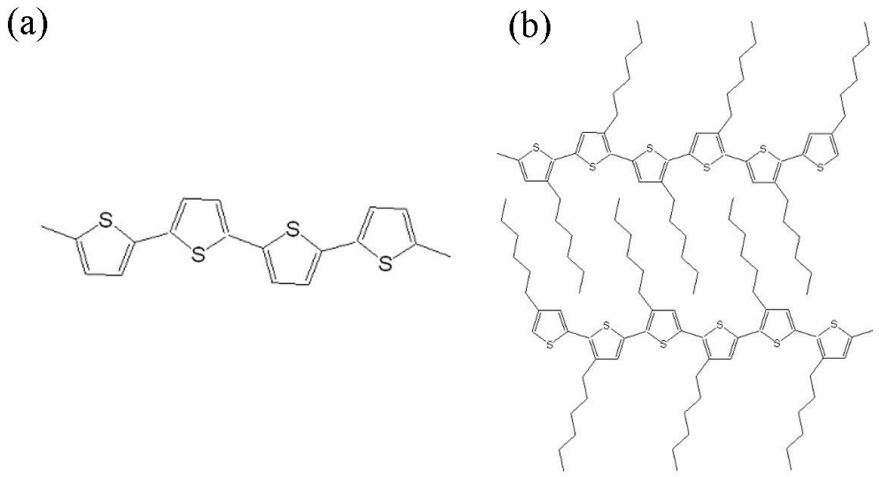

Figure 2.1: *(a) Chemical structure of polythiophene, (b) head-to-tail arrangement of molecules in rr-P3HT.*

2.2.2 PBTOR

BTzOR-based polymer semiconductors shows high solubility in common solvents, extensive conjugation, low optical bandgaps, and high crystallinity, high μ_{FET}^{h} (0.06 – 0.25 $cm^2/(Vs)$), as well as significantly enhanced I_{on}:I_{off} ratios and ambient I-V stability. The high μ_{FET}^{h} of the BTzOR-containing head-to-head polymers arises due to higher degree of backbone coplanarity induced by following factors (i) attractive (thiazolyl)S···O(alkoxy) van der Waal interaction in the sub unit due to thiazol, **Figure: 2.2** (ii) by eliminating C–H···H–C interactions which normally occur in thiophene based polymers.[15, 16] These structural features allow the molecule to achieve better packing to facilitate improved charge transport properties.

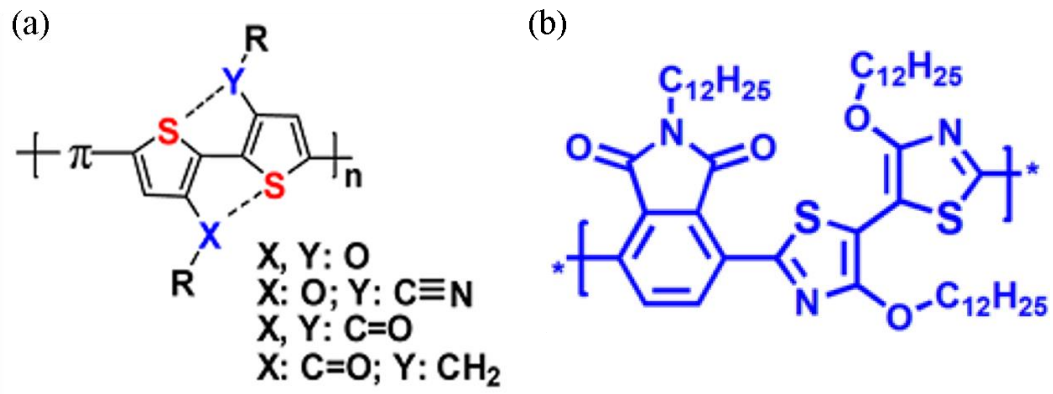

Figure 2.2: *(a) Head-to-head linkages via intramolecular S···O conformational locking; S···O = S(thienyl)···O(alkoxy) and S(thienyl)···O(carbonyl). (b) Chemical structure of PBTOR (Reproduced from Reference [15]).*

PBTOR procured from Polyera Active Inc. was used for PFET fabrication without further filtration. 10 mg/ml of the polymer solution in chlorobenzene was spin coated on the dielectric at 800 rpm and annealed at 90°C for 30 min, in the N_2 glove box to obtain a uniform film of thickness ~ 80 nm.

2.3 Dielectric: PVDF-TrFE

Polyvinylidene fluoride (PVDF) is a semicrystalline polymer having a relatively large dielectric constant (ε_r > 10) and a high DC breakdown strength (E_{bd} ~ 770 MV/m).[17, 18] PVDF produced from homopolymer (i.e., from 100% CH_2=CF_2 monomer) have a regular structure of alternating CH_2 and CF_2 groups. PVDF exist in four polymorphous forms viz, α, β, γ, and δ phases depending on the chain conformation, among which α, β phases are most commonly obtained.[19] The chain conformations of α, β phases are shown in **Figure: 2.3a**. The polar β phase with the zigzag (all-trans) confirmation is of interest in this work owing to its high (semi-)crystallinity and FE properties among all of the PVDF polymorphs.[20] The electrostatic properties of PVDF arise from the high difference between the electro-negativity of the fluorine atoms and other atoms such as carbon and hydrogen in the monomer unit. The resulting molecular dipoles in the monomer unit (CH_2-CF_2) are aligned perpendicular to the main chain axis as shown in **Figure: 2.3a**. The energy required to form the all-trans form decreases with increasing defect groups. Thus a random copolymer P(VDF-TrFE) synthesized using PVDF, and a comonomer polytrifluoroethylene (PTrFE) will increases the unit cell size and inter planar distance of the ferroelectric phase, resulting in a reduced dipole-dipole interaction. Also, it results in elevated remnant polarizations and crystallinity in P(VDF-TrFE), in addition to lowering the Curie temperature (T_c ~ 110 ^{0}C) allowing it to crystallize into ferroelectric phase below the melting point (T_m ~ 150 ^{0}C).[21] The crystal structure, phase transition and ferroelectric properties are affected by the ratio of VDF/TrFE content and the processing conditions.[22, 23] They have been widely considered to be the materials of choice for various polymer ferroelectric (FE) and

piezoelectric (PE) applications such as electronic memory devices, polymer transistors, sensors, and actuators.[24]

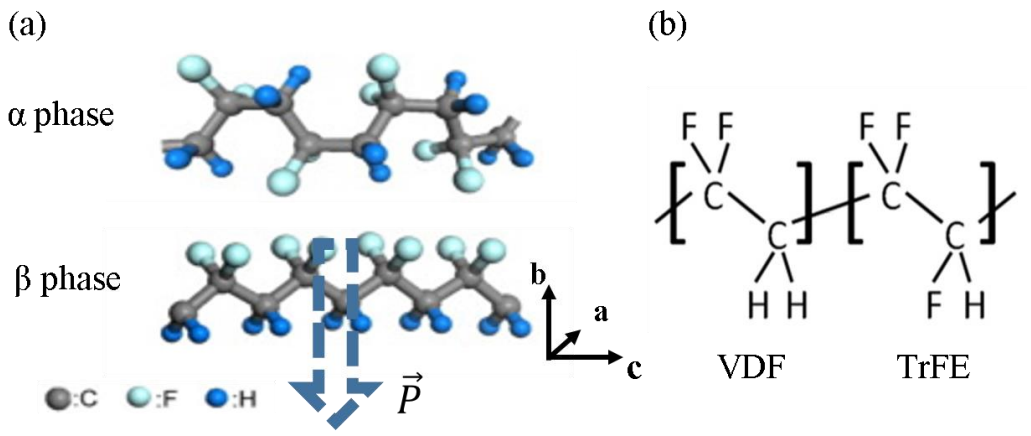

Figure 2.3: *(a) Schematic of α, β phase configurations of PVDF molecule, the direction of dipole moment in a monomer unit is shown as a dotted arrow in the figure, c-axis represents the molecular axis in PVDF, (reproduced from Reference [20]) (b) chemical structure of P(VDF-TrFE) random copolymer.*

P(VDF-TrFE) having molar composition of 75:25 of VDF:TrFE procured from Sigma Aldrich is used in the preparation of PFET gate insulating layer. The copolymer was first dissolved in N-N dimethylformamide (DMF) and thoroughly dissolved overnight using a magnetic stirrer. Post-annealing was carried out at 145 ^{0}C for 120 min. in inert atmosphere to increase the crystallinity and ferroelectric characteristics of the film.

2.4 Methyl Ammonium Lead Iodide ($MAPbI_3$)

There is a large class of hybrid perovskite compounds with promising optoelectronic characteristics. Out of those, methyl ammonium lead iodide $MAPbI_3$, has

been most extensively investigated and can therefore be seen as a standard perovskite and a model compound. Crystal structure of $MAPbI_3$ is shown in **Figure: 2.4**.

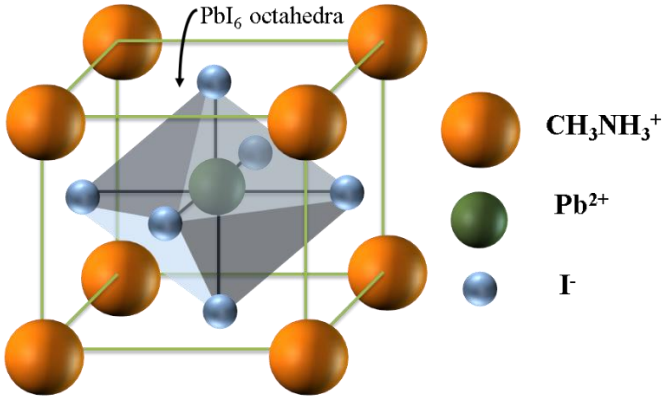

Figure 2.4: *Crystal structure of $MAPbI_3$ at room temperature.*

Methyl ammonium iodide (MAI) and lead iodide (PbI_2) purchased from Dyesol was used without further purification. $MAPbI_3$ films were prepared using one step solution method from a 40 wt.% solution made using 1.05:1 molar ratio of MAI:PbI_2 in dimethyl sulfoxide.[25] The solution was thoroughly mixed for 5 hours using magnetic stirrer. Solution is then spin coated on the substrate at 5000 rpm for 80 sec to obtain a thin film of thickness ~ 80 nm. Post-annealing of the film was carried out at 100 ^{0}C for 60 min. in an inert atmosphere to assist the $MAPbI_3$ film formation.[26]

2.5 Device Fabrication

OFET and lateral MSM devices were fabricated on an optically flat BK7 glass substrate, while Indium tin oxide (ITO) coated glass substrates with a sheet resistance of 15 $\Omega.cm^{-2}$ was used for PSD fabrication. Substrates cut to 1x1" size were first cleaned by RCA procedure before film coating. RCA is a method of chemically removing the organic residue from the substrate based on sequential oxidative desorption and complexing of the residue with hydrogen peroxide (H_2O_2)-ammonia solution (NH_4OH)-

deionized water (DI-H_2O) mixture.[27] A step by step account of the procedure is given below,

(i) Ultrasonic cleaning of substrates in a soap solution, at 70 ^{0}C for 10 min.

(ii) Ultrasonic cleaning the substrates in DI-H_2O for 10 min.

(iii) Ultrasonic cleaning the substrates in 1:1 mixture of Isopropyl alcohol and Acetone for 10 min.

(iv) Soak the substrate in a mixture of H_2O_2:30 % NH_4OH: DI-H_2O (1:1:5 by volume). The solution is heated up to100 ^{0}C, and maintained for ~2 min.

(v) Ultrasonic cleaning the substrates in DI-H_2O for 10 min.

(vi) Wash the substrate in DI-H_2O, and then blow dry under N_2 flow.

The quality of the RCA was monitored by the contact angle of water on the cleaned substrate. A good RCA cleaning will result in complete wetting of the substrate by water.

2.5.1 PFET

PFETs were fabricated in TC-BG geometry. Al/Au gate electrodes were thermally evaporated at 10^{-6} mbar vacuum on to an RCA cleaned BK7 substrate using precut shadow masks. Al-electrodes used for poling the dielectric is thermally evaporated orthogonal to the gate electrode. This was followed by spin coating of P(VDF-TrFE) dielectric layer. Spin coating speed and duration are optimized for a thin dielectric coating while maintaining a low leakage current through the insulator. Necessary post-processing of the dielectric was performed to ensure the desired

structural phase and surface roughness. Polymer semiconductor is then spin coated on the dielectric surface to obtain a thin, uniform film covering the channel area. Post-annealing of the semiconductor layer is performed to remove any residual solvent and to achieve better packing of the polymer molecules. Source/drain electrodes were thermally evaporated on to the semiconducting surface using a shadow mask with a predefined channel length. The evaporation rate of the electrode materials was maintained to obtain a smooth metal-semiconductor interface. Schematic of the step by step procedure of PFET fabrication is shown in the **Figure: 2.5**.

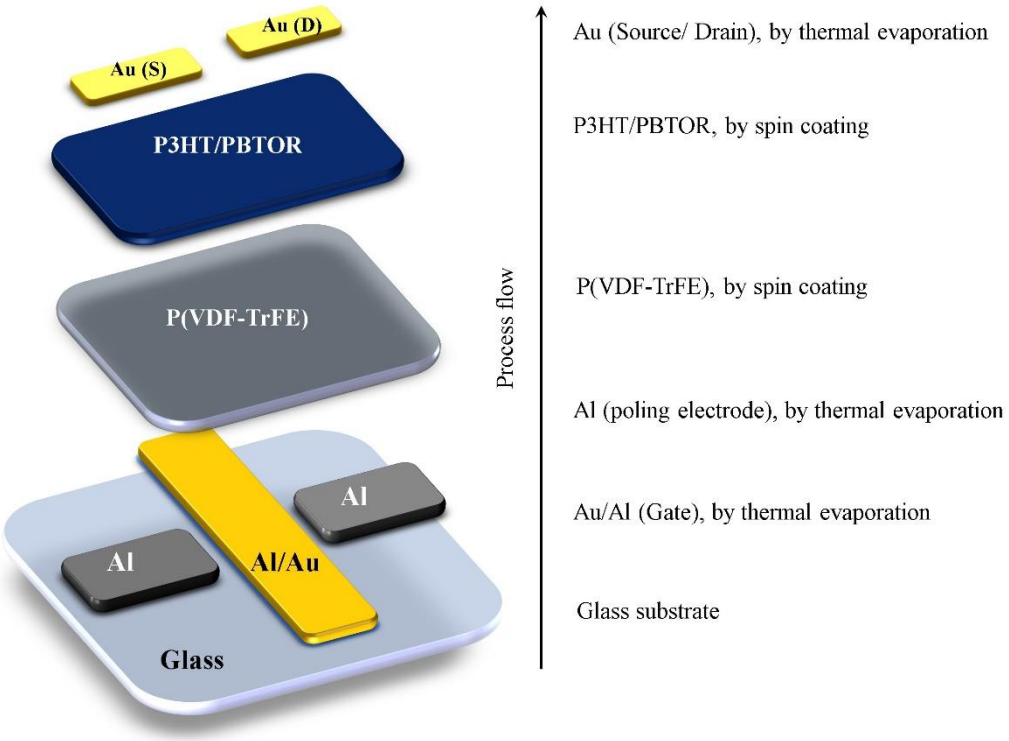

Figure 2.5: *Schematic of a step-by-step description of PFET fabrication.*

2.5.2 Lateral MSM Devices

Devices were prepared on cleaned glass substrates. Two parallel electrodes (Al or Au) were thermally evaporated at ~10^{-6} mbar using a predefined shadow mask.

Asymmetric electrode (Al-Au) were deposited in two steps. The shadow masks were designed to have an electrode width of W~2 mm and channel length L~10-70 µm. Optical quality HOIP films were prepared by a single-step method *via* solution processing. $MAPbI_3$ solution (40 wt.%) in dimethyl sulfoxide (DMSO) with 1.05:1 molar ratio between MAI and PbI_2 was spin coated at 3000 rpm for 80 sec covering both the electrodes. Additive 2,2′,2"-(1,3,5-Benzinetriyl)-tris(1-phenyl-1-H-benzimidazole) (TPBi) was spin coated from chloroform at 5000 rpm for 10 sec at the end of the earlier step.[28] The film was annealed at 100 ºC for 60 min. in N_2 filled glove box while keeping ultra-low oxygen level. Schematic of lateral MSM device fabrication is shown in **Figure: 2.6**.

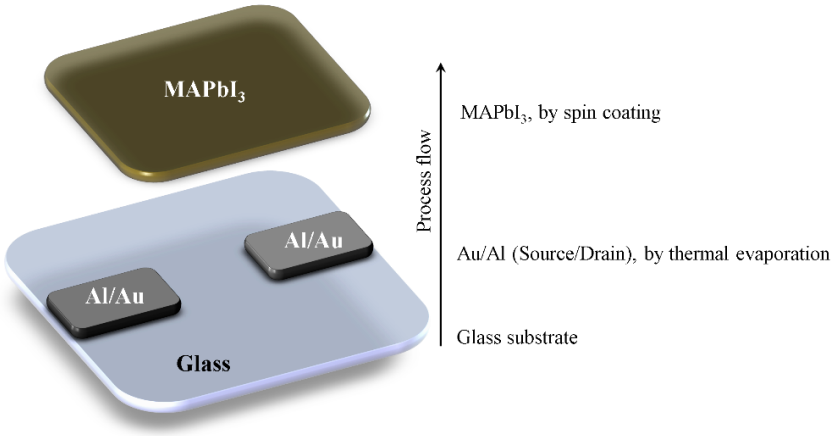

Figure 2.6: *Schematic of lateral MSM device fabrication.*

2.5.3 Position Sensitive Detector

PSDs were fabricated on ITO substrates. Optical quality HOIP films were prepared on patterned ITO substrate using the $MAPbI_3$ solution as described in the previous section. It was followed by spin coating of a very thin layer of acceptor polymer poly[2,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,2'- bithiophene)] (N2200). 40 nm of

gold electrodes was thermally evaporated on the perovskite film using predefined shadow masks. The step-by-step procedure of a PSD fabrication is shown in **Figure: 2.7**.

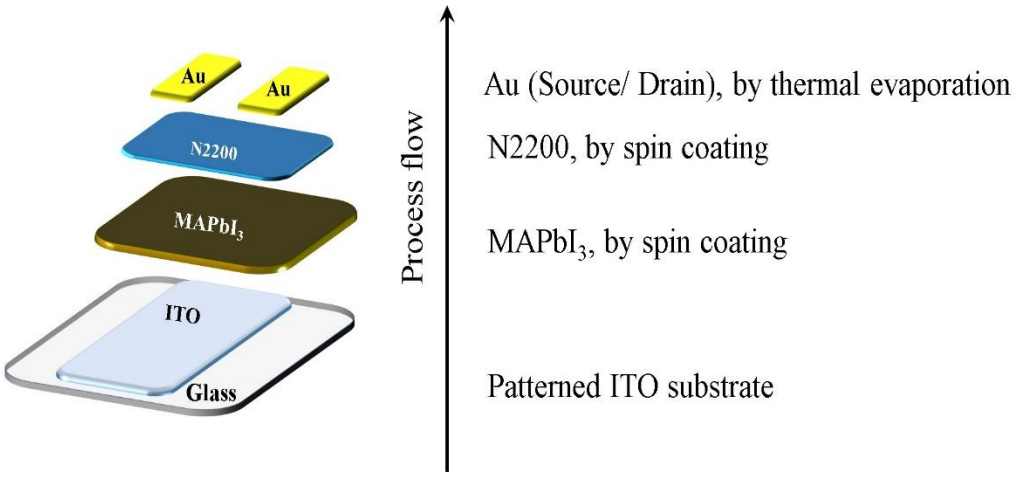

Figure 2.7: *Schematic of PSD fabrication procedure.*

2.6 Experimental Techniques

2.6.1 X-ray Diffraction Measurement

X-ray diffraction (XRD) measurements were performed using Bruker axs D8-Discover with Cu K-α source. Thin films samples were prepared on RCA cleaned BK7 glass for the measurement. Bruker axs D8-Discover with Cu K-α source was used for the measurement. Scans were performed in steps of 0.0045 ^{o}.

2.6.2 UV/VIS Absorption Measurement

Absorption measurements on thin films were carried out using Perkin Elmer UV/ Vis Spectrometer Lambda-750. The samples for measurements were prepared as thin films coated on RCA cleaned quartz substrates.

2.6.3 DC Characterization

The output and transfer characteristics of OFETs were measured using Keithley SCS 4200. The measurements were performed in a vacuum chamber (10^{-3} mbar) fitted with external electrical connection. Device parameters such as field effect mobility(μ_{FET}^{sat}), on-off ratio (I_{on}/I_{off}), threshold voltage (V_{th}) were extracted from the expression $I_{ds,sat} = \frac{W}{2L}\mu_{FET}^{sat}C_i\left(V_{gs} - V_{th}\right)^2$, where $I_{ds,sat}$ is the saturation source-drain current, W is the width of the transistor channel, L is the length of the channel, C_i is the capacitance per unit area of the gate dielectric, V_{gs} is the applied gate voltage.

2.6.4 Optoelectronic Measurement

Current-voltage characteristics of MSM devices under global illumination were measured from top side (HOIP side) of the device as shown in **Figure: 2.8a**. The devices were kept under vacuum during the measurement. 532 nm wavelength continuous wave (CW) laser diode along with neutral density filters was used for the illumination of the devices. Photoresponse was recorded using Keithley SCS 4200.

Non-uniform illumination of the channel region of PSD and the local photocurrent scan was carried out by using a home built large-area high-resolution laser beam induced photocurrent (LBIC) scanning setup, as shown in **Figure: 2.8b**. 532 nm diode laser was used as the light source. The light was illuminated from the ITO side during the measurements. An external driver circuit driven by a function generator reference signal was used to modulate the laser. The same reference signal was coupled to SRS 830 Lock-in amplifier for a phase locked detection of photogenerated signal from the device. 50x, 0.45 NA microscope objective was used to obtain a tightly focused light spot (radius < 8 μm) on the sample plane. The device under test was placed on a

sample holder situated on top of Thorlab xyz motion controller with 5 μm resolution. *LabVIEW* program was used for instrument control, data acquisition and display. A Silicon photo-detector placed just above the sample surface was used to capture the transmitted image of the sample.

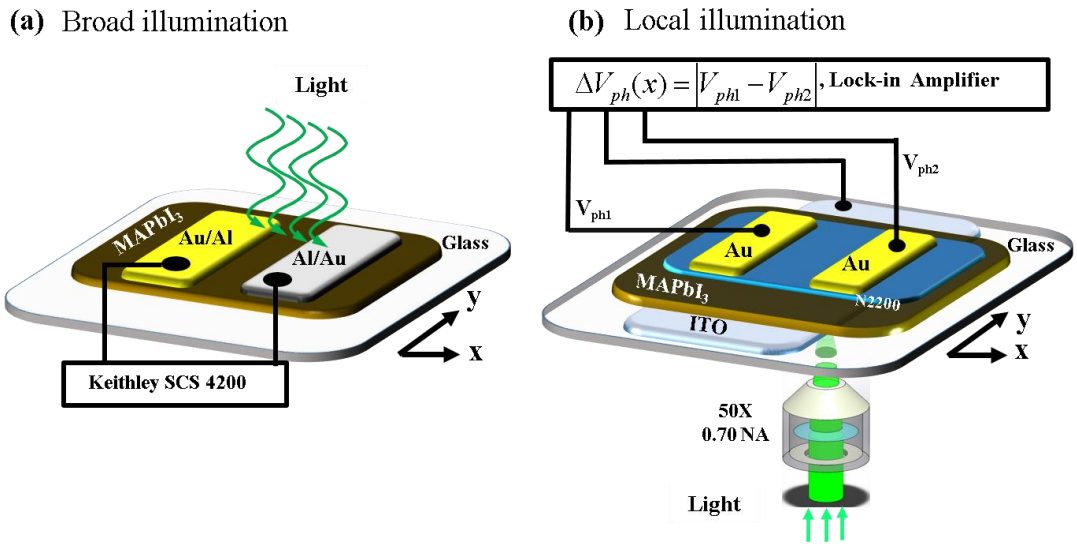

Figure 2.8: *Schematic of (a) photoresponse measurement of HOIP MSM device under broad illumination mode (b) lateral photosignal measurement setup in a bottom illumination mode. Sample mounted on an x-y stage is controlled at micron scale precision.*

2.6.5 Transient Response Measurement

Transient measurements on PSD was carried out by monitoring the signal across the Au-electrode and the ITO electrode in response to a 50 ns pulse laser source (**Figure: 2.9**). The laser illumination spot (λ = 532 nm laser with 320 µW power) is scanned across the channel from the overlapping electrodes (x = 0) towards the center of the PSD channel. The photocurrent signal from the sample was amplified using a trans-impedance preamplifier (SRS570) before coupling it to an oscilloscope. The transient

photocurrent was monitored using a Lecroy 6100A oscilloscope in DC coupling mode with a bandwidth 1.25 GHz and impedance of 50 Ω and the results were verified using a high speed calibrated photodiode.

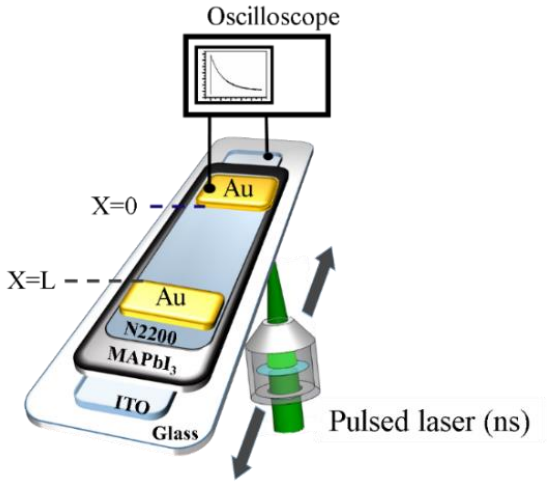

Figure 2.9: *Schematic of the transient response measurement of PSD. The direction of scan is represented in the as arrows in the figure.*

2.6.6 Atomic Force Microscopy (AFM)

JPK Nanowizard 3 AFM was used to measure the surface topography and phase contrast of the region of interest (ROI) on the sample surface. Schematic of the AFM measurement setup is shown in **Figure: 2.10**. Various AFM cantilevers depending upon the mode of operation (contact/noncontact) and property of interest (conducting/non-conducting) were used in the measurement. The contact force was set using force-distance curve before each scan to apply optimal force on the sample surface. Aluminum coated cantilevers from Budget Sensors with nominal spring constant 40 N/m and frequency 300 kHz was used for non-contact scanning of the samples for surface topography and phase contrast measurement.

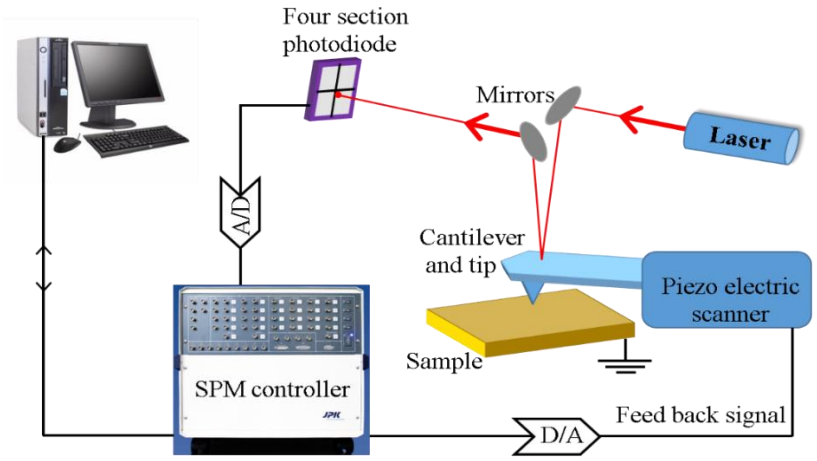

Figure 2.10: *Schematic of AFM setup for surface topography and phase contrast measurement.*

(a) Piezo Force Response Microscopy (PFM)

Piezo force response microscopy (PFM) measurements were carried out using an Ir/Pt coated cantilever (SCM-PIT from Bruker) having nominal spring constant 2.8 N/m and resonance frequency of 75 kHz. The samples were grounded during each measurement.

To estimate the piezoelectric response, an AC ($V = V_0 \cos(\omega t)$) signal was applied to the tip during the measurement. A spontaneous polarization on the surface of the sample will give a quantifiable deflection on the cantilever due to an inverse piezoelectric response. The amplitude of tip deflection takes the form $\Delta Z = \Delta Z_0 \cos(\omega t+\varphi)$, where $\Delta Z_0 = d_{33}V_0$,and d_{33} is the piezoelectric coefficient corresponds to the volume change in the material under applied voltage as shown in **Figure: 2.11**.[29] It gives the measure of the amplitude of Vertical PFM (VPFM). The phase difference (φ) between the applied AC signal and PFM signal hold the information about the direction of dipoles on the surface.[30] Similarly d_{15} component of polarization tensor gives

information about the lateral PFM signal (LPFM). The phase contrast in the LPFM can give information about the orientation of the dipoles along the surface of the material. PFM was used in this thesis to measure the local polarization on the surface of P(VDF-TrFE) samples.

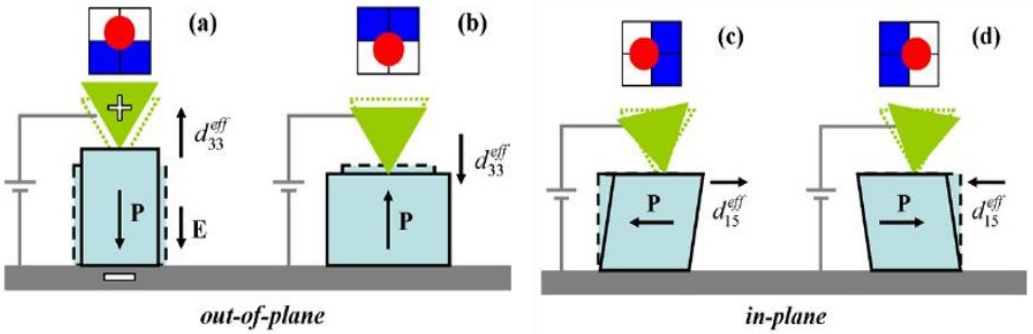

Figure 2.11: *(a) Electric field aligned parallel to the spontaneous polarization leads to a lifting of the cantilever due to the d_{33} effect (out-of-plane signal). (b) The antiparallel alignment of the electric field and the spontaneous polarization leads to a vertical contraction and a horizontal expansion of the ferroelectric. (c), (d) Electric field applied orthogonally to the polarization results in a shear movement due to the d_{15} coefficient. This action causes a torsional deformation of the cantilever forcing the laser spot to move horizontally (in-plane signal). Vertical PFM (VPFM) and lateral PFM (LPFM) signals were recorded in independent channels along with corresponding phase signal. (reproduced from Reference[30]).*

(b) Kelvin Probe Force Microscopy (KPFM)

Kelvin probe force microscopy (KPFM) is used to measure the surface potential on the surface of a sample. A potential difference is developed between the conducting tip of the AFM cantilever and the grounded sample due to difference in their Fermi levels. This contact potential difference can be expressed as $CPD =$

$(\phi_{tip} - \phi_{sample})/q$, where ϕ_{tip} is the potential at the tip of the cantilever and ϕ_{sample} is the local surface potential on the sample and e is the electronic charge. It can be measured as the deflection of cantilever due to the CPD.

KPFM measurements of the devices were carried out in the ambient atmosphere using JPK Nanowizard 3 AFM. Cr/Pt coated cantilever with nominal frequency 75 kHz and force constant 2 N/m was used for the measurement. Cantilever tip potential was calibrated with respect to highly oriented pyrolytic graphite (HOPG) surface before each set of measurements. A constant hover height of 40 nm was maintained during the KPFM scan to obtain maximum signal from the measurement.

(c) Scanning Photocurrent Microscopy (SPCM)

A multimode optical fiber with a tapered end having aperture ϕ ~ 105 nm was used for scanning the channel of MSM device. The optical fiber attached to a tuning fork having resonant frequency, f = 37 kHz and quality factor Q ~ 940 was mounted on the piezo head of the atomic force microscope and operated in near field mode ($d < \lambda$). 532 nm laser operated at 5mW was used as the light source in the measurement. The laser intensity was modulated at 83 Hz using an optical chopper. Modulated light was coupled to the optical fiber using a 20x, 0.40 NA microscope objective lens. The photocurrent signal from the device was amplified using SRS 830 lock-in amplifier (bandwidth ~ 100 kHz) and coupled to JPK scanning probe module (SPM) control for display. A photomultiplier tube (PMT) was used to measure the transmitted light through the device. The transmission map of the device is correlated with the SPCM image to find out the ends of the channel. Ambient light was completely blocked to avoid any external exposure of the sample. The measurements were performed in

ambient air due to practical limitations of mounting the instrument in vacuum. The amount of moisture was controlled by keeping desiccants around the sample holder. A scan of 3 lines typically takes 15 minutes. Schematics of SPCM setup is shown in the **Figure: 2.12**.

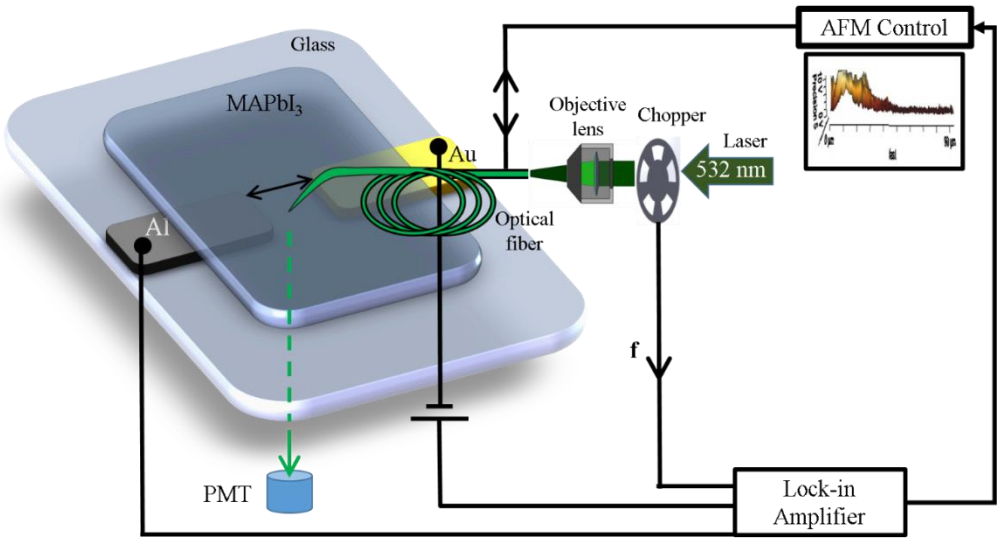

Figure 2.12: *Schematic of SPCM setup in a near-field optical microscopy configuration.*

2.7 Summary

A range of high performance and functional materials were used in the construction of FETs, lateral MSM device and PSDs. Purity of the material and cleanliness of the surfaces were monitored during the fabrication process, also the geometry and processing conditions were optimized for each step of the fabrication to create high performance devices. Special attention was given to the solvents to achieve smooth interfaces. Various characterization techniques were employed to measure the optoelectronic properties and structure-property relations in FETs, lateral MSM devices and, PSDs.

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Chapter 3

Ferroelectric Organic Field Effect-Transistor

3.1 Introduction

OFETs have attracted interest in areas of chemistry, physics, materials, and microelectronics, since the first discovery of organic semiconductors based OFETs in the 1970s.[1,2] On the technological side, OFETs are key components in integrated circuits used plastic smart cards,[2] radio frequency identification (RFID) tags,[3, 4] and organic active matrix displays.[5-7] On the scientific side, OFETs are used as test bed for novel organic semiconductors and studying fundamentals of charge transport.[8, 9] In the past decade, OFETs with added functionalities such as phototransistors, organic memory FETs, organic light emitting FETs, sensors based on OFETs are introduced. Heart of these devices are the materials with various dielectric and optoelectronic properties.[10] Among them, ferroelectric dielectric materials have attracted attention due to their applications in nonvolatile memory devices rendered by the electrically switchable spontaneous polarizations. Also, the large dielectric constant of these materials enables higher charge density and hence lower operating voltage in OFETs. The advent of these materials in organic electronics has opened up additional capabilities to control surfaces and interfaces for fine tuning the molecular, structural and device engineering aspects.[11-13]

The discovery of the piezoelectric properties of poly(vinylidene fluoride) (PVDF) by Heiji Kawai,[14] and the study of its pyroelectric and nonlinear optical

properties led to the discovery of its ferroelectric properties in the early 1970s.[15-17] Since then, considerable development and progress have been made on both materials and devices based on PVDF.[18-20] There are many ferroelectric polymers, such as poly(vinylidene fluoride) (PVDF) copolymers, poly(vinylidene cyanide) copolymers, odd-numbered nylons, polyureas, ferroelectric liquid crystal polymers and polymer composites of organic and inorganic piezoelectric ceramics.[21] Among them, PVDF and its copolymers are the highly investigated and promising ferroelectric polymers because of their large spontaneous polarization, in addition to their chemical stability, resistance to organic solvents, and high elastic modulus compared with other polymers. There are various copolymers of PVDF reported in the literature, such as poly(vinylidene fluoride hexafluoropropylene) (P(VDF-HFP)), P(VDF-TrFE), poly(vinylidene fluoride-trifluoroethylene-chlorofluoroethylene) (P(VDF-TrFE-CFE)) to name a few. High ferroelectricity and crystalline nature of P(VDF-TrFE) among the PVDF copolymers make it the first choice for dielectric in FE-OFETs.

3.2 Device Fabrication

Top contact-bottom gate OFETs (TC-BG OFETs) were fabricated on RCA cleaned BK7 glass substrates Semiconducting polymers PBTOR (poly 4,4'-dialkoxy-5,5'-bithiazole (BtzOR)) from Polyera Active Inc. and P3HT from American Dye Source were used in the device fabrication. 80 mg/ml P(VDF-TrFE) (75/25) copolymer solution from DMF was spin coated on the substrate at 1300 rpm for 60 sec. Post-annealing of the P(VDF-TrFE) was performed at 145^0C for 120 min. in an inert atmosphere. Thermally evaporated 40 nm Chromium-Gold (Cr-Au) electrode was used as the gate electrode. 10 mg/ml of the polymer solution (P3HT/PBTOR) in chlorobenzene was used for the fabrication of semiconducting layer. A homogeneous

solution was prepared by stirring the precursor overnight using magnetic stirrer. The solution was filtered by PTFE filter having 45 µm pore diameter to remove any particles/agglomerates. Semiconducting layer was fabricated by spin casting the solution at 800 rpm for 60 seconds. The film was then annealed at 90^{o}C for 30 min, in the N_2 glove box to remove the solvent and to achieve higher crystallinity of the film. Hence formed films were measured to have a thickness ~ 80 nm. Au electrodes were deposited on the semiconduting layer by physical vapor deposition (PVD) at low pressure ~ 5x10^{-6} mbar. Very low pressure duirng the further helps the removal of any residual solvent. Evaporation of the metal was maintained at a constant rate ~ 1A^{o}/s. Shadow masks were used to define the OFET channel and source-drain electrodes (width: 1-2 mm, length: 40-100 µm). The detailed description of the device fabrication process flow is given in the section: 2.5.1.

3.3 Electronic Characterization

OFET measurements were performed in a vacuum chamber (10^{-3} mbar) with sealed external electrical contacts. The chamber was evacuated for sufficient duration to minimize any residual moisture. Output and transconductance measurements on OFETs were performed using Keithley SCS-4200. IV-scans were done at moderate 0.02s step speed. Representative transfer and output characteristics of P3HT and PBTOR transistors are given in the **Figure: 3.1**. OFET performance parameters were extracted in the saturation regime from the transconductance characteristics using the equation (1.21). The mobility was extracted from the slope of $(I_{ds})^{1/2}$ versus V_{gs} in the saturated region of the transfer curve where the source-drain current is independent of V_{ds}.

$$\mu_{FET}^{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{ds,sat}}}{\partial V_{gs}}\right)^2 \qquad \ldots\ldots (3.1)$$

where $I_{ds,sat}$ is the drain current, W and L are, respectively, the channel width and length, C_i is the capacitance per unit area of the gate insulator layer for each transistor, and V_{gs} is the applied gate voltage. Capacitances per unit area was measured from Metal-Insulator-Metal capacitor created alongside with each OFET. A C_i of about 45 nF/cm^2 was calculated from the measured data of the capacitor at 1 V and frequency of 1kHz. Characteristics were calculated from a sample space of a large number of (> 10) PBTOR and P3HT ferroelectric OFETs.

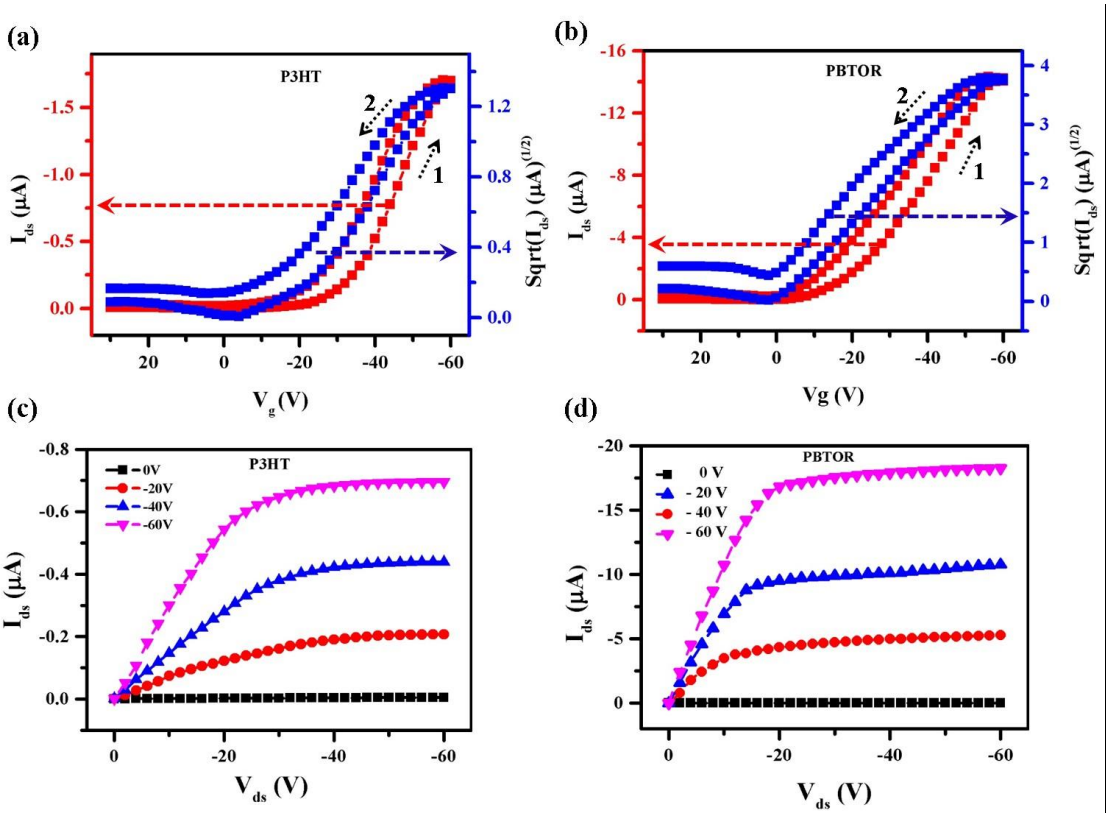

Figure 3.1: *Representative transfer and output characteristics of P3HT (a) & (c) and PBTOR (b) & (d) OFETs. The direction of voltage sweep is indicated in the figure. Transfer characteristics exhibit finite hysteresis due to the ferroelectric dielectric.*

PBTOR and P3HT transistors exhibited p-type mobilities μ_{FET}^{h} ~ 3.5x10^{-2} cm^2/(Vs) and 9x10^{-3} cm^2/(Vs). The μ_{FET}^{h} is comparable to that of similar OFET structures reported in literature.[22] A novel method using external electric field to extract higher charge transport performance form these structures is discussed in the next chapter.

3.4 Polarization-Electric Field Characterization (P-E)

P-E loop measurement was performed to understand the ferroelectric nature P(VDF-TrFE) thin films. 350 nm P(VDF-TrFE) films sandwiched between Au electrodes are used for the measurement. A 40 nm thick gold electrode deposited on BK7 glass serves as the bottom contact. Top gold electrode having 40 nm thickness was fabricated by thermal evaporation on top of the spin coated P(VDF-TrFE) film. Precision Premier II tester from Radiant Technologies, Inc. was used for the measurements. Measurements were performed under ambient condition. Polarization hysteresis loops are measured by applying triangular pulses from −8 to 8 MV/m, between top and bottom electrodes of the samples. Each measurement was normalized to the area of the device. The P-E curve of P(VDF-TrFE) film is shown in the **Figure: 3.2**. P(VDF-TrFE) films exhibited ferroelectric characteristics even though the values are not high. The effect of sizable amount of ferroelectricity present in the P(VDF-TrFE) gate dielectric corroborate with the finite hysterics observed in the transfer characteristics of the OFETs, as shown in the **Figure: 3.1**.

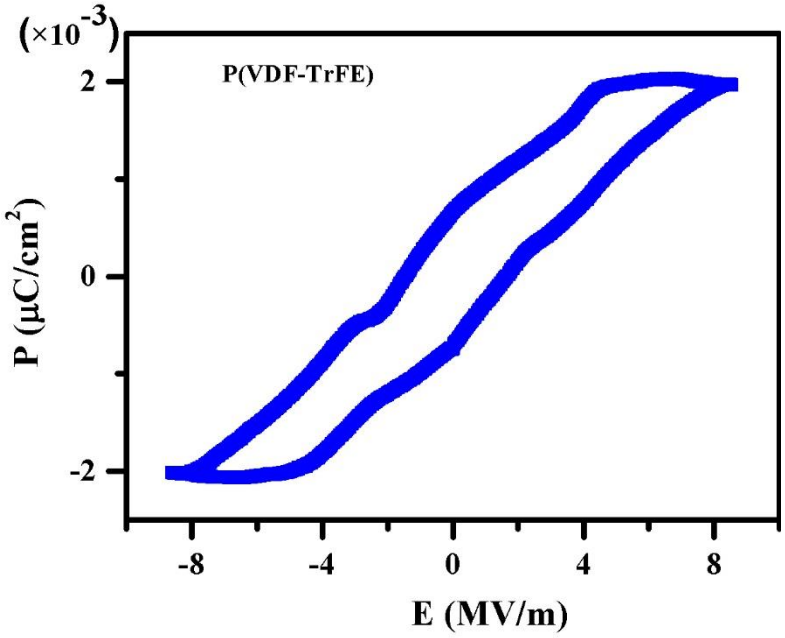

Figure 3.2: *Polarization-Electric field curve of Au/P(VDF-TrFE)/Au devices.*

3.5 X-ray Spectrum Analysis

XRD measurements were performed on the P(VDF-TrFE) film to analyze the crystallinity of the film and to find the fraction of *β* phases present in the fim. The measurements were carried out on P(VDF-TrFE) samples using Bruker axs D8-Discover with Cu K-α source. Scans were performed in steps of 0.0045 °. The XRD spectra of P(VDF-TrFE) films grown on BK7 glass is shown in **Figure: 3.3**. Peak present at 19.8° is attributed to the (110) and (200) orientation planes, which are associated with the polar *β* phase. From the position of this sharp peak, the inter-planar spacing is determined to be ~ 4.48 Å which indicates that the chains are packed on a hexagonal (or pseudo-hexagonal) lattice of axial length of 5.17 Å.[23] The second peak at 18.0° shows the presence of paraelectric *α*-phase coexisting along with ferroelectric *β* phase.

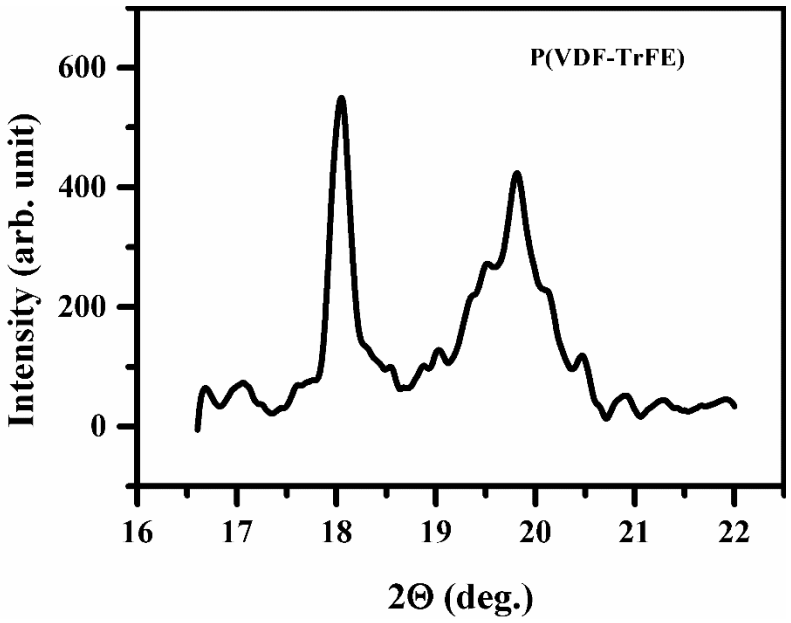

Figure 3.3: *X-ray spectrum of P(VDF-TrFE) thin film annealed at 145^{0}C for 120 minutes.*

3.6 Summary

Ferroelectric-OFET is demonstrated using copolymer P(VDF-TrFE) and P3HT and highly ordered PBTOR semiconductor. PBTOR FE-FETs exhibited higher field-effect mobility compared to that of P3HT transistors. The effects of improved packing of molecule and coplanarity are reflected in the performance of PBTOR FE-OFETs.

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Chapter 4

Electric Field Induced Ferroelectric-Surface Modification for High Mobility Organic Field Effect Transistors

4.1 Introduction

A decisive factor in OFET performance arises from the organization of the charge transport layer at the semiconductor-dielectric interface as mentioned in section: 1.10.[1-3] The assembly and organization of the charge transporting molecule in an OFET depends on the intrinsic properties of the material as well as the chemical, dielectric and structural properties of underlying gate insulator layer. An appropriate pair of dielectric and semiconductor which results in optimum surface microstructure can significantly enhance FET characteristics.[4-6] A novel pattern-free method is introduced in this chapter for the fabrication of efficient OFETs well suited to solution process to further enhance the device properties. This strategy involves electrostatic modification of the semicrystalline dielectric (ferroelectric) substrate, to enable a higher degree of order for the deposited semiconductor in the bottom gate OFET structure. Even though the mobility value of the assembled semiconducting polymers are not extraordinarily high, the results present a direct evidence of correlation of dielectric surface-structure and OFET performance. Ferroelectric polymer P(VDF-TrFE) is used as the gate dielectric layer in this study as they can give a handle to control the polarization direction at the interface.

4.2 Device Fabrication

Top contact-bottom gate OFETs (TC-BG OFETs) were fabricated on RCA cleaned BK7 glass substrates as described in section 2.5.1. Al electrodes for poling were deposited on the glass substrate orthogonal to the gate electrode. P(VDF-TrFE) was spin coated on top of these electrodes. DC voltage is applied on the poling electrodes during the post-annealing of the P(VDF-TrFE). Control samples were prepared without applying DC field during annealing of the dielectric. Distance between the poling electrodes and the applied voltages were optimized to maintain the electric field well below the dielectric breakdown field. Post-annealing of the spin coated semiconductors were carried out at 90^0C for 30 minutes inside a N_2 filled glove box. Predefined masks were used for thermal evaporation of electrodes. A typical image of OFET device is shown in **Figure: 4.1**.

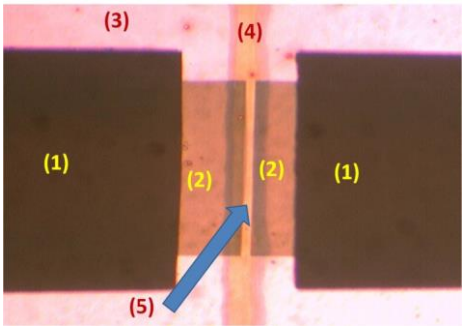

Figure 4.1: *Image of an actual OFET device with poling electrode (top view), each part of the OFET is numbered, and typical dimensions are given below.*

(1) Aluminum poling electrode (width: 3-3.5 mm)

(2) Gold source-drain electrode (width: 1-2 mm)

(3) PBTOR/P3HT (thickness: 80-200 nm)

(4) Gold gate electrode (thickness: 40-45 nm)

(5) Channel (width: 1-2 mm, length: 40-100 µm).

4.3 Electronic Characterization

OFET measurements were performed and the parameters were calculated as explained in section 3.3. It was ensured that the presence of the poling electrodes did not alter the typical OFET and leakage characteristics. Typical transfer and output characteristics of P3HT and PBTOR transistors made using EF treated P(VDF-TrFE) dielectric layer are given in **Figure: 4.2**. Characteristics of control OFETs fabricated with non-EF treated P(VDF-TrFE) is also shown in the figure. OFET performance parameters were extracted in the saturation regime from the transconductance characteristics using the equation (3.1).

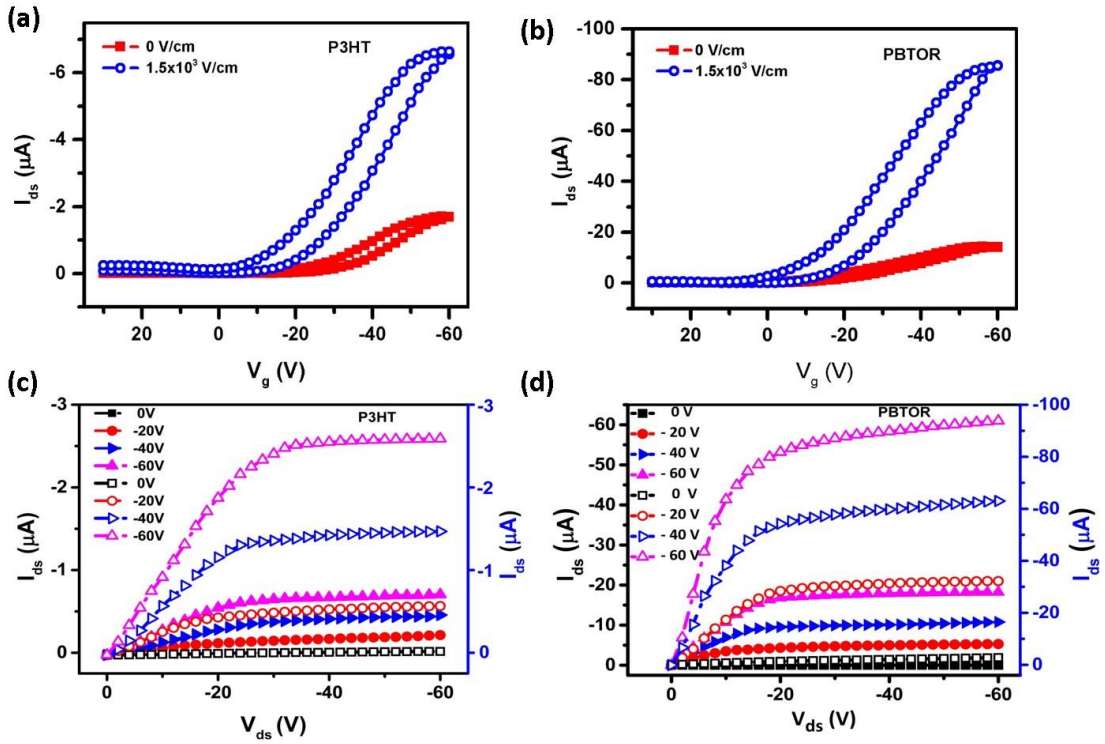

Figure 4.2: *Representative (a) transfer characteristics and (c) output characteristics of P3HT OFETs. Representative (b) transfer characteristics and (d) output characteristics of PBTOR OFETs. Hollow symbols represent EF treated samples. Solid symbols represent the characteristics of control samples where no EF is applied.*

Output and transfer characteristics shows an increase in the current in OFETs with EF treated dielectric layer. The improvement in the transistor current is independently verified by P3HT and PBTOR. Subthreshold slope, threshold voltage and On-Off ratio of measured devices are shown in the **Table: T1**.

P3HT				PBTOR			
EF (V/cm) x (10^3)	S (V/dec)	V_{th} (V)	ON/OFF	EF (V/cm) x (10^3)	S (V/dec)	V_{th} (V)	ON/OFF
0.00	15.3	-18.4	10^4	0.00	14.1	-17.3	10^4
0.44	15	-17.9	10^4	0.42	14.1	-17	10^4
0.65	15.2	-17.1	10^4	0.60	14.2	-16.4	10^4
0.66	14.8	-16.8	10^4	0.70	13.8	-15.8	10^4
0.73	14.6	-16.3	10^4	0.75	13.6	-15.3	10^5
0.90	14.1	-15.6	10^4	0.89	13.5	-14.9	10^5
1.26	13.6	-15.2	10^5	1.30	13	-14.3	10^5
1.37	13.1	-14.8	10^4	1.44	12.6	-13.9	10^4
1.48	13.1	-14.6	10^4	1.57	12.6	-13.8	10^4
1.86	13.8	-15.6	10^4	1.99	12.6	-14.6	10^4
				2.34	13.9	-15.2	10^4

***Table T1**: Subthreshold slope, threshold voltage, On-Off ratio of measured OFET devices.*

4.4 Polarization-Electric Field Characterization (P-E)

Ferroelectric phase of P(VDF-TrFE) was verified experimentally by P-E loop characterization, Measurement was performed on EF treated and control samples of 350 nm P(VDF-TrFE) film sandwiched between electrodes. The P-E curve of P(VDF-TrFE) films measured is shown in the **Figure: 4.3**. The P-E curve shows that the EF treated dielectrics have higher remanent polarization compared to control samples. However, a very high (> $2.0x10^3$ V/cm) EF treatment is shown to be detrimental to the ferroelectric character of the film, as shown in the red curve in **Figure: 4.3**. The structural effect of EF treatment is analyzed using XRD measurement as presented in the next section.

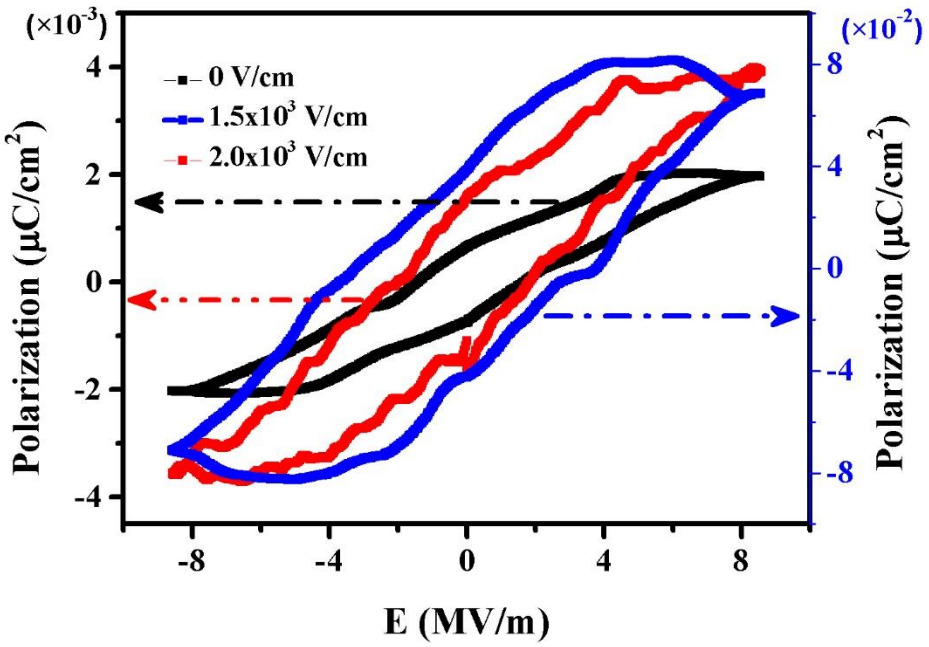

Figure 4.3: *Polarization-Electric field curve (P-E) of EF treated P(VDF-TrFE) film. P-E curve of control sample is shown as black curve.*

4.5 X-ray Spectrum Analysis

Detailed structural characteristics were examined by X-ray characterization of the electric field (EF) treated films. X-ray diffraction measurements carried out on samples EF treated at 0 V/cm, 5×10^2 V/cm, 1.1×10^3 V/cm, 1.5×10^3 V/cm and 2.1×10^3 V/cm are shown in **Figure: 4.4** reveals a systematic trend. Lower EF results in a combination of α, β and γ phases coexisting in the film. Major peaks present in the XRD spectrum are 18.0°, 18.7° and 19.8°. Presence of peaks at 18.0°, 18.7° indicate paraelectric α phase and γ phase coexisting with β phase at lower EF.[7] Intermediate EF, 1.5×10^3 V/cm results in maximum β phase character, with a sharp peak at ~ 20° which is attributed to the β phase of P(VDF-TrFE) and highest crystallinity (**Table: T1**) as shown in the X-ray diffraction pattern.[8]

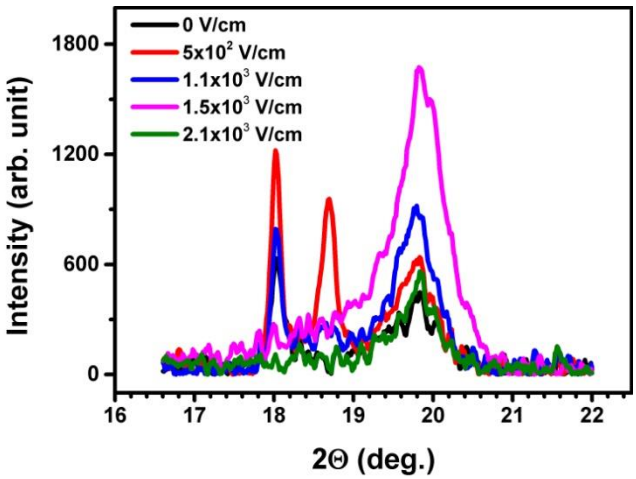

Figure 4.4: *X-ray spectrum of P(VDF-TrFE) film grown under various EF.*

Higher β phase contribution is evident from the Polarization-Electric field curve also as shown in **Figure: 4.3** and from the Vertical Piezo response force (VPFM) microscopy images as shown in **Figure: 4.7**. The intensity maxima and Full-width half maxima (FWHM) of this β phase feature is a function of EF. A clear and monotonic increase in the intensity accompanied by a decrease in FWHM with EF reveals an increase in order and crystallinity (**Table: T2**).

E.F (V/cm)	Angle (2θ, deg.)	Crystallite size, d (nm)	Angle (2θ, deg.)	Crystallite size, d (nm)	Angle (2θ, deg.)	Crystallite size, d (nm)
0	18.04	48.13			19.77	13.21
5×10^2	18.02	66.62	18.69	44.82	19.75	13.17
1.1×10^3	18.03	76.16	18.71	21.91	19.77	12.56
1.5×10^3					19.84	15.32
2.1×10^3					19.79	11.97

Table T2: *XRD peaks in P(VDF-TrFE) film and crystallite sizes.*

4.6 Microstructure and Piezo Force Response Analysis

Atomic force microscopy (AFM) measurements were carried out using JPK Nanowizard 3 AFM. A Cantilever having gold reflective coating on detector side and nominal resonance frequency of 280 kHz was used for surface topography

measurements. Piezoresponse force microscopy (PFM) measurements were performed using Bruker Dimension Icon AFM-Raman system. Pt/Ir coated conducting cantilever with nominal frequency of 75 kHz was used for PFM measurement.

High-resolution AFM imaging of the dielectric layer also reveals a formation of sizable crystalline regions with EF treatment. This feature of well-defined regions increases with EF up to a threshold electric field (EF_{th}) magnitude. Beyond this EF_{th}, the domain sizes reduce with a larger presence of domain boundaries. AFM topography and phase studies reveal the evolution of P(VDF-TrFE) surface under bias (**Figure: 2.6**).

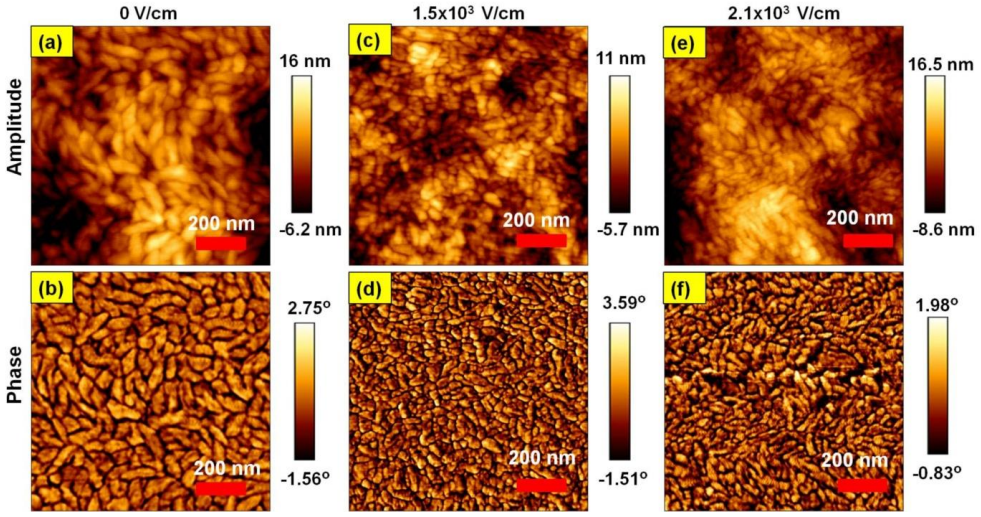

Figure 4.5: *AFM topography and phase of P(VDF-TrFE) surfaces EF treated at various voltages, 0 V/cm (a) & (b) 1.5×10^3 V/cm (c) & (d) and 2.1×10^3 V/cm (e) & (f). The scale is indicated in the images.*

A change from a low to high surface roughness is evident from the AFM height images given in **Figure: 4.5b** and the change in surface roughness with the applied EF are also shown in the **Figure: 4.6**. For very high applied field ($\geq 2.75\times10^3$ V/cm), the

film tends to form a lower fraction of crystallites and domains with a noticeable presence of ruptures which evolve on the dielectric surface (see **Figure: 4.10b**). Phase images of the P(VDF-TrFE) surface show distinct phases with sizable domain boundaries for large bias exposure films (see **Figure: 4.5b, 4.5d** & **4.5f**).

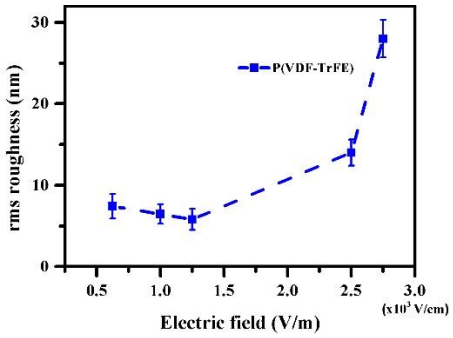

Figure 4.6: *Dependence of the surface roughness of the P(VDF-TrFE) films on EF.*

The P(VDF-TrFE) films studied using high-resolution PFM techniques reveal and track the structural variation with EF. Vertical PFM amplitude (VPFM-a) is a measure of the amplitude of out-of-plane (upward and downward polarization, w.r.t. the substrate) piezoelectricity in the vicinity of the surface.[9] VPFM images of EF treated P(VDF-TrFE) samples are given in the **Figure: 4.7**.

VPFM-a shown in **Figure: 4.7** reveals the local piezo response from the sample. Analysis of the images reveals an increase in amplitude and aggregation of out of plane piezo domains compared to the control sample which corroborate well with P-E measurements from the similar set of samples as shown in the **Figure: 4.3**. VPFM-phase (VPFM-p) measured along with VPFM-a gives detailed information about the orientation of in-plane polarization. The surface roughness also decreases from 7.42 nm to 5.8 nm indicating lower surface trap density. The reduced roughness along with the uniformly ordered in-plane arrangement of the dipoles then promotes an ordered growth

of the deposited semiconducting polymer layer.[10] It is noted that application of EF (> 1.5×10^3 V/cm) reverses this trend and increase the surface roughness to a range of ~ 28 nm as shown in **Figure: 4.6**.

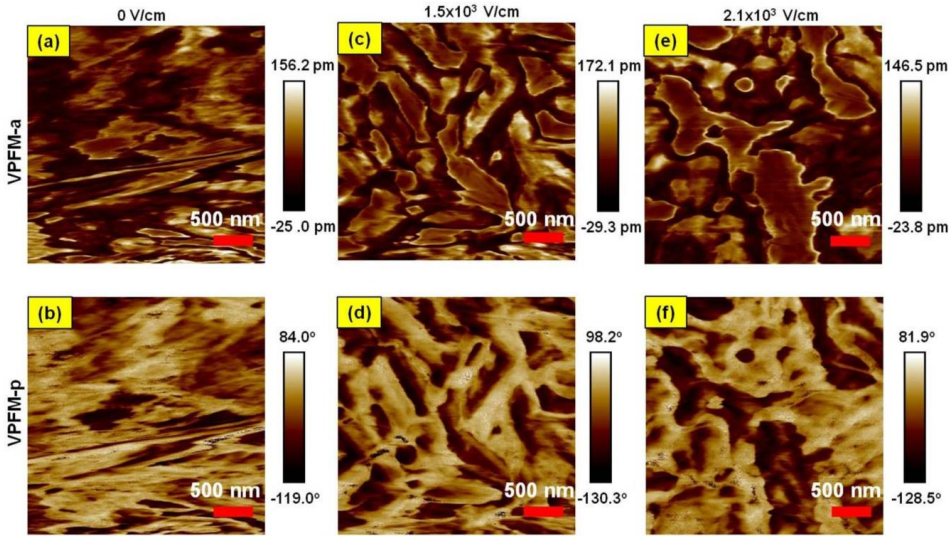

Figure 4.7: *Vertical–PFM (VPFM) images of poled P(VDF-TrFE) film. Top row represents vertical piezo response amplitude (VPFM-a), and lower row represents the VPFM phase (VPFM-p). Applied EF is represented on top of each set of measurements.*

4.7 Polarization Anisotropy Characterization

Optical polarization anisotropy measurements were performed on ultra-thin PBTOR films deposited on top of poled and nonpoled P(VDF-TrFE) samples. A **l**aser of wavelength 532 nm was used as the light source. PolarSpeed-M(L)-AR liquid crystal from LC-Tech advanced liquid crystal whose polarization axis can be precisely rotated using applied voltage along with LCC-230 controller was used for varying the polarization axis of the incident light. The transmitted light passing through the sample was analyzed by rotating the polarization axis of the liquid crystal. Measures were taken to ensure the sample is centered with respect to the rest of the optical components in the

setup. **Figure: 4.8a** shows the schematic of the experimental setup. The polarization axis of LC is rotated continuously at a given rate while maintaining a static P(VDF-TRFE)|PBTOR position and the signal is digitally monitored.

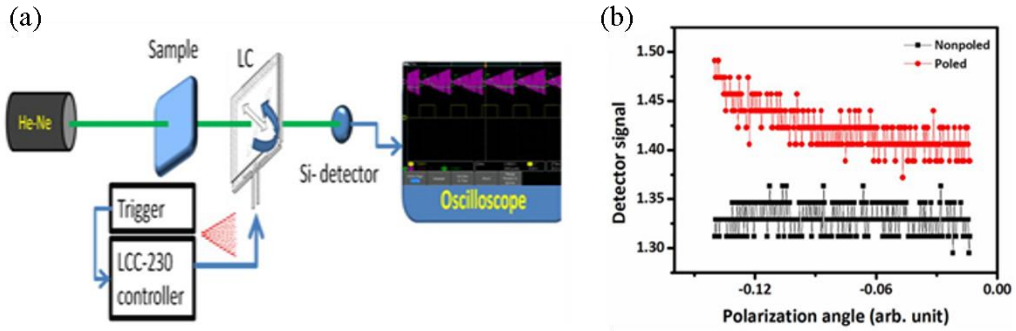

Figure 4.8: *(a) Schematic of optical polarization anisotropy measurement. (b) Anisotropy of the transmitted polarized light through the poled and nonpoled P(VDF-TrFE)|PBTOR film. (Signals were shifted vertically for convenience of representation).*

Ordered lamellar packing was observed in PBTOR, due to large degree of planarity of the monomer and secondary factors arising from S(thiol)-O(alkoxy) interactions originating from intramolecular interaction.[11] The observed further enhancement factor of μ_{FET} in EF treated devices is attributed to an improved orientation of PBTOR on PVDT-TrFE template and consequently lower scattering of charges at domain interfaces. We speculate that these surface microstructure features on the dielectric do translate to a higher degree of order and orientation of the deposited polymer semiconductor film.[12] This transfer of order from the substrate to the semiconductor layer is a subtle effect and shows up readily in optical anisotropy measurements as shown in the **Figure: 4.8b**.

The measurements also indicate that the EF effect persists during the PBTOR deposition procedure and does not relax upon removal of EF. This feature is consistent

with PFM imaging and retention of the enhanced OFET mobility for an extended duration. It was noted that the control samples of P(VDF-TrFE) films do not exhibit transmission-anisotropy (**Figure: 4.8b**).

4.8 Electrical Analysis

Anisotropy in lateral charge transport was also monitored using Current-Voltage (IV) curve in various sets of P(VDF-TrFE)|PBTOR interface and is shown in the **Figure: 4.9**. Micro channels of length ~ 20 microns were created using shadow mask, and gold electrodes were deposited on the PBTOR film as shown in the **Figure: 4.9a** for the measurement. IV measurements were performed in parallel and perpendicular directions of applied EF. A Clear trend of anisotropic transport is seen in the IV measurements.

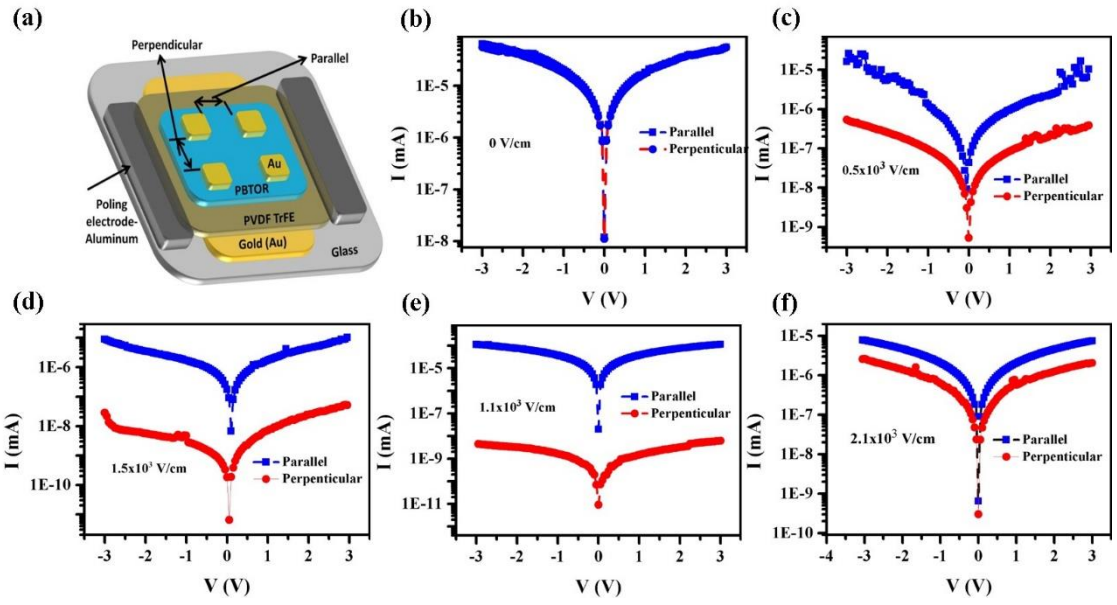

Figure 4.9: *Typical anisotropy of current density (blue curve) parallel and perpendicular (red curve) w.r.t the applied EF direction on a PBTOR thin film coated on EF treated P(VDF-TrFE) substrate. Figure (b) represents the control sample.*

Reliable FET characteristics were obtained from measurements on a large number of PBTOR and P3HT based devices (**Figure: 4.10a** and inset respectively). A systematic trend was obtained from the devices as a function of the EF treated dielectric surface. It was observed that for both the semiconducting polymer based FETs, μ_{FET} increased with the electric field (EF) treatment. The magnitude of increase with the EF observed over many batches of devices cannot be accounted by statistical variations inherent in these OFETs. For devices with the dielectric treated with low and intermediate EF range ($< 10^3$ V/cm) the increase in μ_{FET} is linear, and for higher EF range μFET saturates and exhibits a mild reversing trend. This response of $\mu_{FET}(E)$ provides a window to control and optimize the performance parameters. For the PBTOR based FETs, $\mu_{FET}(E)$ increases from 0.03 $cm^2/(Vs)$ to 0.13 $cm^2/(Vs)$. Similar trends were obtained for P3HT based FETs with an enhancement factor of ~300% as shown in **Figure: 4.10a** inset. In both the cases, on-off ratio was not significantly altered. The threshold voltage of PBTOR FETs followed the mobility trend. Improved mobility values are reflected in lower threshold values for this range of EF. There was no indication of a discernible thickness change with the electric field treatment procedure in P(VDF-TrFE) films.

Earlier studies on P3HT based FETs on ferroelectric layers have revealed the presence and influence of polarization fluctuations on the interfacial charge transport.[13] Randomly oriented ferroelectric microcrystals at the interface are shown to affect the charge carrier transport. The introduction of the external electric field applied during the annealing process in the present case has a clear beneficial feature which manifests as larger degree of orientation and ordering and consequently reduced scattering losses.

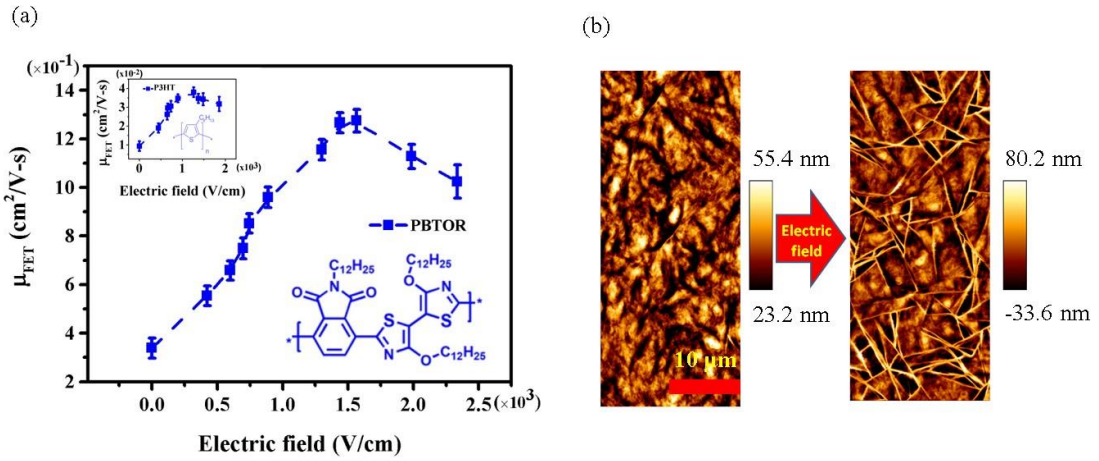

Figure 4.10: *(a) Field effect mobility μ_{FET} as a function of EF applied to the dielectric surface in a PBTOR FET (inset shows the trend of μ_{FET} of P3HT FET). (b)AFM topography of P(VDF-TrFE) surface at 0 V/cm and 2.75×10^3 V/cm are shown in the figure.*

The observation of reversal of the EF-induced trend at higher EF strengths, which manifests as a lowering of μ_{FET} beyond a threshold range can also be understood from the microstructure patterns. It should be noted that a negative piezo electric response of P(VDF-TrFE) observed at the higher electric field has been attributed to lowering of crystalline dimensions.[14] Large EFs result in a higher density of surface deformations as evident in the AFM topography of the surface as shown in **Figure: 4.10b**. The strain-induced needle-like structures evolving at higher EF as observed in **Figure: 4.10b** are shown to be detrimental to the device performance, as shown in the leakage behavior (I_g) (**Figure: 4.11**).

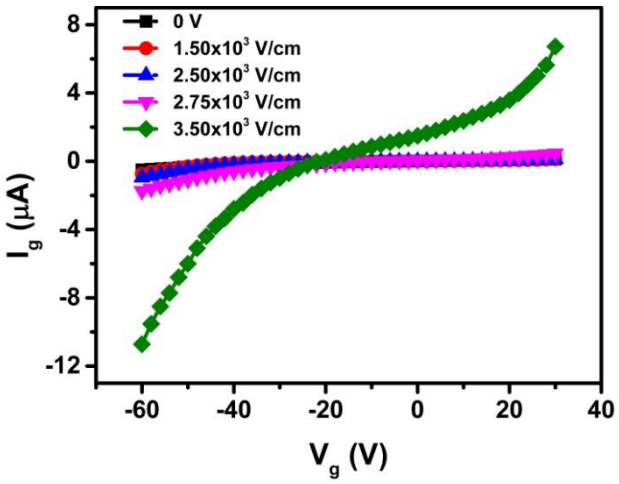

Figure 4.11: *Leakage current dependence on the applied EF in the OFET devices.*

Lateral-PFM (LPFM) measurements (**Figure: 4.12**) on the dielectric reveal information about the amplitude and direction of in-plane piezo amplitude and domains which are arranged parallel to the substrate. Scans were performed while keeping the cantilever axis perpendicular to the EF direction, to achieve maximum torque on the cantilever. LPFM showed an increased presence of in-plane piezoelectric character having the same phase at intermediate EF (**Figure: 4.12d**) compared to non EF treated and high EF treated film surfaces. We can then attribute the lower mobility from high EF treated devices to the combination of these factors: (i) EF induced rupture of crystalline segments in P(VDF-TrFE) films as shown in the **Figure:4.10b** and (ii) increase in anisotropy in the in-plane ferroelectric domains at higher field densities. This feature also puts a limit on the EF magnitude applied during device fabrication. The semi-crystalline semiconducting system needs to be designed such that it can optimally utilize the anisotropic cue offered by the surface to develop into an ordered assembly at the interface.

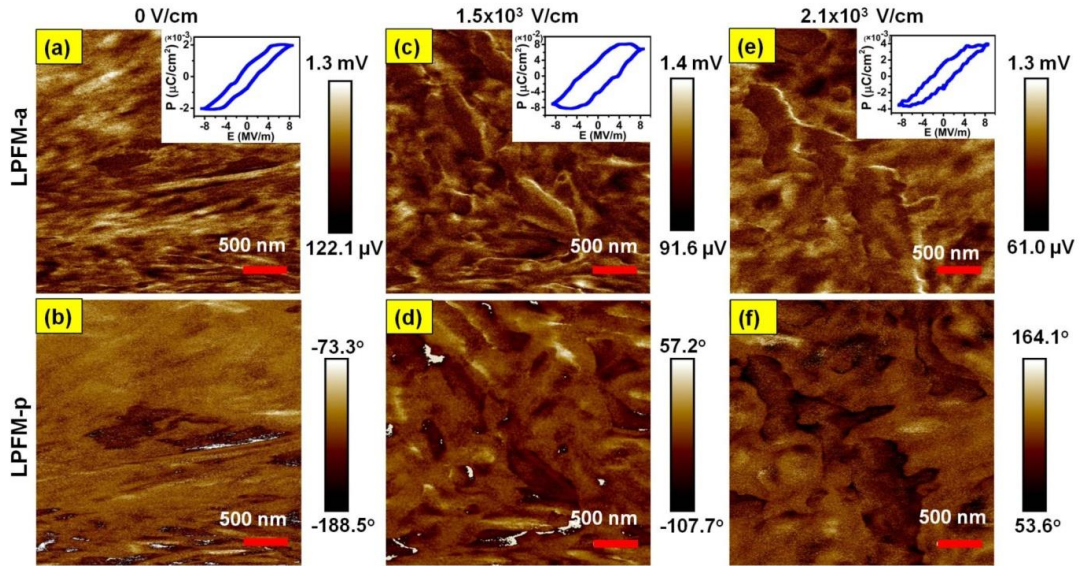

Figure 4.12: *Lateral-PFM (LPFM) measurement of EF treated PVDF-TrFE samples (3×3 micron size). The top row of images shows the amplitude (LPFM-a) and lower row shows the phase (LPFM-p). Inset in the top row shows the P-E curve of corresponding samples.*

It is to be noted that an analogous situation arises when the semiconducting interface are formed under mechanical shear conditions. Higher μ_{FET} has been observed as a result of the increased strain in the film which enhances the orbital overlap between adjacent molecules.[15] These soft-template approaches are particularly relevant in organic electronics as the charge transport is largely dominated by hopping mechanism unlike the band transport in inorganic crystals.[16] Any improvement in the degree of order translates to a reduced density of interfacial traps and improved energetics for carrier transport.

4.9 Summary

The ability to tune the charge transport behavior at the transport interface in the OFET device using external applied EF across the ferroelectric surface during the

fabrication process is demonstrated in this chapter. The carrier mobility μ_{FET} of the EF treated devices increases several folds (up to 300%) compared to that of untreated devices. Atomic force microscopy (AFM) and piezoresponse force microscopy reveal the evolution of the microstructure and polarization response as a function of the field. The observation of improved crystallite/polarization features clearly correlates with the higher μ_{FET} of the devices.

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Chapter 5

HOIP based MSM Devices: Electrical Transport and Photocurrent Microscopy Studies

5.1 Introduction

Any semiconducting device consist of multiple interfaces which determine the final performance and stability.[1, 2] The interfaces charge transport analysis in HOIP devices departs from that of conventional semiconductor interfaces due to the presence of mobile ions in the bulk as well as at the surface in a working device. Moreover, the ionization potential of the HOIP material is known to vary on a large scale depending upon the method of preparation and stoichiometry of precursors involved.[3] This chapter addresses the current-voltage characteristics of HOIP lateral Metal-Semiconductor-Metal (MSM) devices with symmetric and asymmetric electrodes, where electrodes are deposited on a substrate in a coplanar configuration. High-resolution photocurrent measurement was used to understand the local photogeneration profile at the HOIP-metal interfaces and inside the channel.

Most of the photo-conductive devices are usually fabricated in a sandwich configuration where the active layers are stacked between counter electrodes. This configuration requires a transparent electrode for optoelectronic applications. In contrast, this chapter describes a lateral MSM structure, which removes the complexity of device preparation and permits direct access to the active layer for spatially resolved

measurements. The device architecture can be tailored accordingly in the fabrication of optoelectronic devices such as back contact solar cells. This configuration opens up the possibility to use more combinations of electrodes compared to sandwich structure. The distance between electrodes (channel length, *L*) can be varied from few µm to 100's of µm range allowing to directly probe microscopic aspects of charge transport in the channel region. Lower capacitance offered by this geometry can reduce the electronic noise.[4] Higher compatibility of this architecture with field effect transistor technology provide easy integration with the driving circuits for a flexible platform.

In this chapter studies of standard Metal-Semiconductor-Metal device structure are presented. Issues related to interfacial barriers, surface and bulk contributions are examined by conventional I-V measurements as well as scanning photocurrent microscopy (SPCM) techniques.

5.2 Device Fabrication

MSM devices were fabricated on RCA cleaned glass substrate. 40 wt.% $MAPbI_3$ solution was spin coated on the substrate at 3000 rpm for 80 seconds followed by an additive (TPBi) mixed with anti-solvent ($CHCl_3$) treatment. The perovskite films were annealed at 100 ^{0}C for 60 min under N_2 atmosphere. Laterally separated electrodes were fabricated by thermal evaporation using shadow mask on the $MAPbI_3$ film. Combination of metals of different work function was used as electrodes in the fabrication of symmetric (Al/$MAPbI_3$/Al, Au/$MAPbI_3$/Au) and asymmetric (Al/$MAPbI_3$/Au) MSM devices. UV/VIS absorption spectroscopy (**Figure: 5.1a**) and XRD (**Figure: 5.1b**) measurements were carried out to ensure the high material purity of HOIP film.

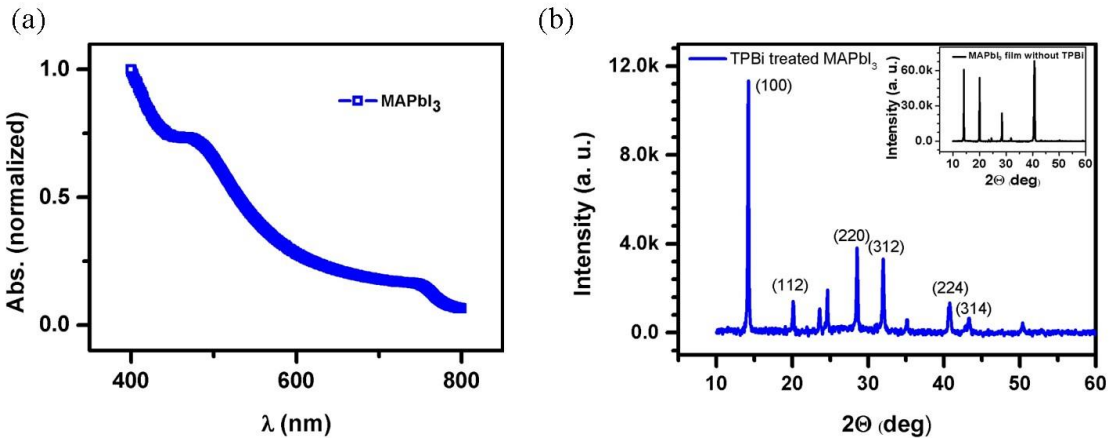

Figure 5.1: *(a) UV/VIS absorption spectrum of $MAPbI_3$. (b) X-ray diffraction spectrum of annealed-$MAPbI_3$ film (inset shows the XRD pattern of $MAPbI_3$ film without TPBi treatment).*

5.3 Effect of Additive-Antisolvent treatment: Surface Roughness

As a primary requirement for efficient devices, the grain size distribution of HOIP films were studied using atomic force microscopy (AFM) measurements, in contact mode using JPK Nanowizard 3 AFM with Cr/Pt coated AFM cantilever having a nominal force constant 0.2 N/m and resonance frequency 13 kHz. AFM microscopy established the improvement of surface morphology and corresponding reduction in average roughness and grain size upon the TPBi additive- anti-solvent treatment of $MAPbI_3$ films. **Figure: 5.2(c) & (d)** and **Figure: 5.2(e) & (f)** shows AFM topography and roughness measurements of $MAPbI_3$ films with and without TPBi treatment. Bright filed images of TPBi treated $MAPBI_3$ film as shown in the **Figure: 5.2(b)** also reveals a smoother microstructure compared to untreated $MAPbI_3$ film shown in **Figure: 5.2(a).**

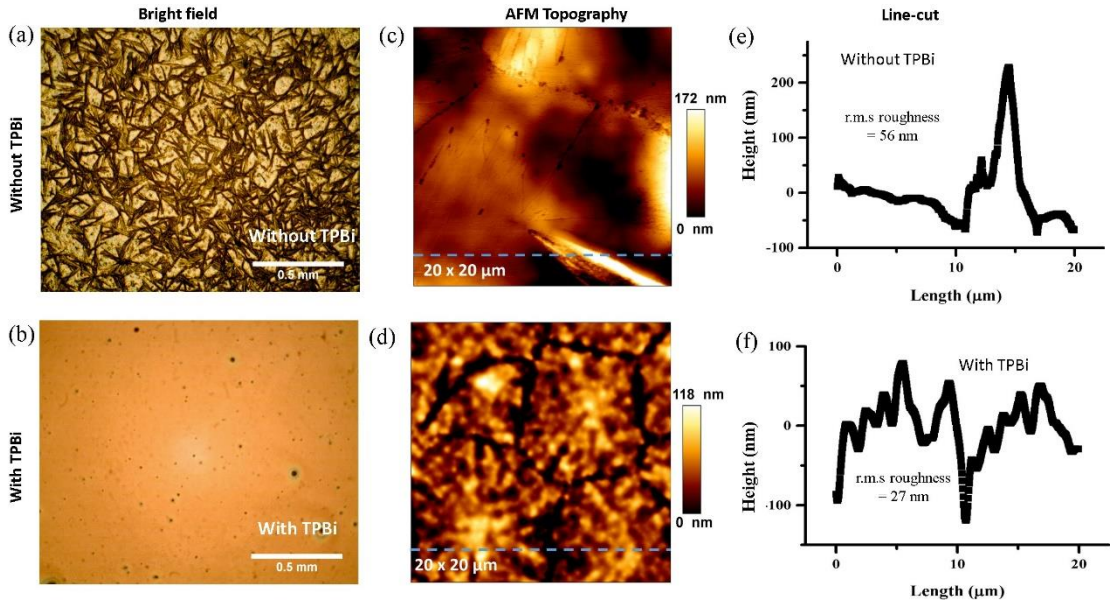

Figure 5.2: *Bright field images of $MAPbI_3$ films (a) without TPBi and (b) with TPBi. AFM images (20µm x 20µm) of $MAPBI_3$ films (c) without TPBi and (d) with TPBi treatment. Figures (e) & (f) shows the line scans indicated by blue dashed lines in (c) & (d) respectively.*

The objective of the additive mediated anti-solvent treatment was the reduction of the grain size of perovskite crystals by inducing multiple seeding points, to achieve uniform, pinhole-free perovskite thin films.[5, 6] The grain size reduction was achieved by fast removal of good solvent (DMSO) from the film using an orthogonal solvent ($CHCl_3$), which results in rapid crystallization and reduced grain size.

5.4 I-V Characteristics Under Dark and Light Conditions

Current-voltage characteristics of the devices were studied using Keithley SCS 4200. Measurements were performed in vacuum sealed chamber with electrical contacts, while maintaining 10^{-3} mbar pressure. Light I-V measurements were carried

out under broad illumination of the channel area using a 532nm CW laser with 1.2 mW/cm^2 power density. The light was illuminated from the HOIP side of the device.

Current-voltage measurements of devices with both symmetric (Al/$MAPbI_3$/Al and Au/ $MAPbI_3$/Au) and asymmetric (Al/ $MAPbI_3$/Au) electrode combinations were performed under dark and light conditions to understand the charge transport in lateral Metal-HOIP-Metal devices. Measurements were carried out on devices with a channel length (L) ranging from ~ 15 µm to 70 µm. Dark current and photocurrent measurement under broad illumination of these devices are summarized in **Figure: 5.3**. The Arrow represents the direction of voltage sweep.

Devices with both symmetric and asymmetric electrode combination exhibit Schottky characteristics as observed in the I-V profile. I-V characteristics of dark and light condition show symmetric behavior as observed in I-V profile in the symmetric electrode (Al/$MAPbI_3$/Al and Au/$MAPbI_3$/Au) devices for the various channel length studied. However, it can be observed that the effective photocurrents in the symmetric electrode devices reduces as the channel length increases, as expected from the increase in the resistance. Symmetric, nonlinear current response of the form $J \sim J_0 e^{(-\frac{eV}{kT})}$ indicates the presence of metal-semiconductor Schottky barrier. However, symmetric electrodes favor single carrier transport.

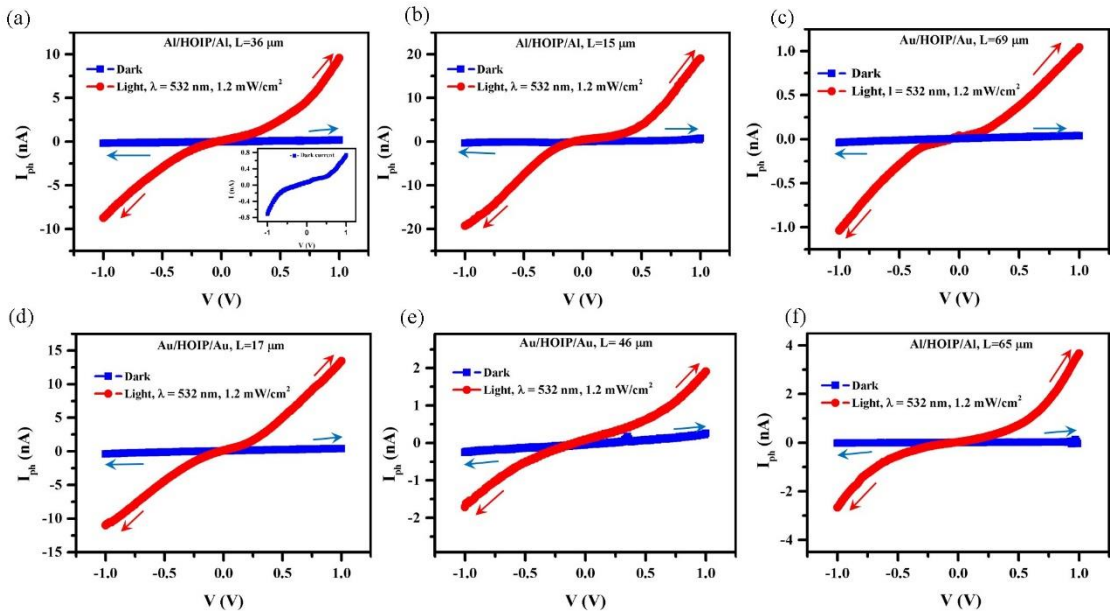

Figure 5.3: *Channel length the dependence on I-V characteristics of HOIP MSM devices with symmetric electrode devices (a) & (b) (Al/ $MAPbI_3$/Al) and (c) & (d) Au/ $MAPbI_3$/Au. (b)& (d) represent short channel and (a), (c), (f) & (d) represent long channel devices. I-V measurements were commenced from zero volts and the direction of scans are mentioned in the figure.*

A noticeable deviation from I-V behavior was observed in the asymmetric electrode (Al/$MAPbI_3$/Au) devices under broad uniform illumination. A trend is observed in the I-V response as a function of channel length (*L)* as shown in the **Figure: 5.4**. At short channel length (L ~ 15 μm) range, the metal-semiconductor interface in Al/$MAPbI_3$/Au facilitates both electron extraction at Al/$MAPbI_3$ junction and hole extraction at Au/$MAPbI_3$ junction. Consequently, high forward bias current and small reverse bias current is observed with a rectification ratio η ~ 28%. For the short channel length, the space-charge region extends to most of the device. Essentially, the Al/ $MAPbI_3$/Au can be modeled as two carrier transport similar to diode.

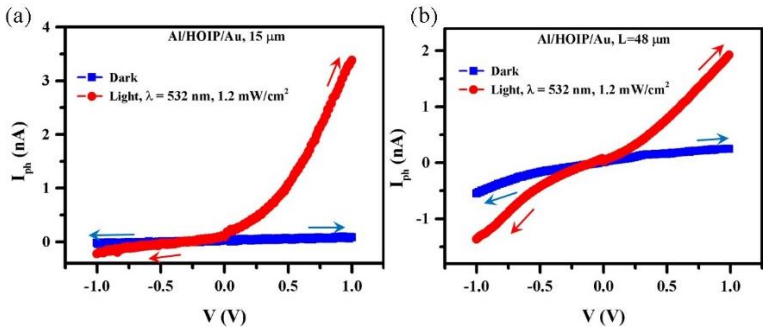

Figure 5.4: *Typical current-voltage characteristics of asymmetric electrode (Al/MAPbI$_3$/Au) MSM devices at (a) short (L~15 μm) and (b) long (L~50 μm) channel lengths.*

The same configuration in case of a longer channel length (*L*~48 μm) as in **Figure: 5.4b** has higher fraction of reverse bias current as can be seen in the asymmetric I-V curve. The space-charge region in this case is largely localized around the metal-semiconductor junction and doesn't extend deep into the channel region. Hence beyond a certain threshold potential, photocarriers generated in the bulk of the device are extracted by respective electrodes. Due to the increased length of the active HOIP area for photogeneration of carriers, the effects of space-charge region is not dominant in the I-V curve.

5.5 Photogeneration and Lateral Charge Transport Analysis

The analysis of MSM devices can be carried out using a combination of photovoltaic and charge transport physics. The electrical transport under illumination in these systems can be interpreted in terms of different models based on ambipolar drift-diffusion models modified by trap and recombination kinetics.[7] Models based on space charge limited photocurrent have also been used for organic MSM structures.[8, 9] The utility of lateral structures as back-contact solar cells and efficient photodetectors

generally require balanced transport, sizable charge carrier generation (*G*). In case of blocking contacts with sizable barrier in organic MSM structures, the extracted photocurrent has higher contribution from the depletion region associated with the metal semiconductor Schottky barrier. Having channel length comparable to the barrier width allows for dominant space charge region in most of the device. This implies that the mean electron and hole drift lengths $w_{e(h)} = \mu_{e(h)}\tau_{e(h)}E$ are equal to or longer than the channel length *L*: where $\mu_{e(h)}$is the charge carrier mobility of electrons (holes), $\tau_{e(h)}$ is the charge carrier lifetime, and *E* the electric field. Assuming absence of recombination (*R*=0) in the semiconductor, the photocurrent density (J_{ph}) can be given as

$$J_{ph} = qGL \qquad \ldots\ldots (5.1)$$

where q is the electronic charge and G is the photo-induced carrier generation rate of electrons and holes. However, if $w_e < L$ or $w_h < L$ or both of them less than L, space charge region in the channel become less dominant and the recombination of free charge carriers in the bulk becomes significant.

This is shown schematically in **Figure: 5.5** below in the region L_1.

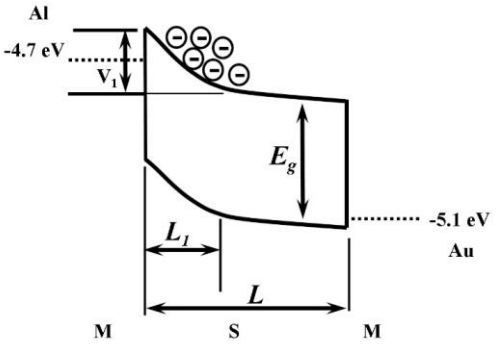

Figure 5.5: *Schematic of energy diagram in lateral MSM structure with asymmetric electrodes.*

The length of the space charge region L_1 is given by the mean electron drift length and limits the saturated photocurrent to

$$J_{ph}^{sat} = qGL_1 \quad \text{..... (5.2)}$$

The limits on the extraction of photogenerated electrons and holes from a semiconductor can be estimated by the plot provided by Goodman and Rose.[10] The fundamental limit for the buildup of space charge is reached when the saturation photocurrent is equal to the space charge limited current. Space charge current is expressed as,

$$J_{SCL} = \frac{9}{8}\varepsilon_0\varepsilon_r\mu_h\frac{V_1^2}{L_1^3} \quad \text{..... (5.3)}$$

But in the $MAPbI_3$ system discussed earlier, photocurrent doesn't follow a V^2 dependence as mandated by the space charge limited formalism (**Figure: 5.6)**. Carrier generation and transport are known to be efficient in these crystalline systems. However the understanding of the nature of contact and the barriers at the interface are not well understood here. It is expected that the transport is not limited by bulk processes, especially since the channel lengths are sufficiently wide, with bias voltages on the lower side (low EF region).

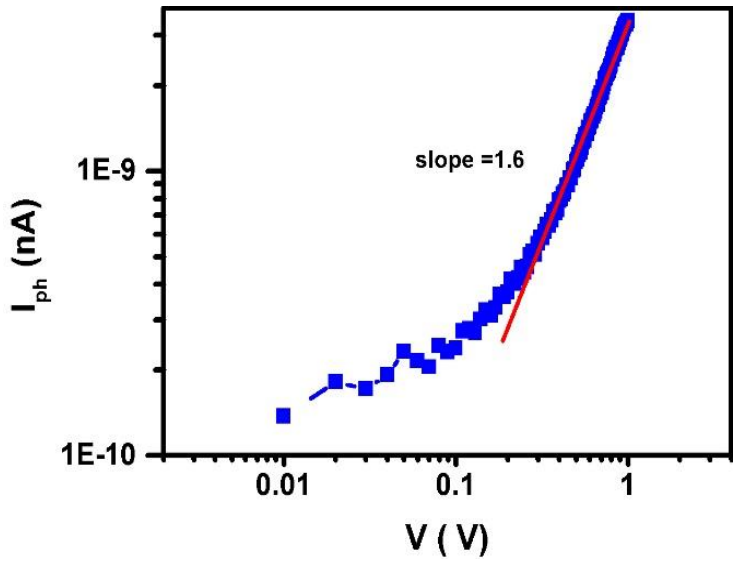

Figure 5.6: *I-V graph of Al/MAPbI3/Au device having channel length, L ~ 15 µm.*

5.6 Surface Potentiometry of MSM Device

KPFM measurement was performed on HOIP film based lateral devices to analyze the in-situ potential distribution on the surface of the MSM device with and without external bias. Results of a KPFM measurement on the device with channel length ~ 50µm is shown in **Figure: 5.7**. Au electrode was grounded during the measurement.

The results show a higher potential near positively biased Al electrode in the MSM device. The magnitude of the potential increases with increase in the applied bias. This higher potential at the Al-HOIP interface is a manifestation of SCR present in the device. These observations are in excellent agreement with the above model explaining charge accumulation at one of the interfaces. A small difference in the absolute surface potential is visible on the device without any applied bias.

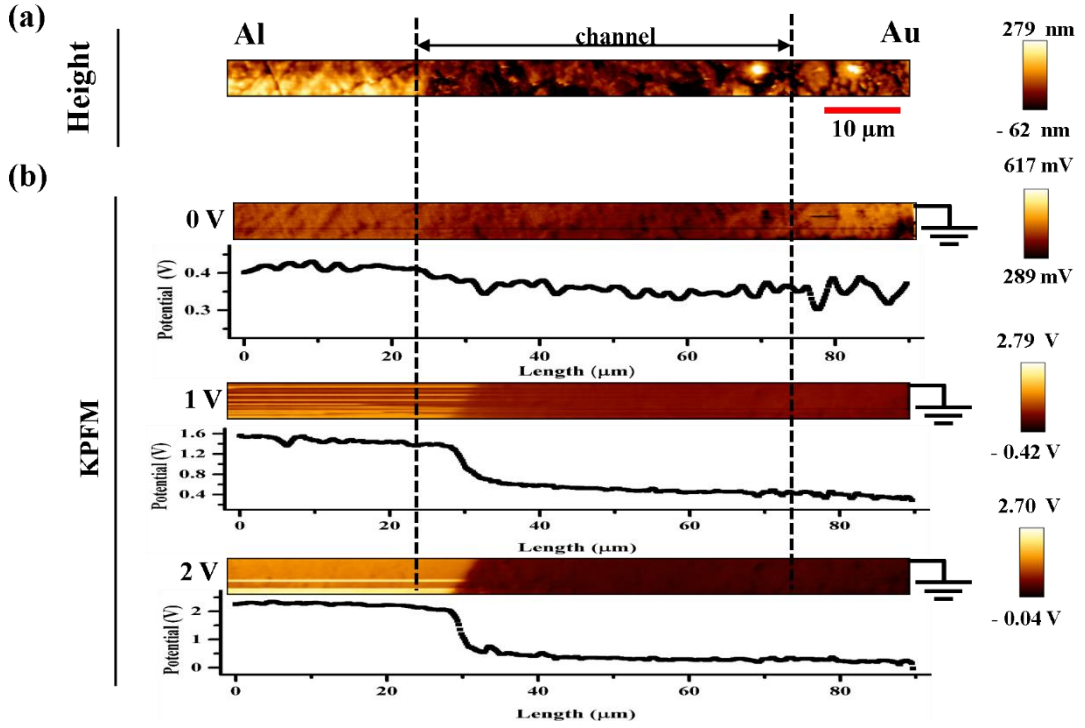

Figure 5.7: *(a) Topography of the MSM channel area (b) Surface potential distribution measured by KPFM in the MSM channel area.*

5.7 Scanning Photocurrent Microscopy of MSM Device

The electric field mapping and the choice of appropriate models can be arrived by 1-D photocurrent scan. This technique relies on near-field scanning optical microscopy (NSOM). A tapered optical fiber with aperture $\phi \approx 105$ nm kept in the near filed regime ($d < \lambda$) was used as the illumination source in the measurement. Light from a CW diode laser ($\lambda = 532$ nm and power = 5 mW) was coupled to the optical fiber using a 20x, 0.40 NA microscope objective lens. Intensity of the laser light was modulated at $f = 83$ Hz using an optical chopper. The optical fiber connected to the piezo head of atomic force microscope (AFM) was raster scanned on the surface of MSM device to obtain a two-dimensional map of the photocurrent in the device. Light was illuminated from the HOIP film side of the device. Devices were scanned starting from one electrode

through the channel till the second electrode. The scan creates a map of the photogenerated carrier collection as a function of the location of carrier generation. A PMT kept below the MSM device was used to collect the transmitted light. It was later correlated with the spatial photocurrent map to determine the electrode edges. **Figure 2.12** depicts the schematic of the experimental setup. The extracted photocurrent from the device is measured via lock-in detection using amplifier SR830. The signal was further amplified and coupled back to the AFM controller for display and analysis. This technique has been used in earlier studies such as understandng of the spatial profile of photocurrent geneartion in nanowires and its relationship with the doping concentration.[9, 11-14] The geometrical confinement of the light using aperture and near-field operation practically removes the need for deconvolution of the contribution from the light beam spot size and scattering phenomena.

Figure: 5.8a shows a typical SPCM image of a ~ 40 μm asymmetric device using near-field scanning optical microscopy. A typical photocurrent line scan taken from the SPCM image of an asymmetric electrode device under forward bias (Al is positively biased) is shown in **Figure: 5.8b**. Spatial mapping of the signal from devices under zero bias didn't exhibit any signature of position dependent photocurrent. A highly localized photo current generation was observed when a positive voltage is applied to the Al electrode of the device. SPCM map of the channel consists of two distinct regions. The first region at the Al-HOIP interface has a dominant photocurrent peak starting from the electrode area (Al) and increases towards the channel. The photocurrent signal further rapidly decreases towards the center of the channel. A second region is also seen in the channel where the photocurrent is negligible, and it extends towards the Au electrode. There is no appreciable photocurrent generation near

the negatively biased Au electrode. The amplitude of the peak marginally increases with applied bias.

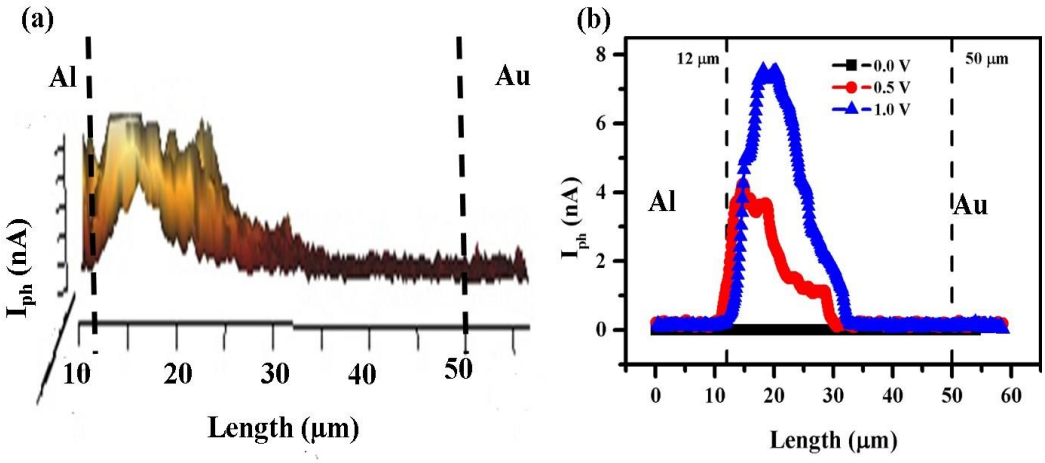

Figure 5.8: *(a) A typical SPCM map of MSM device (b) A typical line scan obtained from the SPCM map of an Al/HOIP/Au device with channel length, L~40 µm, under different bias conditions.*

The line scans shown in **Figure: 5.8** indicates that the photogeneration in the channel is highly non-uniform and voltage dependent. The strong band bending upon forward bias at Al-HOIP space charge interface assist photogenerated charges to separate more compared to the other regions of the channel.

Carrier extraction at the interface is fast in the absence of a barrier. However, as mentioned in the above case, accumulation of electrons at the metal-semiconductor interface facilitates slow carrier extraction. In the slow extraction limit, in a lateral MSM system, the current profile inside the channel can be calculated as,[7]

$$I = I_0 \exp(-\frac{x}{L_d}) \qquad \ldots\ldots (5.11)$$

where *x* is the distance from the electrode edge. The photocurrent thus decays exponentially in the channel with a decay constant L_d, the diffusion length. Fitting of the decay profile to an exponentially decaying function gives the decay length of electrons. Thus the electron diffusion length in this case can be estimated using equation (5.10) to be L_d^e ~ 3-4 μm. Such long carrier diffusion length in attributed to highly oriented growth of the perovskite film on the substrate.[11, 15, 16] Dominant (110) plane observed in the XRD spectrum of $MAPbI_3$ film (**Figure: 5.1b**) corroborate with higher diffusion length in this system.

5.8 Summary

Spatial profile of the photocurrent generation in the HOIP MSM structure is carried out using SPCM which enables direct estimation of carrier decay length. Decay length, L_d^e ~ 3-4 μm was estimated from spatial profile of the photocurrent inside the channel. Charge generation and transport in these system were analyzed using drift-diffusion formalism. Charge transport shows asymmetric I-V behavior when the transport length is comparable to the SCR length scale in MSM structures with electrodes having different work function.

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Chapter 6

Hybrid Perovskite Based Position Sensitive Detectors

6.1 Introduction

Hybrid organic inorganic perovskite (HOIP) is a crystalline system with an estimated charge carrier mobility of $\mu > 10^1$ $cm^2/(Vs)$ compared to a mobility of $\mu \sim 10^{-3}$ $cm^2/(Vs)$ observed in disordered semiconducting polymer system such as P3HT.[1, 2] Wide absorption range,[3] high absorption coefficient and compatibility with scalable processing methods makes HOIP as a promising material for variety of optoelectronic applications.[4-6] In HOIP solar cells the higher quantum yield and higher diffusion length can be attributed to lower trap density and monomolecular recombination rates for charge carriers.[7-9] These novel properties of HOIP are put to use in the development of position sensitive detectors (PSD) in this chapter.

Optical PSDs are class of photodiodes (PD) which can measure the position of the centroid of the light spot projected on their surface and the detection can be either in 1-D or 2-D.[10] PSDs are used in a variety of measurements such as position, angle, distortion, vibration and lens refraction/reflection. They can be made in monolithic form or arrays of discrete element detectors such as charge coupled devices (CCD). Unlike discrete element detectors, monolithic PSDs provide continuous position information with a high speed of response and excellent position resolution.[11] Simultaneous detection of intensity and the position of the centroid of a light spot, simplicity of manufacturing, high resolution, wide dynamic range, small supporting

electronics and higher stability and reliability are the features of PSDs. A detailed description of the principle of operation and the performance of monolithic PSDs made of HOIP materials as the active layer are discussed in this chapter.

6.2 PSD, Principle and Operation

Working principle of PSD can be described using the concept of lateral photo effect proposed by Schottky during 1930s, which later has been gradually implemented for many combinations of semiconductors and semiconductor-metal junctions.[12-15] Lateral photo effect phenomena can be explained using a p-n junction under a non-uniform light illumination, as first described by J. T Wallmark on a-Si.[13]

A p-n junction interface doesn't permit current flow under equilibrium condition due to the built-in potential barrier. But a global illumination at the interface from one side of p-n junction can generate photo carriers at the junction. These photogenerated carriers can migrate under the influence of built-in voltage, resulting in a transverse photovoltage (V_{oc}). However, the light illumination is non-uniform, then a photovoltage can be detected at contacts placed across the base, parallel to the plane of the p-n junction, and this voltage manifests as lateral photovoltage (LPV). LPV can be understood by considering a p^+n junction as shown in **Figure: 6.1** with one side more heavily doped compared to the other side hence making it more conducting. Under non-uniform illumination at the p^+n junction, *e-h* pair will be generated in both the layers. Minority charges on each side move across the p^+n junction at the point of illumination. The high conductance in p^+ layer helps the additional holes to redistribute rapidly over the entire surface to establish an equipotential surface over the p^+ surface compared to the added electrons in n layer. This will establish a non-equilibrium condition all along p^+n interface, except at the point of illumination and hence result in the reinjection of

excess holes back to n layer through the dark region of the interface. The slow-moving excess photogenerated electrons in n layer now move to recombine with the reinjected holes. This flow of electrons in n layer parallel to the p^+n interface creates an electric field and hence the LPV.

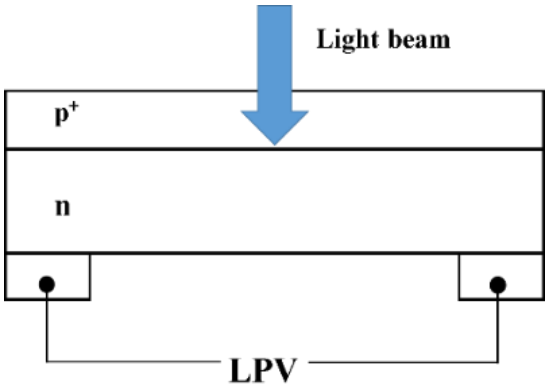

Figure 6.1: *A p^+n junction PSD in photovoltaic operation mode.*

However, if the junction is reverse biased, the reinjection is inhibited by the high potential barrier and the device can be used in photodiode mode. In this case, a current can be measured at the base contacts, and the current is linearly related to the location of the point of illumination due to the difference in the resistance offered by p^+ and n layers to holes and electrons respectively. Hence the non-uniform illumination will generate a linearly varying lateral photovoltage. While the above model has been described in terms of pn junction, it holds true for metal-semiconductor structures and p-i-n structures as well.

6.3 HOIP PSD

The above-mentioned concept of device is applicable to HOIP semiconductors as well. A 1-D PSD structure in this case consists of an epilayer of HOIP film on a common bottom electrode, and two top electrodes separated at a specific

distance (**Figure: 6.3**). These top electrodes maintain certain overlap with the common bottom electrode. Large area PSD with interelectrode distance (L > =3 mm) were fabricated using $MAPbI_3$ active layer. The step-by-step procedure of fabrication of PSD is given in detail in **section: 2.5.3.** Large area requirement mandates uniformity of the $MAPbI_3$ film over the channel area. Highly uniform $MAPbI_3$ films were fabricated using a TPBi-containing antisolvent-mediated single-step fabrication method.[16, 17] In addition to improved uniformity of the sample, additive treatment resulted in pinhole free film with reduced grain size. This procedure enabled formation of uniform films over an area of $1cm^2$. A thin planarizing electron accepting layer of N2200 polymer was spin-coated on the perovskite film, Two gold electrode depostited on top of the film forms the arms of the assembly. The schematic of the PSD is give in **Figure: 6.2.**

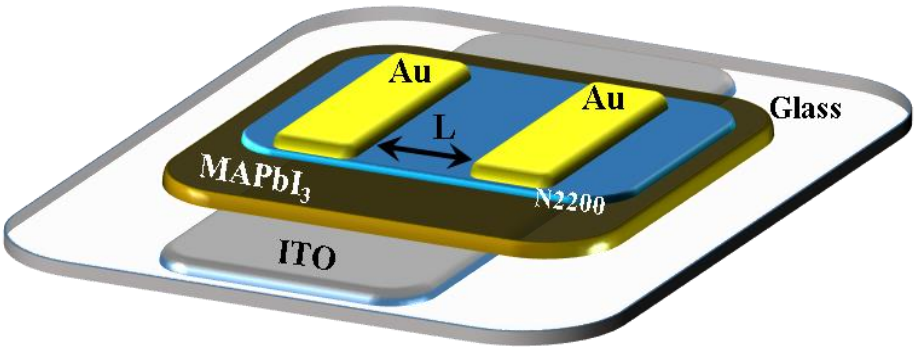

Figure 6.2: *Schematic of the HOIP position sensitive dectector.*

The quality of HOIP film was measured using UV-VIS absorption measurement and X-ray diffraction. UV/VIS and XRD spectroscopy resutls are given in **Figure: 6.3a** and **Figure: 6.3b** respectively. The TPBi additive in anti-solvent treatment during the process is shown to reduce the surface roughness of the $MAPbI_3$, as shown in the **Figure: 5.2**.

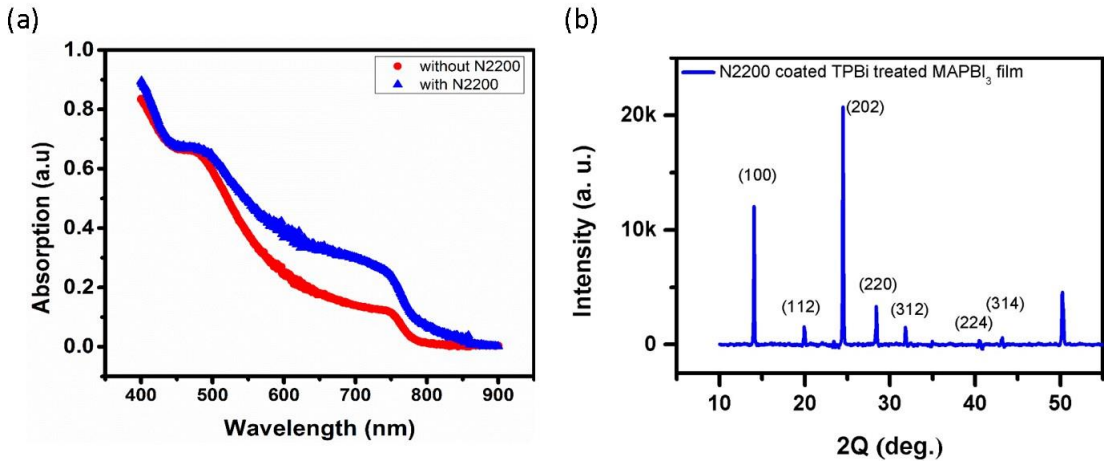

Figure 6.3: *(a) Absorption profiles of perovskite and perovskite-N2200 bilayer films. (b) XRD spectrum of the perovskite-N2200 bilayer.*

6.4 Lateral Photovoltage Measurement

A home built large-area high-resolution laser beam induced photocurrent (LBIC) scanning setup is used to measure differential photocurrent and photovoltage (**Figure: 2.8b**) in the sample.[18] The measurements were carried out in a sealed chamber with nitrogen environment to avoid degradation related issues. Chamber was flushed with ultrahigh pure N_2 gas before each measurement, and a steady N_2 pressure is maintained throughout the measurement to reduce the degradation effects. The control of the high precision micromanipulator sample stage housing the device, laser operation and the data acquisition were carried out using *LabVIEW* and custom-made microcontroller circuits. Lasers of wavelength 532 nm and 635 nm with a power of 683 µW and 5 mW respectively were used to scan the active area of the PSD. Laser beam spot diameter of ~ 10 µm was achieved using an objective lens of 50x magnification and 0.70 numerical aperture. Dual input Lock-in amplifier, SR830 from Stanford Research Systems was used to measure the differential photovoltage $\Delta V_{ph}(x) = |\Delta V_{ph1} - \Delta V_{ph2}|$ from two arms of the device. Each gold electrode with common ITO electrode is defined as an arm of

the device. Light beam is incident on the sample from the ITO side (bottom illumination) of the device as shown in **Figure: 6.4**. Transmitted light through the PSD channel was captured using a sensitive photodiode to overlay with the photoinduced $\Delta V_{ph}(x)$ scans to ascertain the light beam position.

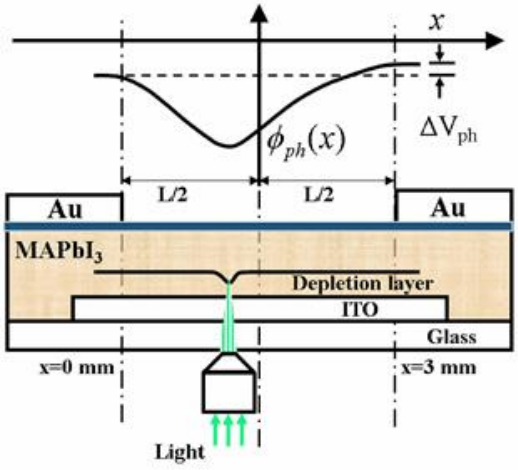

Figure 6.4: *Schematic of the PSD device and potential distribution as a result of non-uniform illumination in the active area of PSD.*

6.5 Photo-Generation and Charge Transport Analysis

The measurements were carried out on several devices (~ 10) with a high degree of reproducibility. The characteristics described below were observed for each device. Substantial short-circuit photocurrent (~ 10 µA) and photovoltage (~ 50 mV) were observed for the light incident (683 µW) with an illuminated area of the beam diameter of ~ 10 µm on the overlapping electrode regions of the two arms. As the light is displaced from the overlapping region ($x < 0$ and $x > 3$ mm) to the channel region, the differential photovoltage decreases. This decrease continues till the light position reaches the center of the channel, where a phase change is also observed (**Figure: 6.5a**). It is observed that two distinct types of variations are observed in the $\Delta V_{ph}(x)$ response

as the light position shifts away from the overlapping electrode regions (**Figure: 6.5a)**. This behavior is indicative of two spatial regimes in the transport mechanisms. The steep decay near the Au-contacts results from cumulative effects of contact resistance, diffusion of charge carriers and optical-scattering effects. We focus on the region x > 0.5 mm and x < 2.5 mm which are further away from the electrodes where a linear regime is available for a typical PSD operation. This length span encompassing the center region of the PSD covers a sizable fraction of the channel as shown in **Figure: 6.5b**. Spatial resolution of 2 μV/μm is obtained for PSD device structures with L ~ 3 mm. This magnitude of sensitivity is an order of magnitude higher than the analogous polymer based PSD structure, and the position resolution (~ few microns) without amplification is comparable to commercial PSDs (which includes external amplifiers).[19, 20] The spatial profiles are marginally altered for light illuminated from the Au side (**Figure: 6.5a** inset and **Figure: 6.5b** inset).

The origin of this $\Delta V_{ph}(x)$ can be understood upon considering that local illumination (at *x*) creates photogenerated charges, and compensates the Schottky depletion region by transfer of holes across the ITO/perovskite interface (**Figure 6.4**).[21, 22] The observed polarity of the current and voltage upon photoexcitation is consistent with this interpretation. The equipotential ITO surface then extends to the overlapping electrode region (dark region). The follow-up processes of formation of an effective lateral field for propagation of the counter (-ve) carriers to the Au electrodes gives rises to $\Delta V_{ph}(x)$. The magnitude of the lateral voltage is expected to be a function of distance from the point of illumination to the counter electrode.[23, 24] This qualitative description can explain the trends observed in measurements such as: (i) Wavelength dependence where $\Delta V_{ph}(x)$ is higher for 532 nm compared to 635 nm with light incident from the

ITO side (ii) Higher mobility of the HOIP ($\mu \sim 10^1$ cm^2/(Vs)) as compared to Poly(3-hexylthiophene-2,5-diyl) (P3HT) ($\mu \sim 10^{-4}$ cm^2/(Vs)) leading to higher magnitude of $\Delta V_{ph}(x)$ [8, 25] (iii) The lowering of ΔV_{ph}(x) and the associated spatial gradient as the channel length L increases.

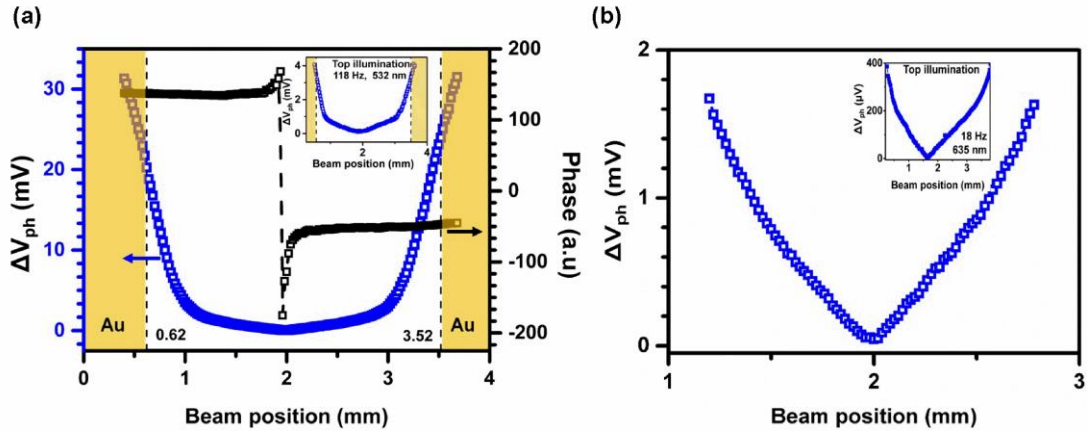

Figure 6.5: *Representative image of differential lateral photo voltage (ΔV_{ph}) from a PSD with a common ITO back electrode and gold top contacts. (a) ΔV_{ph} measured at a laser modulation frequency of 1019 Hz; black curve indicates the phase obtained from the lock-in amplifier of ΔV_{ph}. Inset shows ΔV_{ph} of another device under top illumination. (b) Depicts the expanded scale around the central region $\Delta V_{ph}(x)$ of* ***Figure: 6.5a****. Inset shows the lateral scan of alternate sample measured at 18 Hz modulation using 635 nm laser incident from the Au electrode side.*

6.6 Transient Photocurrent Analysis

Further insight into the device mechanism and the response timescale is obtained from transient photocurrent measurements as a function of light beam-spot location on the PSD channel (**Figure: 6.6**). It was observed that as the magnitude of the signal decreased with x, the single exponential-type transient response profile described by τ_c was maintained for all the beam positions. The decay lifetime τ_c obtained from the

transient photocurrent is of the order of ~ 43 μs and is in the range of lifetime measured in the planar-integrated single-crystalline perovskite photodetectors.[8, 26] The decrease of signal magnitude with *x* largely scales with the increase in the transit period, which is decided by the mobility and the electric field. This non-dispersive behavior is indicative of efficient transport of photogenerated carriers, where trap limited process does not dominate unlike a-Si and conjugated polymer based PSDs. Low monomolecular recombination rate and higher charge carrier mobility in these systems result in high switching speed of the PSD.[9] This feature extends the utility of the PSDs which can access higher scanning rates. Preliminary analysis of this device response to photoexcitation suggests that a drift-diffusion picture is applicable.

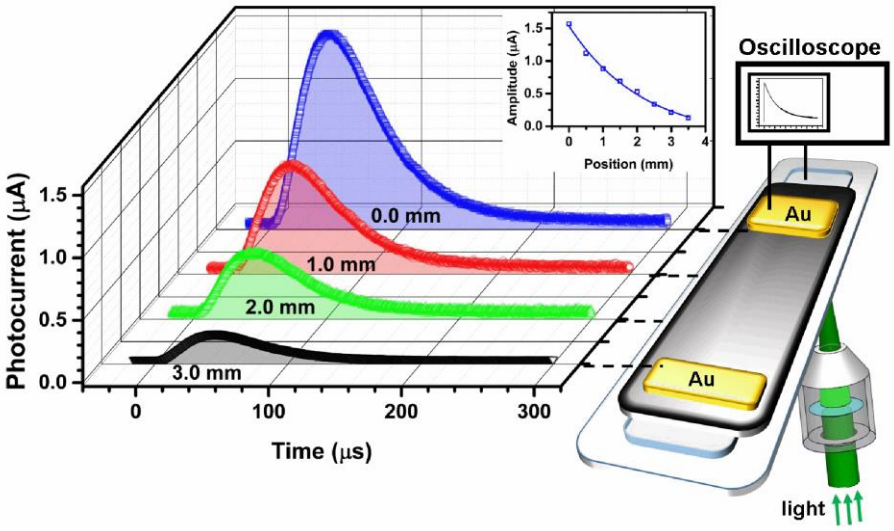

Figure 6.6: *Spatial dependence transient photocurrent measured at various points along the channel. The inset shows the decrease in amplitude as the point of illumination is translated along the channel.*

Polycrystalline nature of HOIP films with low trap densities and high carrier yield upon photoexcitation allows the use of drift-diffusion formalisms to model charge transport in the lateral dimension.[23, 27] Further insight and optimization of the spatial

and temporal response of these device structures can be obtained by device modeling which is underway. Measures to improve uniform films of HOIP over a large area and stable electrode interfaces need to be implemented to realize 2-D PSDs.

6.7 Summary

In summary, HOIP based PSD devices reveal promising performance as 1-D PSD demonstrating a linear response of the differential signal covering a wide wavelength range at reasonable bandwidth. These results form a major step towards realizing numerous functionalities in frontiers of image processing, beam profiling, charge coupled devices and other optoelectronics applications.

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Chapter 7

Summary and Future Directions

This thesis addressed some aspects of lateral charge transport in organic semiconductor an organic-inorganic hybrid perovskite systems. Two different architectures which are relevant in photovoltaics and field effect transistors are discussed. Materials used in the fabrication of these structures were carefully chosen considering their optoelectronic and dielectric performance and current relevance.

The first part of this thesis discussed ways to improve the charge transport in OFET channel by promoting orientation at the dielectric-semiconductor interface. Randomly ordered dipoles at the interface are known to be detrimental to the device parameters such as mobility and switching speed. Ferroelectric characteristics of the semicrystalline P(VDF-TrFE) polymer dielectric was used to improve the order at the interface. An electric field applied to the P(VDF-TrFE) during the curing of the film was used as the driving factor to enforce the order of dipoles at the interface. The improved order at the interface resulted in an enhancement of the field effect mobility by a factor > 300%. Atomic force microscopy and piezoresponse force microscopy revealed the evolution of the microstructure and polarization response as a function of the field. A reduced contrast of in-plane polarization observed in pre-poled P(VDF-TrFE) dielectric as compared to non-poled dielectrics proved the efficacy of this method and it corroborates with the high charge mobility seen in OFETs fabricated with pre-poled P(VDF-TrFE) dielectric.

The second part of this thesis addressed photogeneration and charge transport in MSM structure with HOIP semiconductor active layer. Lateral MSM structures with both symmetric electrode (Al/$MAPbI_3$/Al and Au/$MAPbI_3$/Au) and asymmetric electrode (Al/$MAPbI_3$/Au) combinations having varying channel length of 13 µm- 65 µm were fabricated. I-V behavior of these systems was studied under dark and light conditions. Charge transport showed asymmetric I-V behavior when the transport length is comparable to the SCR length scale in MSM structures with electrodes having different work function. Spatial mapping of the photocurrent profile in the channel of HOIP MSM structure was carried out using SPCM. Relatively high decay length of L_d^e ~ 3-4 µm was estimated from the photocurrent profile inside the channel. Drift-diffusion model of charge transport was used to understand I-V behavior and spatial profile of photocurrent inside the channel of MSM devices.

A lateral MSM structure based position sensitive detector having HOIP as the active material was fabricated. Highly uniform $MAPbI_3$ films were realized using a TPBi-containing antisolvent-mediated single-step solution process method. The additive treatment resulted in a pinhole-free film with reduced grain size and uniform films over an area of 1 cm^2. 1D PSD with channel length exceeding 4 mm was fabricated using gold electrodes, N2200 electron extraction layer and a common ITO bottom contact. Differential lateral photovoltage between two arms of the device showed excellent linear dependence on the position of light illumination. Also, a high spatial resolution of ~ 2 µV $µm^{-1}$ was obtained for PSD device structures with L ~ 3 mm. These devices exhibited sensitivity an order of magnitude higher than that of the analogous polymer-based PSD structure. The PSD operation was observed for a wide range of light wavelength. Transient measurements yielded single exponential-type response in these

devices with a $\tau_c \sim 40$ µs, which is independent of the position of illumination in the channel. It is an indicative of nondispersive charge transport behavior prevailing in this system.

Future Directions

Electric field poled ferroelectric surface can be used to promote directed growth of semi-crystalline polymers. Since the phenomena is universal, it could be applicable for a wide variety of ferroelectric-semiconductor combinations to obtain high switching speed and low operating voltage OFETs. This study can be extended to find the effect of charge transport at in ferroelectrics having varying domain sizes.

Analysis of the lateral MSM structure can be used to design and engineer of the metal-semiconductor interfaces for various device structures, especially in back contact solar cells.

PSD fabrication process can be improved to realize large area, pinhole free, uniform HOIP films. This can further enable the implementation of two dimensional PSDs.