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# Self-Assembled Nanodielectrics for High-Speed, Low-Voltage Solution-Processed Polymer Logic Circuits

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**Solution-processed polymer-based logic circuits are typically associated with high operating voltage and slow switching speeds. Here, polymer field-effect transistors (PFETs) fabricated on hybrid self-assembled nanodielectric (SAND) structures are reported, the latter consisting of alternating organic–inorganic layers exhibiting low leakage current (≈$10^{-9}$ A $cm^{-2}$) and high capacitance (≈0.8 μF $cm^{-2}$). Suitable device engineering, controllable dielectric parameters, and interface energetics enable PFET operation at ±1 V, field-effect mobility ($\mu_{FET}$) > 2.0 $cm^2$ $V^{-1}$ $s^{-1}$, subthreshold swing ≈100 mV $dec^{-1}$, and switching response ≈150 ns. These performance parameters are orders of magnitude higher than similar devices fabricated from other polymer dielectrics. Inverter and NAND logic circuits fabricated from these SAND-based PFETs possess voltage gain up to 38 and maximum-frequency bandwidth of 2 MHz. A systematic study comparing different classes of dielectric and semiconducting material attributes the enhanced performance to improved relaxation dynamics of the SAND layer and tunable chemically functionalized interfaces.**

## 1. Introduction

Solution-processable polymer field-effect transistors (PFETs) are poised to impact next-generation large-area flexible displays, printed radio frequency identification (RFID) tags, and disposable sensors.[1] Recent progress has provided polymer materials with field-effect mobility $\mu_{FET}$ > 1 $cm^2$ $V^{-1}$ $s^{-1}$[2–4]; however, devices with channel lengths in the printable regime ($L \geq 10$ μm) are often limited by high operating voltages (up to 80 V),[2,3] dielectric related bias stress,[5,6] and high power consumption.[7,8] A strategy to decrease PFET operating voltages is to increase the area-normalized gate capacitance ($C$).[9,10] Using ultrathin low-$\kappa$ gate dielectrics[11] and/or high-$\kappa$ materials is an obvious way to address this issue.[12] However, high-$\kappa$ dielectrics at the transport interface can reduce $\mu_{FET}$ due to dipolar broadening of density of states (DOS) or polarization-induced increase in the charge carrier effective mass.[13–16] While ion gel electrolytes and $\beta$-aluminates can reduce operating voltages,[10,17] they incur increased hysteresis and slow dynamic response.[18] Hence, there is a need for dielectric layers which imbue both p- and n-type PFETs with low operating voltages, high $\mu_{FET}$, and reasonable switching speeds.

Low-voltage FETs have been reported using organic–inorganic hybrid dielectrics.[6,7] However, typical devices require high temperature fabrication ($T$ > 400 °C) and are not scalable to arbitrary numbers of layers,[6,7,19] thus limiting the capacitance, leakage, and scaling properties of the dielectric structure.[20,21] In contrast, self-assembled nanodielectric materials (SANDs) are processable at low temperatures and are deposited with precise thickness control.[5,14] Furthermore, SANDs enhance the static response parameters in organic semiconductor,[7] carbon nanotube,[22] graphene,[23] and amorphous oxide FETs.[24] Hence, it is essential to understand the origin of high performance in SAND-based PFETs. Moreover, for many applications, it is essential to enhance the dynamic response parameters to obtain fast switching speeds and large gain-bandwidth products. However, it has not been possible to obtain fast switching speeds from SAND-based devices. This is mainly because of the inherent limitation of the SAND fabrication which is restricted to $Si/SiO_2$ substrates having substantial parasitic capacitance. This has remained an issue for most self-assembled dielectrics as well. Thus, to minimize parasitic capacitance for improved switching speed, SAND gate-dielectrics must be deposited on patterned metal gates. Here, we report an approach to SAND fabrication which combines conformal growth of an $HfO_x$ primer layer on patterned metal electrodes followed by solution phase SAND self-assembly. This result in ultrathin SAND-based

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PFETs with parasitic capacitance <1 nF cm$^{-2}$ and $\mu_{FET}$ ≈ 2.5 and 0.5 cm$^2$ V$^{-1}$ s$^{-1}$ for p-FETs and n-FETs, at operating voltages of |1 V| and |2 V|, respectively. These SAND-based devices and logic circuits exhibit dynamic response times of ≈150–350 ns, maximum-frequency bandwidth of ≈1.5–2 MHz, and voltage gain as high as ≈38. A detailed understanding of the interfacial transport property is then developed from a range of polymeric and dielectric materials to develop design principles for high performance dielectric materials.

## 2. Results and Discussion

### 2.1. Characterization of the SAND Layer

**Figure 1**a shows a typical device schematic and Hf-SAND growth procedure. First, patterned metal electrodes are conformally coated with 2.1 nm of $HfO_x$ by atomic layer deposition (ALD), followed by iterative self-assembly of Hf-SAND (see the Experimental Section). $C_{SAND}$ (at 10 kHz) for six layered iterative SAND-6L structures is ≈ 0.4 ± 0.1 μF cm$^{-2}$ and $C_{SAND}$ (at 10 kHz) for two layered SAND-2L structures is ≈0.8 ± 0.09 μF cm$^{-2}$. Leakage current densities ($J_{leak}$) as low as 10$^{-8}$–10$^{-9}$ A cm$^{-2}$ at ≤ 2 × 10$^8$ V m$^{-1}$ were obtained for SAND-based metal-insulator-metal (MIM) devices (Section S1, Supporting Information), which translate to an effective leakage current of 0.1 pA in the <1 V operating regime for patterned PFETs. This magnitude of leakage is significantly lower than native $SiO_2$ ($J_{leak}$ ≈1 A cm$^{-2}$ at field ≈± 2 × 10$^8$ V m$^{-1}$)[25] and marginally better than high-κ polymer dielectrics, $J_{leak}$ ≈ 2 × 10$^{-8}$ A cm$^{-2}$ at field ≈± 2 × 10$^8$ V m$^{-1}$ (Section S1, Supporting Information). Note that the high SAND-2L capacitance is comparable to the Debye layer of electrolytes and is rarely observed for polymer dielectric films. The SAND dielectric frequency response is shown in Figure 1b. $C_{SAND}(f)$ remains fairly constant over a frequency range extending to 5 MHz. This frequency response is about two orders of magnitude higher than solution based high-κ polymer dielectrics ($C$ ≈50 nF cm$^{-2}$) and electrolytes ($C$ ≈ 1 μF cm$^{-2}$), where response is limited to ≈10$^4$–10$^5$ Hz.[9,26]

SAND morphology over a large area 90 μm × 90 μm was analyzed to assess suitability for large-area devices and circuits. Atomic force microscopy (AFM) images show uniform coverage with rms roughnesses ≈5.4 Å (Figure 1c). The roughness of SAND on metal substrates is ≈10 times less than other solution processable high-κ dielectrics such as polyvinylidene flouride (PVDF) (details can be seen in Sections S2 and S3 in the Supporting Information). SAND scanning capacitance microscopy (SCM) assessments of capacitive spatial uniformity (Experimental Section) indicate minimal electrostatic force variations in the range ≈100 μV (Figure 1d), while PVDF-based dielectrics exhibit a variation of ≈3–5 mV (Section S3, Supporting Information). The low variation in the Hf-SAND SCM metrics is unusual for organic dielectrics and indicates uniform surface capacitance obtained via self-assembly. It will be seen that the exceptional SAND capacitive and surface uniformity is favorable for a high-quality semiconductor interfaces.[27]

### 2.2. Static Characterization of the SAND-Based PFETs

PFETs were fabricated on Hf-SAND-coated substrates, with patterned metal electrodes to minimize parasitic capacitance and to control the leakage properties (see the Experimental

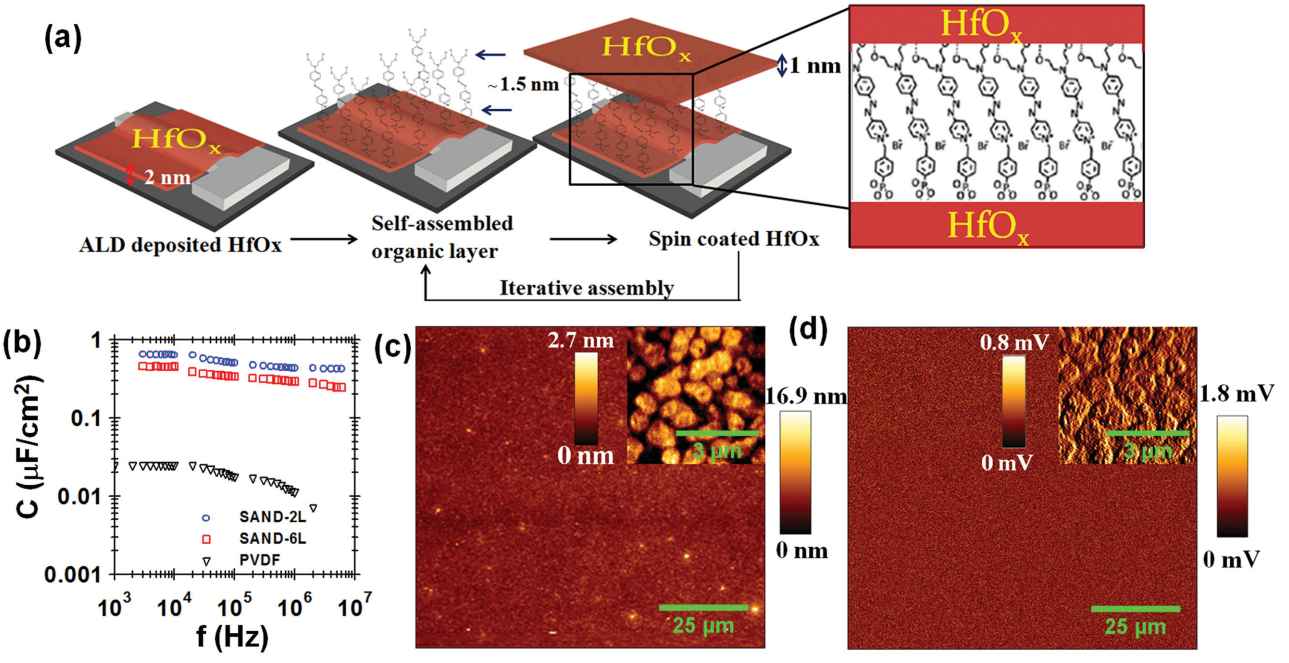


**Figure 1.** Capacitor fabrication and characterization. a) Schematic of the self-assembly process for Hf-SAND (≈5–18 nm) growth on top of ALD grown $HfO_x$ layer. b) Frequency response of a typical SAND-2L, SAND-6L, and high-κ PVDF dielectric film at $V_{rms}$ ≈50 mV. c) Height and d) SCM images (90 μm × 90 μm) indicating uniform Hf-SAND surface topography and capacitive properties over large area. Inset shows an enlarged 5 μm × 5 μm image with color scale bar.

Section). The channel width ($W$) was 0.5–1.0 mm, and $L$ was varied according to the experimental requirements (≈10 µm for dynamic measurements, ≈60–100 µm for static measurements). Two classes of semiconducting polymers were used: p-type PBTOR and n-type P(NDI2OD-T2). To facilitate semiconducting layer coating, *n*-octadecylphosphonic acid (ODPA) was self-assembled on the SAND surface. Capacitance-frequency measurements of ODPA-treated SAND indicate maximum $C_{SAND+ODPA}$ (at 10 kHz) is ≈0.17 ± 0.02 µF cm$^{-2}$ for SAND-6L structures, and ≈0.5 ± 0.09 µF cm$^{-2}$ for SAND-2L structures. Both PBTOR (p-FETs) and P(NDI2OD-T2) (n-FETs) PFETs on ODPA/SAND dielectric layers operate at $|V_g|$ and $|V_d|$ ≈1–2 V with negligible hysteresis and well-defined linear and saturation regimes (**Figure 2**). The performance parameters are: $\mu^h_{FET}$ ≈ 2.0–2.5 cm$^2$ V$^{-1}$ s$^{-1}$ and $\mu^e_{FET}$ ≈ 0.1–0.5 cm$^2$ V$^{-1}$ s$^{-1}$, with $I_{on}/I_{off}$ as large as $10^4$–$10^5$. Contact resistance is negligible (<1%) compared to channel resistance. Typical $\mu_{FET}$ statistics are shown as insets in Figure 2b,d, which compare favorably to state-of-the-art FETs operating at high voltages.[28–30] Furthermore, $V_{th}$ ≈ 0.05 V and SS ≈ 100–500 mV dec$^{-1}$ confirm low-voltage operation. Regarding environmental stability, device performance is stable for 4 weeks in vacuum (≈$10^{-2}$–$10^{-3}$ mbar) and for 3 weeks in ambient (Figure S7, Supporting Information). Bias stress measurements performed by applying a continuous 1.0 V (p-type) or 2.0 V (n-type) bias for up to ≈$10^4$ s (Figure S8, Supporting Information) show little difference in the transfer curves, indicating dielectric layer and transport interface stability. These results show that ODPA-functionalized Hf-SAND dielectrics provide high-quality intefaces for both electron- and hole-conducting polymers.

### 2.3. Analysis of the SAND–Semiconductor Interface

SAND-polymer interfacial characteristics were next investigated by comparing Hf-SAND PFET performance with that of PFETs fabricated from bisbenzocyclobutene (BCB), poly-methyl methacrylate (PMMA), and PVDF gate dielectrics (see **Table 1** for capacitance values) in bottom-gate top-contact p- and n-FETs. Under similar conditions, PBTOR PFETs fabricated on BCB and PMMA exhibit $\mu^h_{FET}$ ≈ 0.1–0.3 and 0.05–0.1 cm$^2$ V$^{-1}$ s$^{-1}$ at $V_g$ = –80 V, respectively, indicating that SAND increases PFET $\mu^h_{FET}$ by an order of magnitude compared to the other polymer dielectrics. Interestingly, n-FETs exhibit $\mu^e_{FET}$ ≈ 0.2–0.5 cm$^2$ V$^{-1}$ s$^{-1}$, irrespective of the dielectric layers. Hence, SAND dielectrics offer a general class of dielectric material where the transport properties at the dielectric-semiconductor interface are not compromised by high-$\kappa$ constituents in the gate dielectric.

A prerequisite for optimum PFET performance is a smooth dielectric-semiconductor interface with low energetic disorder.[13,14] In

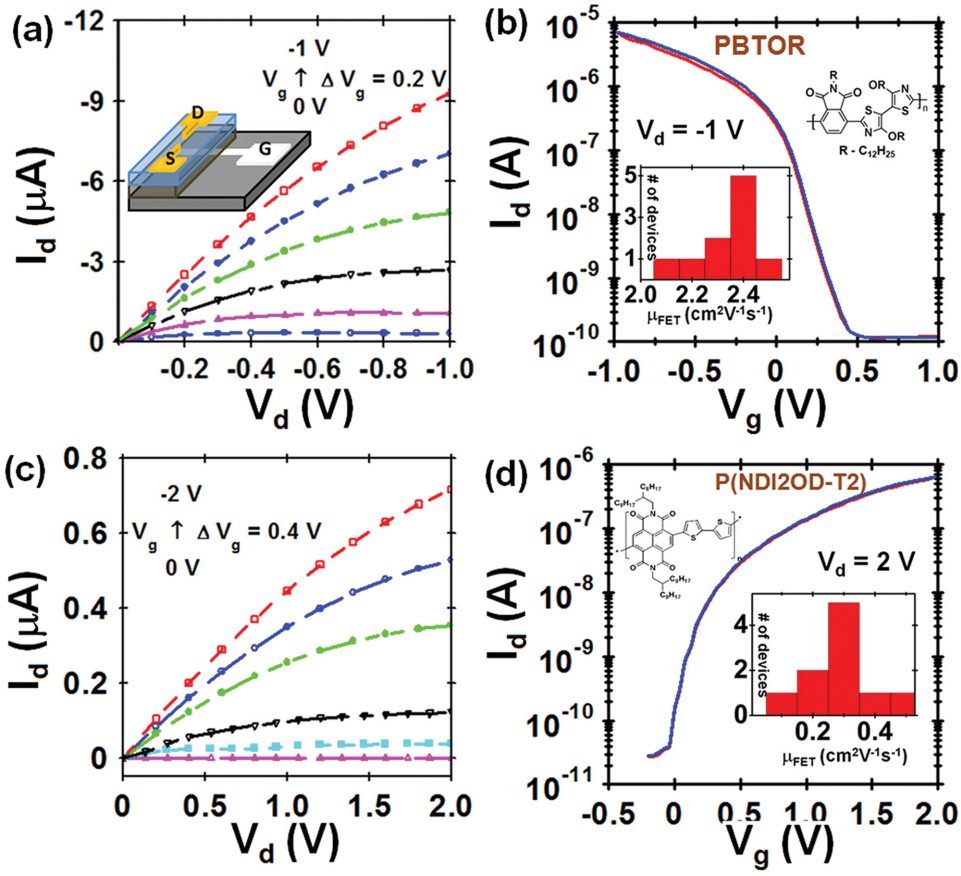


**Figure 2.** a) Output and b) transfer curves for p-type PBTOR semiconductor PFETs on Hf-SAND-2L. c) Output and d) transfer curves for P(NDI2OD-T2) (≈20 nm) n-type semiconducting based PFETs on SAND-4L. Length $L$ = 60 µm and width $W$ = 1 mm were maintained for all devices. Insets (b) and (d) show the statistical distribution of the field-effect mobilities of PBTOR and P(NDI2OD-T2)-based semiconductors, respectively.

  

**Table 1.** Temperature-dependent transport characterization data for PFETs fabricated with PBTOR and P(NDI2OD-T2) as the semiconducting layer and Hf-SAND, BCB, PMMA, or α-PVDF as the gate dielectric layer. Device dimensions are in the range as indicated in the text.

| Polymer | Dielectric | $C$ [nF cm$^{-2}$] | $\mu_{FET}$ [cm$^2$ V$^{-1}$ s$^{-1}$] | $E_a$ [meV] | SS [V dec$^{-1}$] | $\lvert V_{th}\rvert$ [V] |
|---|---|---|---|---|---|---|
| PBTOR | BCB | 4 | 0.3 | 73 ± 16 | 5 | −2 ± 1 |
| | PMMA | 7.9 | 0.1 | 94 ± 19 | 11 | −7 ± 3 |
| | ODPA/SAND | 174 | 2.5 | 58 ± 15 | 0.1 | −0.05 ± 0.1 |
| P(NDI2OD-T2) | BCB | 3.6 | 0.3 | 67 ± 14 | 7 | 1.7 ± 1.9 |
| | PMMA | 6 | 0.2 | 76 ± 7 | 12 | −4 ± 3 |
| | α-PVDF | 15 | 0.12 | 94 ± 13 | 17 | 11 ± 4 |
| | ODPA/SAND | 167 | 0.5 | 46 ± 9 | 0.8 | 0.1 ± 0.3 |

the present study, variable-temperature transport measurements were carried out (**Figure 3**a,b) to estimate the energetic disorder at the transport interface and probe the underlying transport mechanisms. Table 1 summarizes the temperature-dependent data for p-FETs and n-FETs having different dielectric layers. Arrhenius fits to the $\mu_{FET}(T)$ data of SAND-based p-FET yield a lower activation energy ($E_a$) ≈ 58 meV versus ≈73–94 meV for devices with BCB or PMMA dielectrics. Similarly, n-FETs exhibit lower $E_a$ (≈46 meV) for SAND devices versus ≈67–94 meV for the other dielectrics. These $E_a$ values are consistent with the high $|V_{th}|$ ≈ 5–10 V and $SS$ ≈ 7–11 V dec$^{-1}$ obtained for the BCB and PMMA-based PFETs compared to $|V_{th}|$ ≈ 0.05 V and $SS$ ≈ 100–500 mV dec$^{-1}$ for analogous SAND-based PFETs. An $E_a$ < 0.1 eV indicates sufficiently low interfacial energetic disorder to achieve high $\mu_{FET}$. The contrasting observation of lower $\mu_{FET}$ and $E_a$ in the n-FETs versus higher $\mu_{FET}$ and $E_a$ in p-FETs appears to reflect the growth morphology of the semiconductors on SAND. Thus, PBTOR forms a crystalline structure (Figure S5, Supporting Information) with grain boundaries that is likely to hinder intercrystallite charge hopping, hence raise $E_a$[31,32] while P(NDI2OD-T2) films have interconnected microstructures which should be more tolerant to disorder and favor chain-to-chain hopping (Figure S5, Supporting Information).[31]

Interface trap density was next evaluated from the relationship $N_{ss}^{max} = \left[SS \times \frac{\log(e)}{\frac{kT}{q}} - 1\right] \times C/q^2$, where $q$ is the unit electronic charge and $C$ is the dielectric areal capacitance.[27] $N_{ss}^{max}$ for the SAND-based devices is ≈$10^{12}$ cm$^{-2}$ eV$^{-1}$, significantly lower than the lowest value for the aforementioned polymer dielectrics, $5 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$ for BCB and $10^{13}$ cm$^{-2}$ eV$^{-1}$ for PMMA. These results are consistent with the trends of low $E_a$ and higher $\mu_{FET}$ for the SAND-based PFETs versus the polymer dielectric-based PFETs. Furthermore, conductivity in the linear regime $\sigma_{lin}$, monitored as a function of gate induced charge density, $n_G = C_i(V_g - V_{th})$ for p-FETs fabricated with different dielectrics indicates that at low $V_G$, $\sigma_{lin}$ values are comparable for all PFETs (Figure 3c). However, as $n_G$ increases, $\sigma_{lin}$ increases more rapidly for Hf-SAND-based PFETs. This result agrees to a mobility edge (ME) model with exponential DOS: $g(E) \approx \exp(-E/E_o)$, where $E_o$ is the width of DOS.[27,33] Polymer semiconductors are generally described as having disordered localized states with charge carriers in these states contributing negligibly to the effective $\sigma_{lin}$. Hence, charge transport involves thermal excitation to the transport level ($E_t$), requiring energy $E_a$. As the charge density increases, the quasi-Fermi level $E_F$ and $E_a \approx E_F - E_t$ are lowered. Thus, the increase in free charge density reflects decreased localized state or trap densities, leading to high conductance in the Hf-SAND–PFETs.

### 2.4. Dynamic Characterization of SAND–PFETs

The dynamic performance of Hf-SAND-based PFETs was next quantified using large and small signal analysis in a resistor

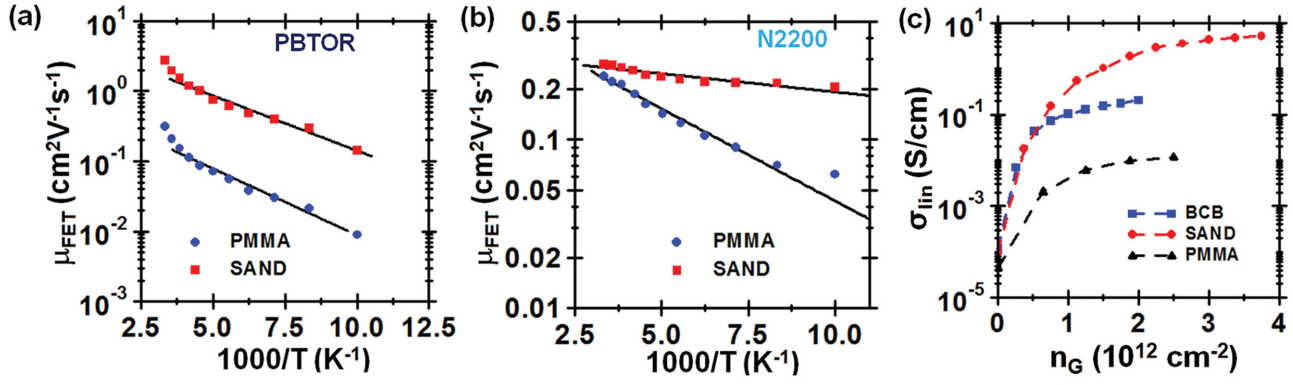


**Figure 3.** Variation of charge transport with temperature and $n_G$. Plot of $\mu_{FET}$ versus 1000/T for a) PBTOR p-FETs and b) P(NDI2OD-T2) n-FETs fabricated with Hf-SAND (6L) and PMMA dielectric layers. Typical device dimensions were $L$ = 60 μm, $W$ = 1 mm. c) Log scale plot of $\sigma_{lin}$ as function of $n_G$ for p-FETs fabricated with different dielectric layers.

load configuration to evaluate their potential in circuits for high frequency applications. PFET transient response is governed by the transit time of charge carriers across the channel, the dielectric relaxation time, and the charging duration of parasitic capacitance due to overlapping electrodes.[34] As evident from the above analyses, SAND provides a favorable interface for charge transport and exhibits efficient dipole relaxation response. Note that the Hf-SAND multilayer supports a capacitance of ≈100 nF cm$^{-2}$ versus ≈10 nF cm$^{-2}$ for aforementioned high-$\kappa$ polymer dielectrics, up to a frequency of $10^7$ Hz (Figure 1b). Furthermore, the higher SAND capacitance translates into a high transverse field at low $V_g$. This combination of an ordered interface, high transverse field, and rapid dielectric relaxation should enhance the SAND-based PFET dynamics. To minimize the parasitic capacitance for transient measurements, devices were optimized by patterning the gate structures with aligned S-D electrodes using combined lithography and physical masking techniques.

**Figure 4** shows PFET transient response obtained by monitoring the $I_{ds}(\Delta V_g)$ profile in response to an input square pulse of $\Delta V_g$ = 5 V (rise time = 10 ns). The $I_{ds}$(t) profile is obtained from the difference between the recorded profiles of $|V_d|$ = 4 V (ON state) and $|V_d|$ = 0 V (OFF state). The OFF state profile essentially originates from the parasitic capacitance due to the overlapping electrodes and is found to be <1 nF cm$^{-2}$ from *RC* fitting to the off-state response (Figure 4b). Note that the external circuitry *RC* time constant was maintained at least 50 times lower than the best FET response time (see the Experimental Section). PFET rise time ($t_{rise}$) and fall time ($t_{fall}$) are defined as the duration over which $I_{ds}$ changes from 10% to 90% and from 90% to 10% of the initial values, respectively. SAND PFETs with channel length $L \approx 10$ µm respond within 150–400 ns at an operating voltage of ±4 V. The magnitude of $t_{rise}$ and $t_{fall}$ were found to be 350 and 150 ns, respectively, for the best SAND-PBTOR PFETs at $V_d$ = –4 V. The magnitude of $t_{rise}$ increases to 2 µs when the operating voltage is decreased to $V_d$ = –1 V. In comparison, PFETs fabricated on the other polymer dielectrics exhibit $t_{rise}$ > 1.5 µs at $V_d$ = –40 V. The unity gain bandwidths of Hf-SAND-based PFETs are therefore in the 1.5–2 MHz range (Figure S11, Supporting Information) indicating the maximum intrinsic frequency response possible with these PFETs. Similarly, transient measurements on Hf-SAND-P(NDI2OD-T2) devices with channel length $L \approx 10$ µm reveal $t_{rise}$ and $t_{fall}$ of 2 µs and 1.3 µs, respectively, at $V_d$ = 4 V. From these observations, it is clear that SAND-based PFET dynamic performance is enhanced and can be attributed to the suitable interface energetics that promote high $\mu_{FET}$, ordered dipoles that allow efficient dielectric relaxation, and high transverse fields that result in low operating voltage devices.

### 2.5. Characterization of Polymer Logic Circuits

Finally, high-performance polymer logic circuits (PLC) enabled by SAND-based p-FETs and n-FETs are discussed. Inverters (**Figure 5**a) and universal NAND logic circuits (Figure 5c) were fabricated and characterized by input–output ($V_{in}$–$V_{out}$) and voltage gain curves. The logic circuits exhibit inverter-like behavior with a maximum voltage gain of ≈38 and a current gain of $10^5$–$10^6$ with near-ideal *Z*-type response. Note that the deviation from the ideal rail-to-rail operation is attributable to the imbalanced electron versus hole mobilities of P(NDI2OD-T2) and PBTOR, respectively, which could be further improved by tuning $V_{th}$ using different metal electrodes. Limited modifications to the inverter *W* and *L* are feasible within a small range while minimizing the parasitic contributions for large bandwidths. Typical static power dissipation ($V_{dd} \times I_{dd}$) from the present inverter-like circuit is in the range of 1–10 nW for $|V_{in}|$ = 1 V and 250 nW for $|V_{in}|$ = 4 V. In comparison, PVDF-based inverters have much higher power dissipation, in the range of 50–100 µW, for maximum $|V_{in}|$ = 80 V. Furthermore, the operating frequencies of these Hf-SAND logic circuits are ≈100 kHz for $L$ = 10 µm devices. A proof-of-concept demonstration of universal NAND gate operation is shown in Figure 5c. Note that threshold engineering is required for reliable rail-to-rail operation of more complicated circuits. Figure 5d compares the frequency response of PFETs fabricated with the various dielectric and semiconducting materials. It is evident

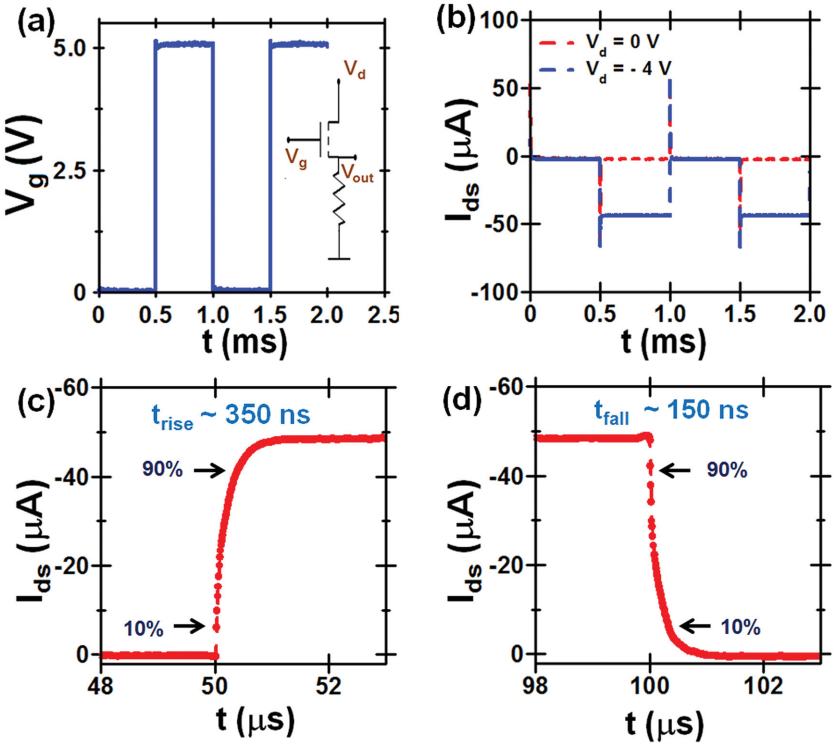


**Figure 4.** Dynamic response of p-FETs ($L$ = 10 µm, $W$ = 1 mm) fabricated with the PBTOR semiconductor and Hf-SAND (6L) dielectric layer in response to a square $V_g$ pulse. a) Input pulse (inset a) circuit schematic. b) Measured $I_{ds}$ through the resistor ($R$ = 1 KΩ ) at $V_{ds}$ = –4 V and $V_{ds}$ = 0 V. c, d) Zoomed transient profile of $I_{ds}(t)$ indicating the manner in which "on time: $t_{rise}$" and "off time: $t_{fall}$" were estimated.

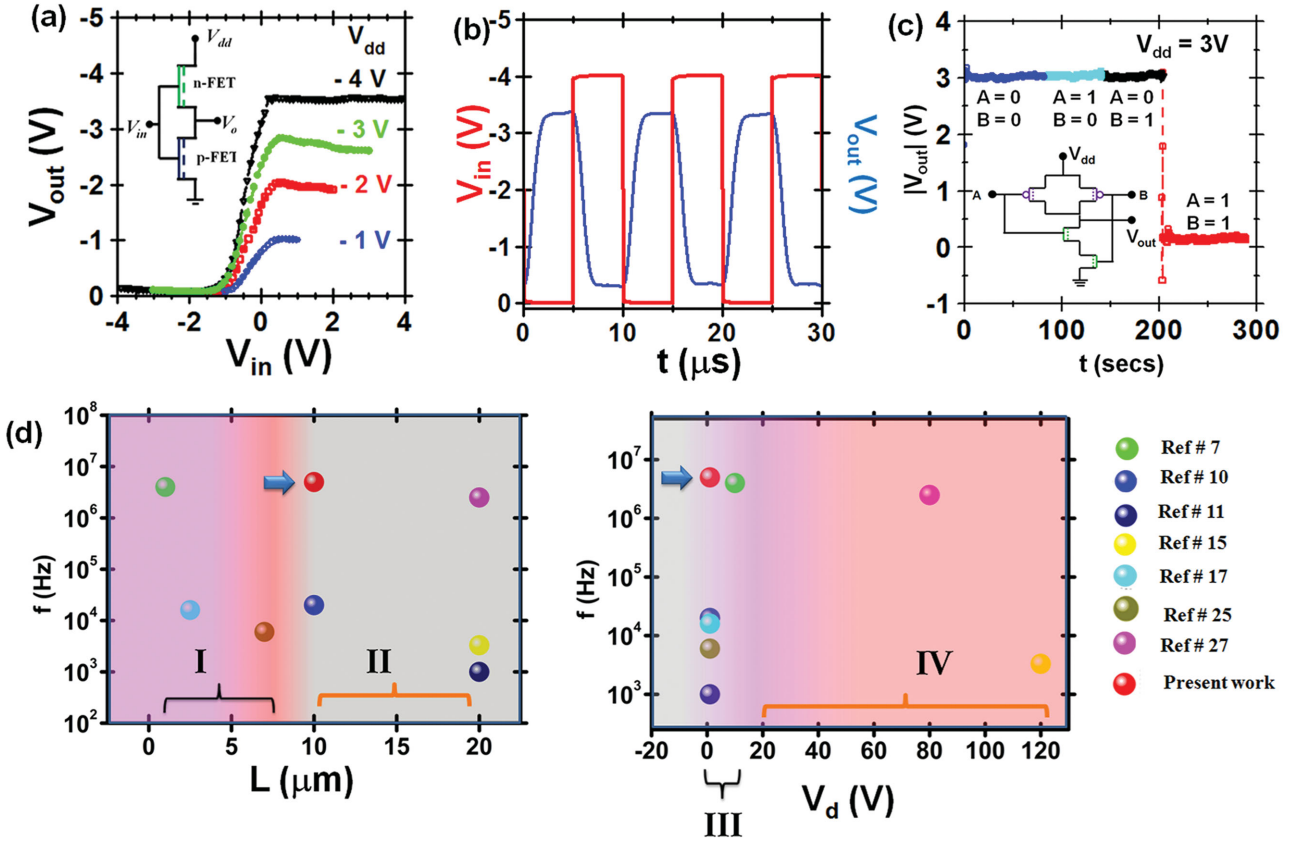


**Figure 5.** Static and dynamic characterization of Hf-SAND (6L)-based logic circuits fabricated with PBTOR-based p-FETs as load and P(NDI2OD-T2)-based n-FETs as driver. a) Typical transfer voltage curves for polymer inverters ($L$ = 10 μm, $W$ = 1 mm). The inset shows the circuit diagram. b) Representative switching response of the same inverter for a square pulse $V_{in}$ = −4 V and $V_{dd}$ = −4 V. c) Output response of NAND circuit for different combinations of input voltages. Input voltages of −3 and +3 V are considered as logic "0" and "1" respectively. d) Comparison of dynamic response from various PFET structures with a range of dielectric and semiconducting materials having different $L$ values and varied bias conditions. Region I indicates nonprintable regime for PFETs, region II corresponds to $L$ that is printable, regions III and IV correspond to low-power and high-power devices, respectively.

that SAND–PFETs offer a novel class of devices which demonstrate nanosecond operating speeds, and consume nanowatts of power with device dimensions compatible with flexible, printable electronics. These metrics are expected to improve further in smaller channel devices and with improved alignment strategies.

## 3. Conclusion

To conclude, we have integrated SAND dielectrics with patterned metal electrodes and demonstrated low-power, high-speed polymer transistors and logic circuits. These devices outperform all the organic devices reported so far in terms of both static and dynamic performance. Interfacial structure-property correlations are established by temperature-dependent transport measurements and microscopic structural characterization. Our results suggest that the design of hybrid dielectrics based on self-assembly technique results in densely packed ordered-dipole which affords enhanced polarizability and relaxation dynamics, thereby increasing relevant device metrics compared to PFETs using other polymer dielectrics. This strategy should provide guidelines for developing high-$k$ dielectric materials that provide an ordered interface for charge transport. The demonstration of low-voltage operating conditions accompanied by attractive device parameters and compatible for both p-type and n-type transport should pave the path to their usage in applications such as active matrix displays with high refresh rates and a range of analog organic-electronic circuits involving inverters, filters, integrators, and oscillators.

## 4. Experimental Section

*Materials*: Conjugated polymers PBTOR and P(NDI2OD-T2) were procured from Polyera Corporation, USA. $HfCl_4$ (precursor for $HfO_x$ dielectric fabrication) and ODPA for surface modification were obtained from Sigma-Aldrich Inc. Hydroxyl-free divinyltetramethylsiloxane BCB was obtained from Dow Chemical, while PMMA ($M_w \approx 996\,000$ g mol$^{-1}$) and PVDF–HFP copolymer pellets ($M_w \approx 455\,000$ g mol$^{-1}$) were procured from Sigma-Aldrich Inc.

*Methods*: FET Fabrication: Bottom-gated top contact devices were fabricated by coating lithographically patterned Al (thermally evaporated at $10^{-6}$ mbar, 1 Å s$^{-1}$, 30 nm thick) gate electrodes on RCA cleaned

glass substrates.This was followed by Hf-SAND growth as described in the next section. The surface of the Hf-SAND layer is modified by a self-assembled monolayer (SAM) of ODPA. Phosphonic-acid-based SAMs were prepared by immersing the SAND-coated substrates in a $2 \times 10^{-3}$ M ethanolic solution of ODPA overnight, rinsing in EtOH and drying under a nitrogen stream. Polymer active layers (20 nm) PBTOR and P(NDI2OD-T2) were spin coated from a 5 mg ml$^{-1}$ solution in chlorobenzene at 1000 rpm for 1 min and annealed in nitrogen atmosphere at 110 °C for 30 min. This was followed by patterning Au S-D electrodes ($10^{-6}$ mbar, 1 Å s$^{-1}$, 30 nm thick) to complete the device fabrication. The physical mask for the S-D electrodes was aligned under a microscope. The channel lengths for the devices were chosen depending on the dimensions of the gate electrode to obtain minimum overlap and low parasitic capacitance. Typical images of the patterned aligned electrodes are provided in the Section S7 in Supporting Information.

Hf-SAND Growth: The primer layer of Hf-SAND is grown by atomic layer deposition to obtain films of thickness ≈2 nm. This was followed by immersing the substrates in a preheated $\approx 3 \times 10^{-3}$ M solution of PAE for 1 h at 60 °C. Synthesis of PAE 4-[[4-[bis(2-hydroxyethyl)-amino]phenyl]diazenyl]-1-[4(diethoxyphosphoryl)benzyl]pyridinium is described elsewhere.[1] Further layers of $HfO_x$ were coated by solution processable methods under ambient conditions. The sol–gel precursor for $HfO_x$ was obtained from a 0.1 M of ethanolic solution of $HfCl_4$ under ambient. Concentrated $HNO_3$ was subsequently added to the cloudy dispersion in a 10:1 molar ratio ($HNO_3$:$HfCl_4$) as a hydrolysis catalyst. The buffer solution was stirred at 50 °C for 4–5 h before coating. The solution was further diluted to obtain a concentration of 0.02 M before coating. Substrates were coated within a NuAire Class 10 HEPA-filtered clean hood at 5000 rpm for 30 s and baked at 150 °C for 1 h. Dielectric properties were controlled by iterative growth of required layers ($HfO_x$ by spin coating and PAE by dipping in the solution as described earlier). Finally, a thin layer of $HfCl_4$ (0.02 M) was spin coated (5000 rpm for 30 s) on top as a capping layer and annealed at 150 °C for 30 min.

Polymer Dielectric Growth: Dielectric layers BCB, PMMA, and PVDF were obtained by spin coating the solutions from their respective solvents (BCB in Mesitylene, PMMA in propylene carbonate at 80 mg ml$^{-1}$, PVDF–HFP at 80 mg ml$^{-1}$ in *N*,*N*-Dimethylacetamide) at 1000 rpm for 1 min to obtain films of thickness 0.2–0.4 μm. The dielectric films were annealed in $N_2$ atmosphere.

Logic Gate Fabrication: Complementary inverters and NAND gates were fabricated with PBTOR as p-type and P(NDI2OD-T2) as n-type active layers. Au S-D electrodes were deposited on the polymer-coated SAND substrates by thermal deposition. For the NAND gate, the channel dimensions were maintained in the range of $L \approx 100$ μm and $W \approx 500$ μm for all four transistors. However, in the case of inverters the channel dimensions were modified to optimize the gain of the circuits while retaining the high-frequency operation. The DC characterizations of the logic circuits were performed using High Impedance Keithley 6514 Electrometer and the devices were biased using Keithley 2400 Sourcemeters. For the AC characterization the input pulse (±4 V) is generated using standard K-Pulse card, and the output response is monitored using Lecroy 6100A for various frequencies.

*Electrical Characterization*: DC Characteristics: Output and transconductance measurements of the PFET devices were performed using Keithley 4200 SCS and the capacitance measurements were performed using both HP4294A and Keithley 4200 SCS in a vacuum chamber of $10^{-3}$ mbar. $\mu_{FET}(T)$ was estimated by varying the $T$ using an He gas-based setup from Cryogenics Technology Ltd. Device degradation studies at room temperature were performed under both ambient and vacuum conditions (Figure S8, Supporting Information).

*Dynamic Measurement*: A train of square pulse voltage (±5 V, $t_{rise} \approx$ 10 ns) was applied with an arbitrary waveform generator (K-Pulse card of 4200 SCS) while the drain electrode was held at a constant DC bias (0 or ±4 V using Keithley 2400). The dynamic response of the PFETs was obtained by monitoring the voltage drop (inset in Figure 4a) over a resistor ($R \approx$ 1–10 kΩ), between the source electrode and ground, using an oscilloscope (Lecroy 6100A). The input capacitance of the set up (Lecroy 6100A with RF probes) was <5.5 pF with RC time constant ≈5 ns. Bandwidth of PFETs were estimated by biasing the devices at $|V_d| = 4$V and $|V_g| = 4$ V, independently using Keithley 2400 Sourcemeters to keep the transistor in the trans-diode regime. A gate–source AC voltage signal ($v_{gs}$) of 50 mV was applied through an AC coupler using an HP8116A function generator. The AC components of the drain ($i_d$) and the gate currents ($i_g$) were simultaneously measured using SR830 lock-in amplifiers. The current gain of the PFETs was estimated by the ratio of $i_d/i_g$. $f_T$ was determined as the frequency at which the current gain was unity.

AFM Measurements: AFM imaging was performed with a JPK Nanowizard 3 by using a Cr/Pt-coated conducting tip (Multi-75E, Resonant frequency, $\omega_R$ = 75 kHz) in noncontact mode. Surface capacitance of the sample was obtained by using a SAND layer coated on metal/ITO electrode and sensing the force proportional to d$C$/d$z$. SCM retrace measures the capacitive force using lock-in amplitude at $\omega_R$, while tip is driven at $\omega_R/2$ in hover mode (1 nm).

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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[1] H. Sirringhaus, *Adv. Mater.* **2014**, *26*, 1319.
[2] C. Kanimozhi, N. Yaacobi-Gross, K. W. Chou, A. Amassian, T. D. Anthopoulos, S. Patil, *J. Am. Chem. Soc.* **2012**, *134*, 16532.
[3] J. Li, Y. Zhao, H. S. Tan, Y. Guo, C.-A. Di, G. Yu, Y. Liu, M. Lin, S. H. Lim, Y. Zhou, H. Su, B. S. Ong, *Sci. Rep.* **2012**, *2*, 754.
[4] S. P. Senanayak, A. Z. Ashar, C. Kanimozhi, S. Patil, K. S. Narayan, *Phys. Rev. B* **2015**, *91*, 115302.
[5] M.-H. Yoon, C. Kim, A. Facchetti, T. J. Marks, *J. Am. Chem. Soc.* **2006**, *128*, 12851.
[6] R. P. Ortiz, A. Facchetti, T. J. Marks, *Chem. Rev.* **2009**, *110*, 205.
[7] A. Luzio, F. G. Ferré, F. D. Fonzo, M. Caironi, *Adv. Funct. Mater.* **2013**, *24*, 1790.
[8] M. Uno, K. Nakayama, J. Soeda, Y. Hirose, K. Miwa, T. Uemura, A. Nakao, K. Takimiya, J. Takeya, *Adv. Mater.* **2011**, *23*, 3047.
[9] L. Herlogsson, Y.-Y. Noh, N. Zhao, X. Crispin, H. Sirringhaus, M. Berggren, *Adv. Mater.* **2008**, *20*, 4708.
[10] J. H. Cho, J. Lee, Y. Xia, B. Kim, Y. He, M. J. Renn, T. P. Lodge, C. Daniel Frisbie, *Nat. Mater.* **2008**, *7*, 900.
[11] Y.-Y. Noh, N. Zhao, M. Caironi, H. Sirringhaus, *Nat. Nanotechnol.* **2007**, *2*, 784.
[12] J. Li, Z. Sun, F. Yan, *Adv. Mater.* **2012**, *24*, 88.
[13] J. Veres, S. D. Ogier, S. W. Leeming, D. C. Cupertino, S. Mohialdin Khaffaf, *Adv. Funct. Mater.* **2003**, *13*, 199.
[14] S. P. Senanayak, S. Guha, K. S. Narayan, *Phys. Rev. B* **2012**, *85*, 115311.
[15] I. N. Hulea, S. Fratini, H. Xie, C. L. Mulder, N. N. Iossad, G. Rastelli, S. Ciuchi, A. F. Morpurgo, *Nat. Mater.* **2006**, *5*, 982.

  

[16] R. C. G. Naber, C. Tanase, P. W. M. Blom, G. H. Gelinck, A. W. Marsman, F. J. Touwslager, S. Setayesh, D. M. de Leeuw, *Nat. Mater.* **2005**, *4*, 243.
[17] B. Zhang, Y. Liu, S. Agarwal, M.-L. Yeh, H. E. Katz, *ACS Appl. Mater. Interfaces* **2011**, *3*, 4254.
[18] L. Herlogsson, X. Crispin, S. Tierney, M. Berggren, *Adv. Mater.* **2011**, *23*, 4684.
[19] H. Klauk, U. Zschieschang, J. Pflaum, M. Halik, *Nature* **2007**, *445*, 745.
[20] M.-H. Yoon, A. Facchetti, T. J. Marks, *Proc. Natl. Acad. Sci. USA* **2005**, *102*, 4678.
[21] C. E. D. Chidsey, D. N. Loiacono, *Langmuir* **1990**, *6*, 682.
[22] V. K. Sangwan, R. P. Ortiz, J. M. P. Alaboson, J. D. Emery, M. J. Bedzyk, L. J. Lauhon, T. J. Marks, M. C. Hersam, *ACS Nano* **2012**, *6*, 7480.
[23] V. K. Sangwan, D. Jariwala, K. Everaerts, J. J. McMorrow, J. He, M. Grayson, L. J. Lauhon, T. J. Marks, M. C. Hersam, *Appl. Phys. Lett.* **2014**, *104*, 083503.
[24] K. Everaerts, L. Zeng, J. W. Hennek, D. I. Camacho, D. Jariwala, M. J. Bedzyk, M. C. Hersam, T. J. Marks, *ACS Appl. Mater. Interfaces* **2013**, *5*, 11884.
[25] K. Everaerts, J. D. Emery, D. Jariwala, H. J. Karmel, V. K. Sangwan, P. L. Prabhumirashi, M. L. Geier, J. J. McMorrow, M. J. Bedzyk, A. Facchetti, M. C. Hersam, T. J. Marks, *J. Am. Chem. Soc.* **2013**, *135*, 8926.
[26] E. Said, X. Crispin, L. Herlogsson, S. Elhag, N. D. Robinson, M. Berggren, *Appl. Phys. Lett.* **2006**, *89*, 143507.
[27] S. M. Sze, *Physics of Semiconductor Devices*, Wiley Interscience, Hoboken, NJ **2006**.
[28] H. Yan, Z. Chen, Y. Zheng, C. Newman, J. R. Quinn, F. Dotz, M. Kastler, A. Facchetti, *Nature* **2009**, *457*, 679.
[29] X. Guo, J. Quinn, Z. Chen, H. Usta, Y. Zheng, Y. Xia, J. W. Hennek, R. P. Ortiz, T. J. Marks, A. Facchetti, *J. Am. Chem. Soc.* **2013**, *135*, 1986.
[30] C. B. Nielsen, M. Turbiez, I. McCulloch, *Adv. Mater.* **2013**, *25*, 1859.
[31] R. Noriega, J. Rivnay, K. Vandewal, F. P. V. Koch, N. Stingelin, P. Smith, M. F. Toney, A. Salleo, *Nat. Mater* **2013**, *12*, 1038.
[32] H.-R. Tseng, H. Phan, C. Luo, M. Wang, L. A. Perez, S. N. Patel, L. Ying, E. J. Kramer, T.-Q. Nguyen, G. C. Bazan, A. J. Heeger, *Adv. Mater.* **2014**, *26*, 2993.
[33] Y. Xia, J. H. Cho, J. Lee, P. P. Ruden, C. D. Frisbie, *Adv. Mater.* **2009**, *21*, 2174.
[34] S. P. Senanayak, K. S. Narayan, *Adv. Funct. Mater.* **2014**, *24*, 3324.