Novel electrodes and active materials for optoelectronics and memory devices

A Thesis
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DOCTOR OF PHILOSOPHY

By

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Dedicated to Prof. G.U.K

And My Parents

To Prof. G. U. K

“You are the one for me, who fought

Any time I need or anytime of drought”

“In difficult times my hand you caught”

“To my life, new dimensions you brought”

“Always provoked me with great thoughts”

“In my mind it will be you whom I will sought”

DECLARATION

I hereby declare that the thesis entitled "N**ovel electrodes and active materials for optoelectronics and memory devices**" is an authentic record of research work carried out by me at the Chemistry and Physics of Materials Unit, Jawaharlal Nehru Centre for Advanced Scientific Research, Bangalore, India under the supervision of Professor **G. U. Kulkarni** and that it has not been submitted elsewhere for the award of any degree or diploma.

In keeping with the general practice in reporting scientific observations, due acknowledgment has been made whenever the work described is based on the findings of other investigators. Any omission that might have occurred due to oversight or error in judgment is regretted.

K. D. Mallikarjuna Rao

CERTIFICATE

Certified that the work described in this thesis titled "**Novel electrodes and active materials for optoelectronics and memory devices**" has been carried out by Mr. **K. D. Mallikarjuna Rao** at the Chemistry and Physics of Materials Unit, Jawaharlal Nehru Centre for Advanced Scientific Research, Bangalore, India under my supervision and that it has not been submitted elsewhere for the award of any degree or diploma.

Professor G. U. Kulkarni

(Research Supervisor)

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Preface

The thesis work pertains to realizing electrode materials and active elements for optoelectronic and multi-level memory devices. It is structured into four parts.

Chapter I presents the evolution of functional materials into devices. Besides providing a historical account, new strategies and approaches from the recent past have been mentioned. Next generation functional materials, particularly, nanomaterials of different dimensionalities have been discussed in relation to the corresponding devices. **Chapter II** introduces characterization techniques used in this thesis.

Chapter III deals with a new generation transparent conductor in the form of highly interconnected metal (Au, Ag, Cu etc.) wire network, invisible to the naked eye, on common substrates such as glass. Chapter-IIIA details out the method of producing such electrodes using a newly developed recipe termed as "*crackle lithography*". It is applicable to large areas, involving only three steps. The process employs spontaneously formed crack network in dried colloidal layer as a sacrificial template for metal deposition. The TCEs thus formed exhibit optoelectronic properties that are superior in many ways, to those of conventional indium tin oxide films and other alternate materials. With PET as substrate, flexible yet robust TCE could be produced and with quartz, the spectral range could be widened to cover UV and IR regions. The method is applicable to various metals and hybrid materials as well as to surfaces with complex curvatures. Importantly, it is a low cost method, scalable for large area substrates. Using these TCEs, devices such as solar cells and transparent heaters have been successfully fabricated replacing the commonly used ITO film as detailed out in chapter-IIIB. Other devices fabricated include many non-optoelectronic devices namely transparent capacitor and transparent strain

sensor. In general, the usage of wire network based TCEs has been successfully extended to transparent electronics.

Chapter IV deals with the fabrication of in-plane resistive switching devices with nanocrystalline PdO thin film as active material. The devices showed multi-level resistive switching with as many as five memory states with good endurance and retention while working in ambient conditions. On the basis of SEM, EDAX, Raman spectroscopy and low temperature resistivity measurements, the mechanism of memory state switching has been proposed. In addition, for the first time, a "multiplex number" is defined to quantify the efficiency of multi-level resistive switching devices. The present PdO based device has shown a high multiplex number when compared to values estimated for devices reported in the literature.

Chapter V presents a simple lithography-free, solution-based method of soldering of carbon nanotubes with ohmic contacts. The soldering was realized by thermal/electrical activation or by both in sequence. The soldered joints were robust enough to sustain strain caused during the bending of flexible substrates as well as during ultrasonication. Further, the specific contact resistance has been estimated from the transmission line model. **Chapter VI** presents summary and future outlook of the thesis work.

Table of contents

Acronyms

0D	Zero Dimension
1D	One Dimension
2D	Two dimension
3D	Three dimension
AFM	Atomic force Microscope
CNT	Carbon Nanotubes
CP	Crackle Precursor/crackle patterns
DC	Direct Current
DI	Deionised
EBL	Electron beam Lithography
ED	Electron Diffraction
JV	Current Density-Voltage
LCD	Liquid Crystal Display
LED	Light Emitting diode
MCP	Metal in crackle patterns
MFM	Magnetic force Microscopy
MOSFET	Metal-oxide-semiconductor Field effect transistor
MP	Melting Point
MRI	Magnetic resonance Imaging
MWNT	Multi walled carbon nano-Tube
NIL	Nanoimprint Lithography
NIR	Near field infrared Spectroscopy
NW	Nano wire
OP	Optical profiler
OSC	Organic Solar cell
PC	Polycarbonate
PDMS	Polydimethylsiloxane
PL	Photolumenescence
PMMA	Poly-methyl-methacrlyate
PEDOT:PSS	Poly(3,4- ethylenedioxythio phene) : poly (styrenesulfonate)
PET	Polyethylene terephthalate PL
PMMA	Poly-methyl-methacrlyate
PVA	Poly vinyl alcohol
PVD	Physical vapour Deposition
QD	Quantum Dot
R2R	Roll-to-roll
RIE	Reactive ion etching
RT	Room temperature
SAED	Selected area electron diffraction
SAM	Self-assembled monolayers
SEM	Scanning electron microscopy
SERS	Surface enhanced Raman scattering
SP	Surface Plasmon
SPR	Surface plasmon resonance
STM	Scanning tunnelling microscopy
SWNT	Single walled carbon nanotubes
TCE	Transparent conducting electrodes
TEM	Transmission electron microscopy
TFT	Thin film transistor
UV	Ultraviolet
UV-vis	Ultraviolet-visible
UHV	Ultra-high vacuum
XAFS	X-ray absorption fine structure
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction

Chapter I

Introduction

I.1 History of Materials

A lump of matter with atoms and molecules as constituents, is termed as a material when one of its properties is seen exploitable in some application. Stone for example, is perhaps the first material known to mankind, where its hardness became useful in hunting animals, chopping food items etc. At the end of stone age ~5000 BC, the first ceramic was discovered. It was a great achievement to turn clay into a resistant ceramic by fire. The ceramics were used to

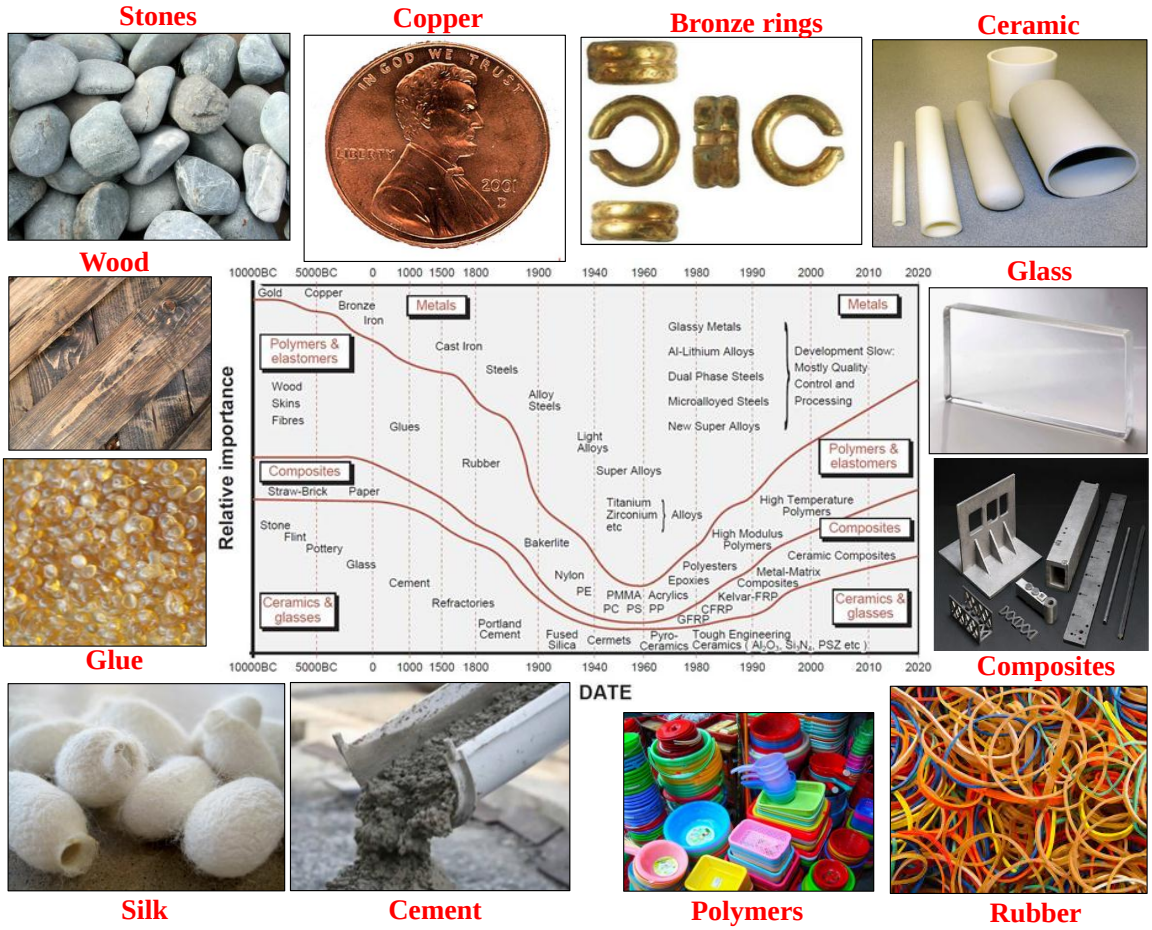

Figure I.1 A plot showing chronological evolution of materials and their relative importance. Some useful materials are shown surrounding the plot.[3-10]

produce pottery and decorative items. Following the discovery of metals and alloys such as copper, tin, brass and bronze, a large variety of materials and tools emerged and several civilizations evolved around them. In 10^{th} century BC, glass was discovered, the main constituents being silica, sodium oxide and alumina.[1] Since glass is optically transparent, it became customary in openings such as windows. In 1525, rubber was found in South America. Magellan, a famous Portuguese navigator explored its use as eraser. Subsequently tremendous applications has been realized with rubber such a tyres, shoes and bags etc., because of its unique physical and chemical properties.[2] In early 19^{th} century, Bakelite- one of the first plastics made from synthetic components, was discovered. It is electrically insulating and heat resistant, which was used in telephone casings, kitchenware, jewellery, fire alarms, and children's toys. In the present age, plastic has become material of daily use globally with endless applications. Mid-19^{th} century, discovery of materials such as stainless steel, synthetic rubber, nylon, teflon and piezoelectric ceramics are other breakthroughs. These materials and thus fabricated devices presented a wide range of applications and tools of comfort and luxury for mankind. Figure I.1 below depicts some aspects of this evolution.

I.2 Nanomaterials and classification

During the late 20^{th} century with discoveries in quantum physics and chemistry, new era of materials began. New families of metal oxides, nitrides, chalcogenides were made in the following decades exhibiting interesting properties- electrical, optical, magnetic and piezoelectric etc. In parallel, there came new intermetallic compounds and alloys, organic-inorganic hybrids, liquid crystals and so on. Many exotic properties were studied in these materials during second half of the century. A highlight from this era has been, high-temperature superconductivity observed in cuprates.[11] In the last three decades, there has been a surge of

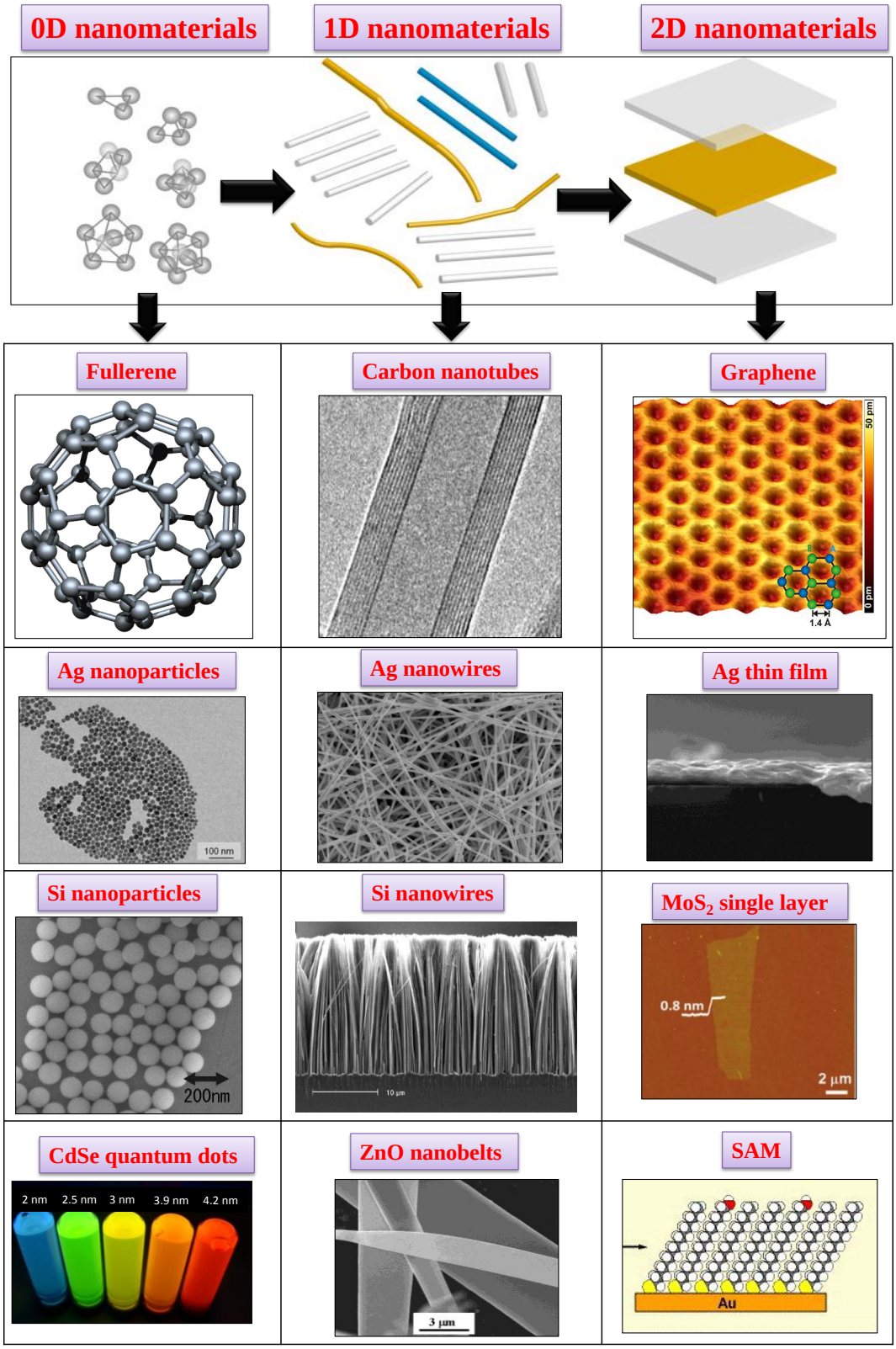

Figure I.2 Examples of nanomaterials of various compositions, sizes and dimensionalities.[12-18]

activity related to nanomaterials. 'Nano' refers to "one-billionth", in the order of 10^{-9}, which designates "extreme smallness". Nano has its origin in the lecture "There's plenty of room at the bottom" delivered by the famous physicist, Richard Feynmann in 1959.[19] Nanoscience is about studying the properties of objects, whose physical dimensions (at least one dimension) are in the range of 1-100 nm. When the materials are confined to such a small length scale, quantum confinement takes place and simultaneously effective surface area increases. As a result, nanomaterials possess very interesting electrical, optical, thermal and magnetic properties which crucially depend upon the size of the system. Besides the size, dimensionality of a nanomaterial- 0D, 1D or 2D, and shape in general, also influence its properties.[20] Accordingly, several new nanomaterials exhibiting exotic properties with various sizes and dimensionalities have been synthesized and some important examples are shown in Figure I.2 and details are given below. The synthesis methods for nanomaterials includes, bottom-up chemical and top-down processes and some times, hybrid methods as well.

Fullerenes: A fullerene is a carbon molecule in the form of a hollow sphere, ellipsoid, tube or any such shape. Spherical fullerenes are also called buckyballs, and they resemble a football (soccer). The examples of fullerene are C_{60}, C_{70}, C_{50} and C_{28}, and their size is typically less than 1 nm. These molecules are known for superconductivity, heat resistant and ferromagnetism properties. Fullerenes have been extensively used for several biomedical applications such as MRI contrast agents, X-Ray imaging contrast agents, photodynamic therapy and drug and gene delivery.

Ag nanoparticles: Ag nanoparticles area typical example of metal nanoparticles. The size of Ag nanoparticles range from 1-100 nm and can be synthesized by various wet chemical methods. Nanoparticles prepared these days are highly monodispersed compared to those (Au) prepared by

Michael Faraday in 1857.[21] These particles have been used extensively as anti-bacterial agents in the health industry, food storage, textile coatings and a number of environmental applications. It is important to note that despite of decades of use, toxicity of silver is still not clear.

Si nanoparticles: Silicon nanoparticles have been synthesized by physical or chemical methods with size range of 1-10 nm. These particles are known for their optical properties which can be tuned either by changing the size or surface passivation. Si nanoparticles find applications in biomedical screening such as diagnostics, targeted cancer therapies and localized chemotherapy.

CdSe quantum dots: CdSe-derived nanoparticles with sizes below 100 nm exhibit a property known as quantum confinement. High temperature pyrolysis and radiolytic methods were adopted to synthesize cadmium selenide nanoparticles. Three CdSe crystalline forms are known- wurtzite (hexagonal), sphalerite (cubic) and rock-salt (cubic). The sphalerite CdSe structure is unstable and converts to the wurtzite form upon moderate heating. CdSe quantum dots have been implemented in a wide range of applications including solar cells, light emitting diodes and biofluorescent tagging. Cadmium selenide is known to be carcinogenic and therefore, appropriate precautions should be taken while handling it.

Carbon nanotubes: Carbon nanotubes (CNTs) are allotropes of carbon having cylindrical nanostructure. Single walled nanotubes, double walled nanotubes and multi-walled nanotubes are three classes of carbon nanotubes. Arc discharge, laser ablation, plasma torch and chemical vapor deposition are few synthesis methods for CNTs. CNTs diameter ranges from 1 to 300 nm and length, from 500 nm to few tens of microns. Depending on the structure, a CNT can exhibit varied electrical conductivity- semiconducting or as a metallic. CNTs are known for their high thermal, electrical, optical and mechanical properties. Biomedical, electrical circuits and devices,

electrical cables and wires, actuators, batteries, solar cells, hydrogen storage, supercapacitor, radar absorption and textile are just a few examples where CNTs are being used extensively.

Ag nanowires: Ag nanowire (NW) is a typical example of a metallic 1D nanomaterial. The diameter and length of Ag NWs are usually in the range of 40–80 nm and 2-25 μm, respectively. Template-directed, one-pot reduction route and chemical reduction with capping agent are few methods for synthesis of Ag NWs. Electrical, optical and thermal properties of Ag NWs are highly interesting. Solar cells, light emitting diodes and strain sensors are few applications of Ag NWs.

Si nanowires: Si NW is one the fascinating material among semiconducting 1D nanomaterials. The diameters and lengths of Si NWs are in the range of 3-50 nm and 0.5 and 25 μm, respectively. Si NWs are semiconducting, and the dopant type and concentration can be controlled during synthesis. Due to their novel properties such as unique electrical, optical and mechanical, these nanowires receive much attention. Si NWs have been used extensively in field-effect transistors, optoelectronic devices and photonics.

ZnO nanobelts/nanowires: ZnO NW is a semiconducting 1D nanomaterial, known for its unique electrical and optical properties. These structures are widely used in applications such as gas sensors, strain sensors, photodetectors and solar cells.

Graphene: Graphene is pure carbon, in the form a single atomic layer with thickness of ~0.4 nm, the thinnest material ever made. Chemical vapour deposition, exfoliation and nanotube slicing are few synthesis methods for graphene. Graphene is the only form of carbon (and generally among all solid materials) in which every atom stands exposed to chemical reaction from two sides. Graphene is remarkably strong for its very low weight and high transparency, high electrical and thermal conductivities. Graphene has a wide variety of utility, in

optoelectronics, biological engineering, filtration, lightweight composites, photovoltaics and energy storage devices. Graphene dispersion are used in paints and coatings, lubricants, oils and functional fluids, capacitors and batteries, thermal management applications, display materials as well as in packaging etc. Graphene may find innumerable applications in the future, being the most fascinating material.

Ag thin film: Ag thin film is an example of a metallic 2D nanomaterial. These thin films are fabricated either by vacuum deposition or by solution processed methods, typical thickness being 5 to 100 nm. Ag thin film exhibits very interesting optical and thermal properties, with high conductivity among all metallic 2D nanomaterials. Ag thin film is one of the most common electrode material for fabrication of devices and circuits. Especially in optoelectronics, it has high demand as an electrode.

MoS_2 layer: MoS_2 is a typical example of a 2D nanomaterial from layered transition-metal dichalcogenide families. MoS_2 with single layer thickness of ~ 0.65 nm, is also known as an inorganic graphene. It has an intrinsic direct band gap of 1.8 eV. Recently, significant work has come out on MoS_2, opening up a whole new range of possibilities in optical and optoelectronic devices. MoS_2 has been shown to possess very high mechanical strength and thermal stability up to 1100 °C. Spintronics, FETs, gas sensors, solar cells and electrochemical devices are some examples, where MoS_2 layer is used.

Self-assembled monolayers: Self-assembled monolayers (SAM) of organic molecules are molecular assemblies formed spontaneously on surfaces by adsorption. SAMs produced by adsorption from solution, from the vapor phase or by physisorption using Langmuir–Blodgett method. These monolayers not only lower the surface energy but also increase the contact angles of the surfaces. SAMs are an inexpensive and versatile surface coating for applications including

control of wetting and adhesion, chemical resistance, bio compatibility, sensitization, and molecular recognition for sensors.

I.3 Nanolithography

To use individual nanomaterials in devices involving thermal, magnetic, optical properties and particularly electrical signaling, to measure them one would require an address system. The address system refers to electrodes or connections, which receive or transmit the input/output signal from a single device out of an array of devices. The address system may provide physical contacts/connections between the nanomaterial and measurement unit/system. The physical contacts should translate the signal effectively without any lose. Depending on the size and dimensionality of the nanomaterial and particular application, design and dimensions of the address system is varied. The address systems are usually laid with metallic thin films. In many of the common day-to-day devices, important functional materials find their place, where each material is addressed by a set of metal electrodes. In the case of supercapacitors and solar cells etc., the nanomaterials should be arranged or organized in a specific manner. For all the above mentioned situations, materials have to be patterned with various length scales. Such patterning of the material is called lithography. In Latin, *litho = stone*, *graphein = writing*, i.e writing on an arbitrary substrate. Lithography was first introduced in 1798 by Alosis Senefelder as a printing tool for transferring geometric shapes on a mask to the surface of a desired substrate. The patterning of the materials can be done using photons, electrons, ions or even sharp probes.[22] Various lithography techniques have emerged based on the source employed and method adopted as depicted in Figure I.3 and discussed below. The lithography methods are usually top-down approaches.

Photolithography: This technique utilizes the exposure of the photons on a photoresist through a photomask containing required design. Depending on the exposure conditions, polymer chains

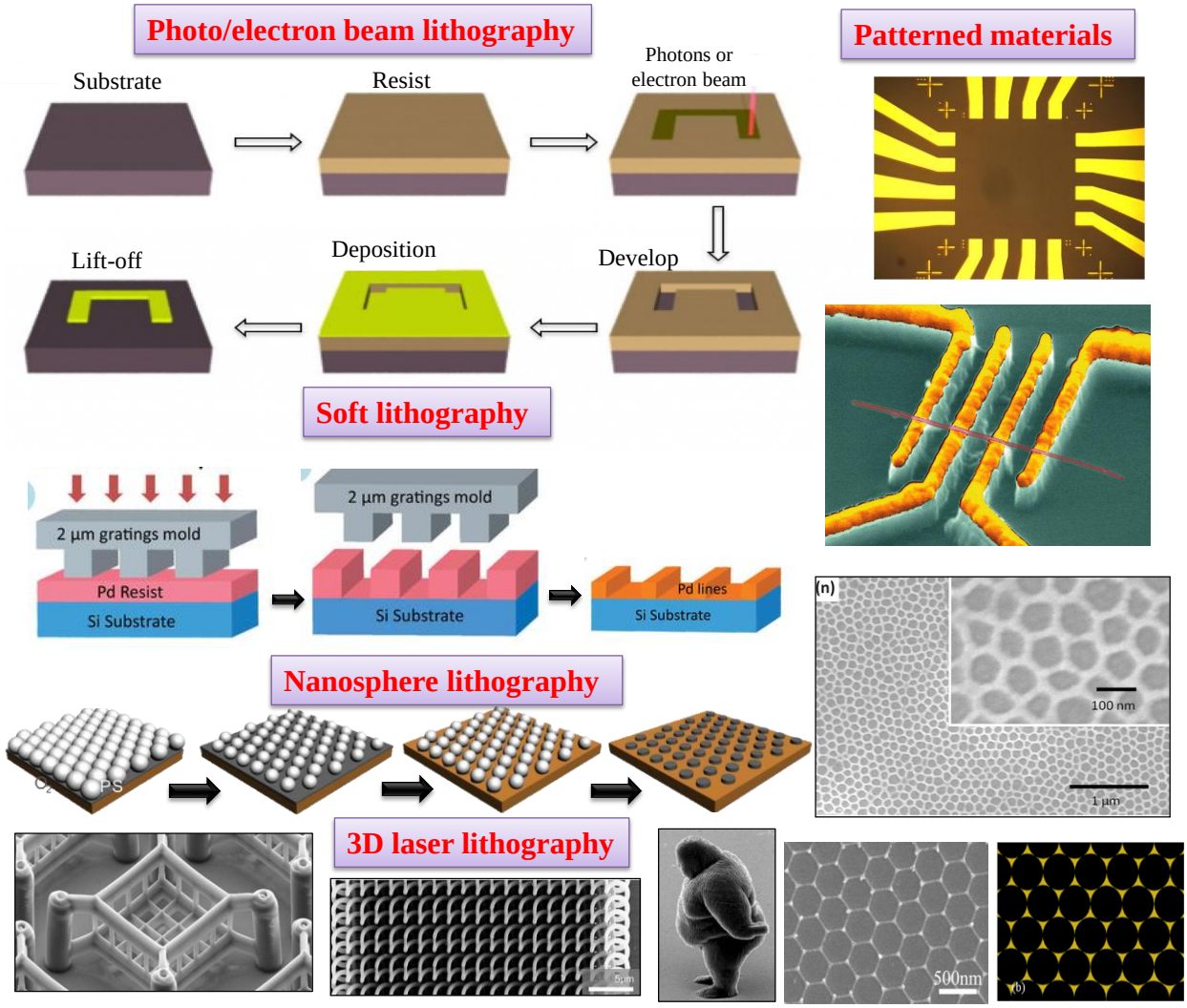

Figure I.3 Important lithography tools and recipes for patterning of materials.[23-27]

of photoresist may get either broken into smaller oligomers or get cross-linked in the exposed regions. In the lift-off process, the exposed photoresist was dipped in a developer solution, if the material from the exposed regions gets washed away; it is called a positive resist. In the case of negative resist, the exposed regions will get cross-linked and remain intact while the unexposed regions get washed away during the developing stage. Thus, the patterns on the photoresist can

be used as a protective layer in subsequent etching or deposition processes to create desired patterns on the substrate (see Figure 1.3).[28]

Photolithography can be performed in three different ways, namely contact printing, proximity printing and projection printing. The photomask is placed either in contact or in proximity to the photoresist. In projection printing, an optical lens system is used to project a deep-UV pattern from an excimer laser (wavelength of 193 or 248 nm) on the photoresist enabling pattern size reduction by 2-10 times. It is capable of fabricating high-resolution patterns as small as few tens of nanometers (~50 nm) at a high throughput (~50 wafers/hr). It has been employed in manufacturing of advanced ICs and CPU chips. In recent years, immersion lithography, resolution enhancement technology and extreme-UV lithography have been developed to improve the lithography resolution of projection printing.

Electron beam lithography: Electron beam lithography (EBL) utilizes electron beam instead of photons (photolithography) to achieve high resolution patterns due to small wavelength and a small probe size. It is a serial technique, capable of creating finer features for the fabrication of high density devices/circuits. The process steps involved in EBL are very much same as compared to that of photolithography (see Figure 1.3). Poly(methyl methacrlylate) (PMMA) has been the most widely used and high resolution positive tone resist and hydrogen silsesquioxane (HSQ), a relatively new resist material, is a high resolution negative tone resist. One of the most important parameter of the EBL process is the resolution of a resist, smallest line widths can be patterned consistently. Lower the molecular weight of the polymeric resist, higher is the resolution. The resolution is ultimately decided by the relation between the probe diameter and the interaction volume of the polymer. The resolution is also limited due to proximity effects and swelling of the polymer in the developing solvent, leading to the higher feature size than

expected.[29] To suppress the proximity effect, electron beam with higher energy can be used. EBL is not suitable for high-volume manufacturing because of its limited throughput. There has been significant interest in the development of multiple electron beam approaches to lithography in order to increase throughput.

Soft lithography: Soft lithography refers to a family of techniques for fabricating or replicating structures using "elastomeric stamps, molds, and conformable photomasks".It is called "soft" because it uses elastomeric materials, most notably Polydimethylsiloxane (PDMS). Unconventional soft lithography techniques, developed in 1993 by Whitesides group at Harvard University.[30] The soft lithography tool-kit comprises of the stamp, inks and substrates, of which the key element is the stamp. One of the most successful stamp materials is PDMS, also known as Sylgard 184. Soft lithography is similar to that of routinely used steal stamping, but here the patterned materials are in micro to nano sizes. Preparation of elastomeric stamp is the first step in the Soft lithography. In order to fabricate elastomeric stamp, PDMS is poured on top of desired mask and cured. Once the stamp is fabricated with the desired features, it can be used for many purposes such as molding, printing, embossing, imprinting etc (see Figure 1.3). Soft lithography has unique advantages such as low cost, clean room free operation, 3D patterning, non-planar surface patterning and well-suited for bio-applications.

Nanosphere lithography: Nanosphere lithography (NSL) is a promising inexpensive fabrication tool for producing regular and homogenous arrays of nanoparticles with different sizes. This method combines the advantages of both top-down and bottom-up approaches. The flat substrate is coated with a suspension containing monodispersed spherical colloids (e.g., polystyrene) after a chemical treatment to enhance its hydrophilic character. Upon drying, a hexagonal-close-packed (HCP) monolayer or bilayer, called a colloidal array mask, is formed. The capillary force

and convective transport of the nanospheres are the main factors that dominate the self-assembly process. While the ordering and quality of the obtained arrays is considerably affected by the rates of solvent evaporation. The mask formed during the self-assembly of the colloidal particles was directly used for metal deposition. In some cases, the colloidal particles were plasma/reactive ion etched before metal deposition to modify the patter dimensions. The subsequent removal of the mask (lift-off) by sonication in an adequate solvent or by stripping leaves an array of ordered nanodots on the surface of the substrate. These patterns find applications as localized surface plasmon resonators, SERS substrates or biosensors and solar cells.[31]

Other lithography methods

Stereo-lithography, multi-photon lithography, 3D laser lithography and direct wire lithography are the next generation lithography tools for advanced patterning of materials. All the above mentioned lithography techniques are process intensive and tedious. Most of these methods require sophisticated instruments, expensive setups and limited throughput. Nowadays, researchers are focusing on developing new lithography methods. One would ideally require a lithography method, which is simple, inexpensive, sub-micrometer features and scalable to large areas. More importantly, the process should be adoptable to flat, curved and rough surfaces with ease. In this thesis, efforts have been made to develop such lithography methods.

I.4 Nanoelectronics

Various nanostructures and large number of lithography tools as discussed so far have culminated to develop nanoelectonic devices, thus realizing enormous applications. Nanoelectronics refer to the use of nanomaterials in electronic components. The term covers a diverse set of devices and nanomaterials, which exploit inter-atomic interactions and quantum

mechanical properties, arising due to confinement effects.[32] Figure 1.4 shows few examples of nano-electronic devices, with relevant discussion.

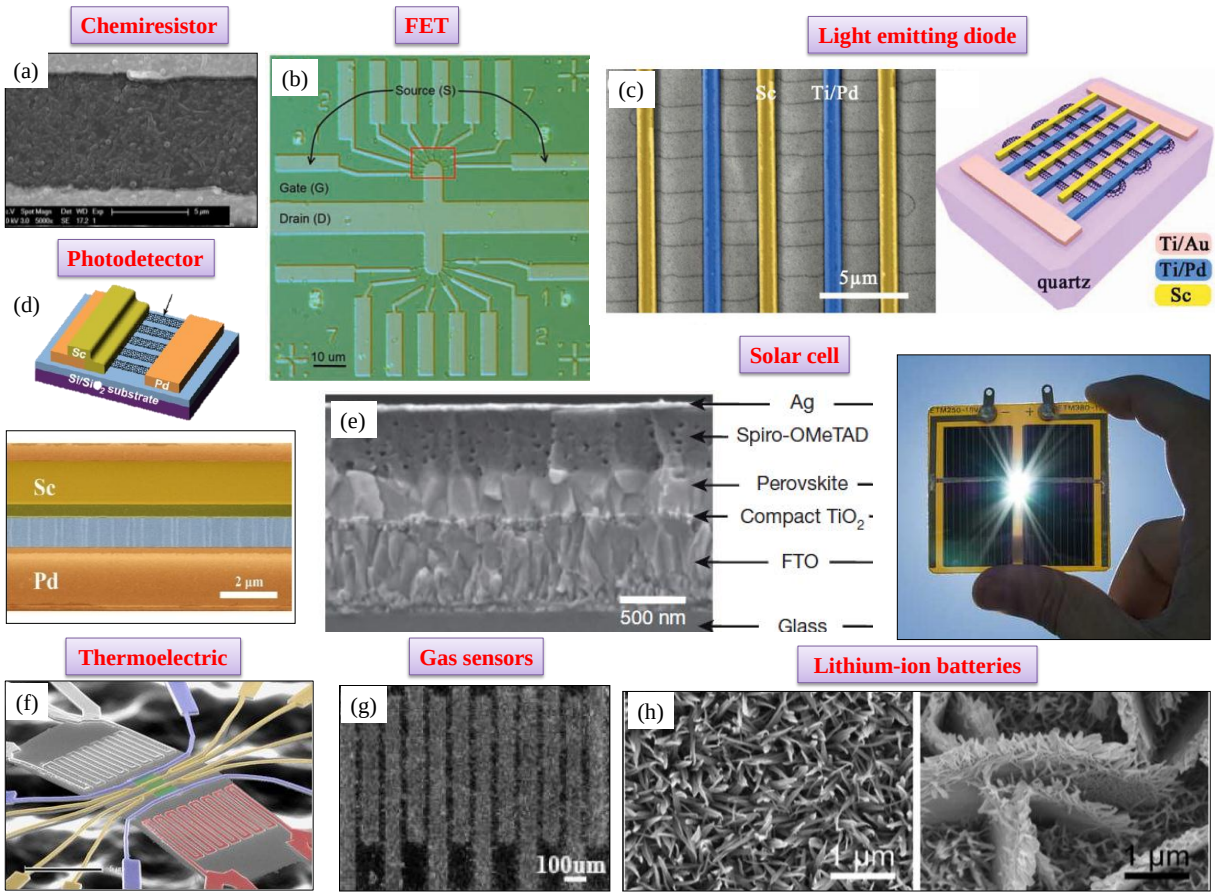

Figure I.4 Examples of various devices fabricated with nanomaterials.[33-40]

Chemiresistor: Chemiresistor is a sensor, which measures pH of a solution without using reference electrode. The resistance of device is the measure of change in pH value. The device is fabricated with oxidized single-walled carbon nanotubes (ox-SWNTs) functionalized with the conductive polymer poly(1-aminoanthracene) (PAA), spanning across the gap electrodes (see Figure 1.4a). The polymer contributes to the device selectivity, while the carbon nanotubes provide a sensitive and robust platform necessary to chemically stabilize the polymer. In keeping with the goal of creating a miniature, passively powered pH sensor, chemiresistor architecture is

preferred. Since the gate electrode is eliminated. Removing the reference electrode relieves the size limitation of this device. A smaller device can more easily be implanted at a location of interest inside the body.[33]

Field effect transistor: Carbon nanotubes (CNTs) have been shown to outperform conventional copper interconnects and silicon field-effect transistors (FETs) as individual devices. In Figure 1.4b, the optical micrograph of CNT FET demonstrates high-density device array and multidirectional device arrays, indicating the source, drain, and gate electrodes. Here FET is fabricated with semiconducting single walled carbon nanotube connected with Ti/Pd metal source and drain electrodes on top of a SiO_2/parylene dielectric. The FET showed ambipolar characteristics with high on-state conductance and on–off ratio (10^3), fast switching (2 $V.dec^{-1}$) and small hysteresis.[34]

Light emitting diode: Light emitting diode (LED) was fabricated with serpentine carbon nanotube on a quartz substrate. The CNT was connected with two asymmetric metal contacts which may connect directly to the conduction (Sc contact) and valence (Pd contact) bands of the CNT (see Figure 1.4c).The emission intensity of the device increases linearly with current. The LEDs are shown to outperform others due to the larger device current, higher emission intensity, and narrower emission bands which are all important for real optoelectronic applications of nanoscale light sources.[35]

Photodetectors: Light detection is a primary subject in optical sensing and is critical for a variety of industrial, military and scientific applications, including monitoring and controlling manufacturing process, optical communication, biological and military night time sensing. The device is fabricated by asymmetrically connections, the two ends of the SWCNT arrays with Pd and Sc of different work functions, followed by PMMA coating for passivation (see Figure

1.4d).This type of IR detector preserves the potential advantage desired for cost-effective, lightweight, and compact IR photodetectors, with additional advantages on simple device fabrication and un-cooled IR detection at room temperature.[36]

Perovskite solar cell: A perovskite solar cell is a type of solar cell which includes a perovskite absorber, most commonly a hybrid organic-inorganic lead or tin halide-based material, as the light-harvesting active layer. Figure 1.4e shows the cross sectional SEM image of vapour-deposited perovskite solar cells. The perovskite solar cells based on planar heterojunction thin-film architecture have a solar-to-electrical power conversion efficiency of over 15% with an open-circuit voltage of 1.07 V. One big challenge for perovskite solar cells is long-term stability. The water-solubility of the organic constituent of the absorber material make devices highly prone to rapid degradation in moist environments.[37]

Thermoelectric device: Thermoelectric devices convert heat (temperature differences) directly into electrical energy, using a phenomenon called Seebeck effect. Figure 1.4e shows the SEM image of thermoelectric device fabricated with p-doped Si nanowire array. The efficiency of the device was tuned with the doping level and the nanowire size. These devices currently find only niche applications such as on-chip heat recovery, cooling and power generation, because of their limited efficiency.[38]

Gas sensors: Solid-state gas sensors have wide applications in semiconductor processing, medical diagnosis, environmental sensing, personal safety, and national security. Gas sensor was fabricated with self-assembled SnO_2 nanowire on interdigitated electrodes as shown in Figure 1.4f. The sensor response increases with the hydrogen concentration and operating temperature. These devices have shown high sensitivity at low concentration of hydrogen ~10 ppm. The gas

sensor relies on surface reactions on nanowire, oxidation or reduction caused by different gas exposures.[39]

Lithium-ion batteries: Rechargeable lithium-ion batteries are the dominant power sources for numerous portable consumer electronic devices due to their advantages such as high energy density, long lifespan and environmental benignity. Hierarchical $Co_xMn_{3-x}O_4$ array micro-/nanostructures with tunable morphology and composition have been grown on conductive stainless steel as shown in Figure 1.4h. The hierarchical $Co_xMn_{3-x}O_4$ structures exhibit interesting electrochemical performance as integrated electrodes for lithium-ion batteries. The specific capacities are in the range of 540–207 mA h g^{-1}. These integrated functional materials may hold great promise for the construction of advanced electrodes for high performance energy storage devices.[40]

The above discussed devices are just a few examples of nanoelectronic devices. Still there is a quest to develop new type of devices and improve the performance of the existing devices. The improvement in the device performance not only involves development of novel materials but also synthesis of hierarchical structures incorporating composite materials. The devices can show enhanced performance because of new design and strategy adopted during fabrication.

Among all the nanomaterials ZnO stand out as one of the most versatile materials, due to their diverse properties and functionalities.[41] ZnO is a key technological material. ZnO is an attractive material for short-wavelength optoelectronic applications owing to its wide band gap 3.37 eV, large bond strength, and large exciton binding energy (60 meV) at room temperature. ZnO crystallizes in two main forms, hexagonal wurtzite and cubic zinc blende. Under general conditions, ZnO exhibits a hexagonal wurtzite structure. In addition, due to its non-

centrosymmetric crystallographic phase, ZnO shows the piezoelectric property. It is a versatile functional material that has a diverse group of growth morphologies, such as nanocombs, nanorings, nanohelixes, nanosprings, nanobelts, nanowires, nanocages and other complex morphologies.[41] ZnO is also biocompatible, biodegradable, and biosafe for medical and environmental applications. Due to their remarkable performance in electronics, optics, and

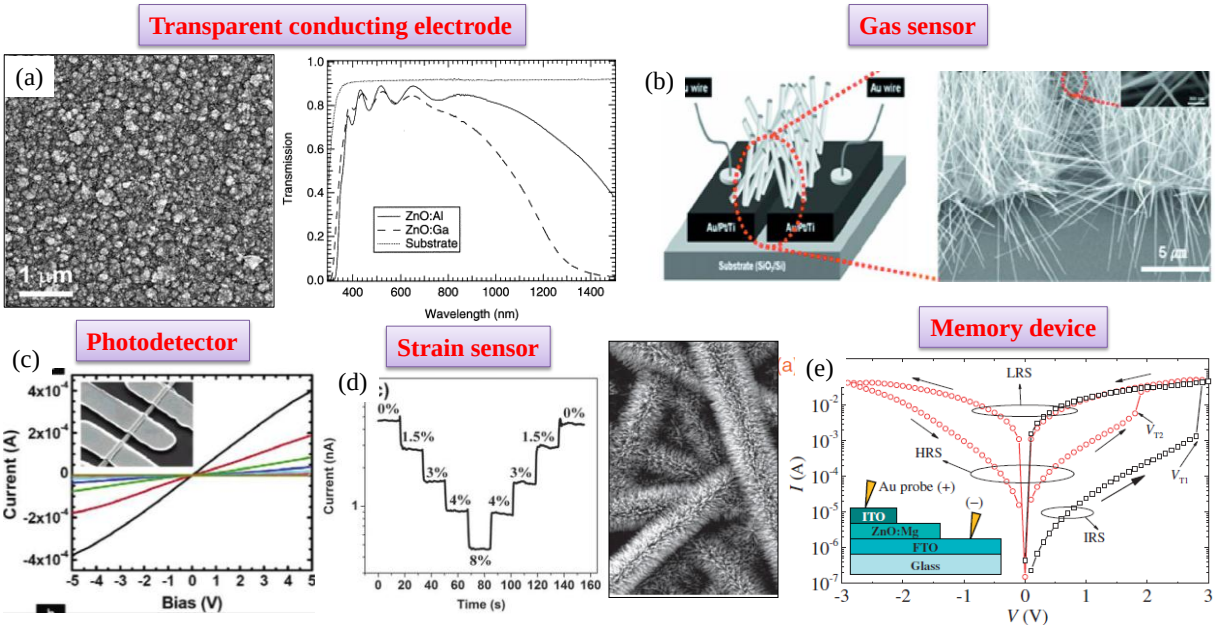

Figure I.5 A bunch of devices fabricated with ZnO nanostructures such a transparent conducting electrodes, gas sensor, photodetector, strain sensor and memory device.[42-46]

photonics, ZnO nanostructures are attractive candidates for many applications such as UV lasers, light-emitting diodes, solar cells, nanogenerators, gas sensors, strains sensor, photodetectors, memory devices and photocatalysts.[41] Few examples are depicted in Figure I.5.

ZnO is transparent to visible light and can be made highly conductive by doping. Several elements are doped in ZnO films, such as Al, Ga, F and so forth. Among them the most popular are Al-doped ZnO and Ga-doped ZnO because of better electrical conductivity. Figure I.5a shows the transmittance and SEM images of ZnO:Al and ZnO:Ga. Thus, ZnO thin film has been used as a transparent conducting electrode (TCE).[42] The growth of ZnO NWs can be done

even on bridging the gap between two pre-patterned Au catalysts (see Figure 1.5b). These NWs were used in NO_2 gas sensing at 225 °C. Gas sensitivity was found to be linearly proportional to the photoluminescence intensity of oxygen-vacancy-related defects.[43] Instead a bunch of ZnO NWs, single ZnO NWs devices were used as UV photodetectors as shown in Figure I.5c. These devices show extremely high photoconductive gain, attributed to the presence of oxygen-related hole-trap states at the NW surface.[44] On the other hand, ZnO NW/polystyrene nanofiber hybrid structures were used in a strain sensor as shown in Figure 1.5d. The device can withstand strain up to 50%, with high durability, fast response, and high gauge factors.[45] Finally, ZnO nanostructures have also been used in memory devices. A resistive switching based memory device is fabricated with Mg doped ZnO thin film. Due to the oxygen vacancy movements, two distinctive resistance states (0 and 1) were achieved, which were employed in resistive memory storage.[46] Thus, ZnO is a multi-functional material. Perhaps it is one material which is very cheap and used in wide variety of functional devices with simple fabrication recipes. Other comparable examples are TiO_2 and SnO_2. There is a quest for such multifunctional nanomaterials for usage in day-to-day devices.

I.5 Flexible nanoelectronics

Nanomaterials with given performance usually offer solution processability paving way to flexible electronic systems. Indeed, such systems represent some of the largest families of commercially produced nanomaterials today, and numerous commercial products based on nanoparticle formulations are widely available. Flexibility means many qualities: bendable, comfortably shaped, lightweight and non-breakable. The progress of flexible electronics has been driven primarily by the requirement of cheaper (such as ZnO, discussed above), large-area electronic devices that can be integrated on flexible substrates through low-temperature

deposition or solution processed methods. Although many promising results have been reported with organic semiconductors, the performance and lifetime of such devices suffer from low carrier mobility and poor chemical stability, which hinders their practical usage. On the other hand, inorganic semiconductors provide superior carrier mobility and chemical stability. However, the great challenge lies in integrating brittle inorganic semiconductors on flexible substrates, while preserving the structural and electronic properties. Figure 1.6 shows few examples of flexible nanoelectronic devices fabricated with organic and inorganic materials.

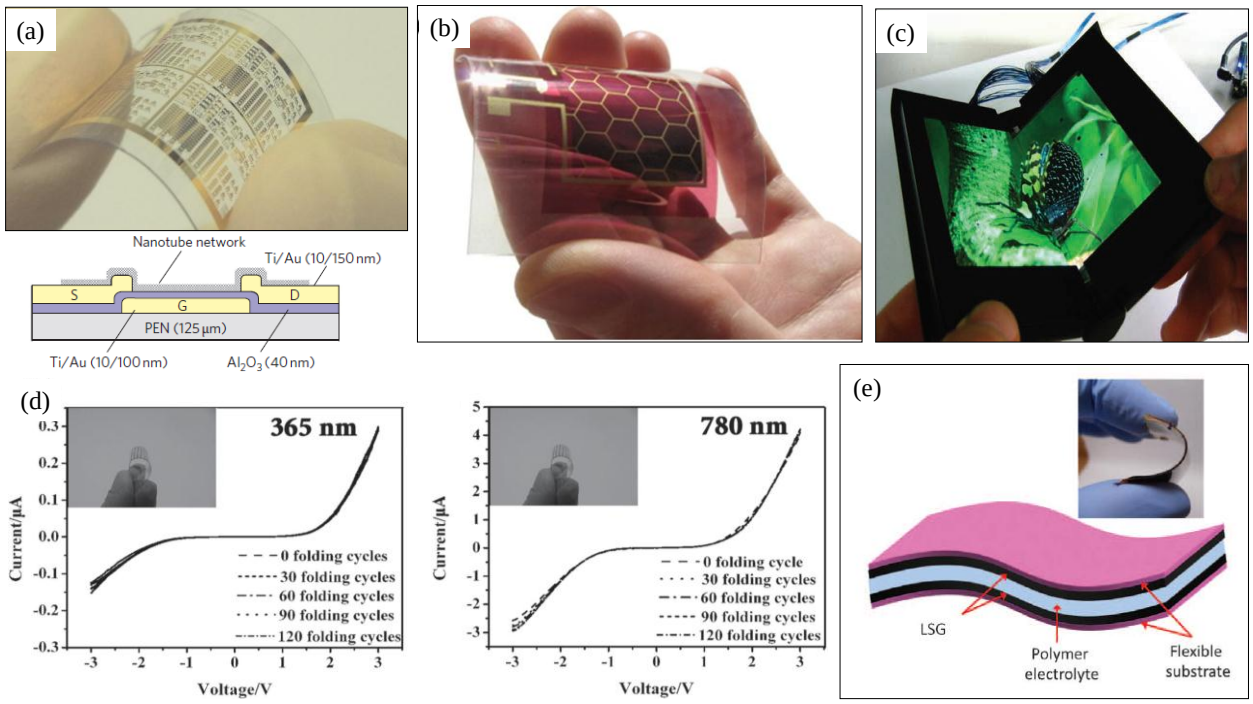

Figure I.6 Photographs and schematics of various flexible devices (a) field effect transistor, (b) polymer solar cell, (c) light emitting diode, (d) I-V characteristics of photodetector at 365 nm and 780 nm wavelength light and (e) electrochemical capacitor.[47-50]

The basic active devices of almost all the flat-panel displays and other applications, is thin-film transistor (TFT). For such applications, it is advantageous that the semiconductor material for the active layer be deposited on a plastic substrate using a fast and low-temperature process. Figure 1.6a shows a TFT fabricated with CNT films on flexible plastic substrate. The

transistors simultaneously demonstrate a mobility of 35 cm^2 V^{-1} s^{-1} and an on/off ratio of 6×10^6.[47] With the development of composite PEDOT:PSS/metal grid TCE on plastic substrate as an alternative to ITO, paved a way to flexible polymer solar cells. Figure 1.6b shows the flexible polymer solar cell fabricated with PEDOT:PSS/metal grid TCE and P3HT:PCBM as an active material. Light emitting diode is another important device, where the flexibility leads to development of bendable displays. Figure 1.6c shows photograph of a flexible organic light emitting diode (OLED) display device having a top emission structure.[48] In another case, organolead halide perovskites based photodetectors were fabricated on flexible substrate. In the photocurrent measurement, the photodetector has shown a broad photoresponse, ranging from 780 nm to 310 nm wavelength light. From the curves shown in Figure 1.6d, it can be seen clearly that the conductance of the device remains almost constant even after 120 cycles of bending. These results indicate the extreme flexibility, good folding endurance and electrical stability of the flexible device.[49] The practical usage of the flexible displays not only requires flexible OLEDs but also flexible batteries. Figure 1.6e shows a flexible super capacitor fabricated with laser-scribed graphene.[50] The flexibility is extended to all the devices in nanoelectronics. *With 'flexibility' in the modern day devices, comes the 'flexibility' in human life.*

I.6 Transparent nanoelectronics

An additional attribute, what one looks for in a functional device is some level of transparency. Transparent electronics is an emerging and promising technology for the next generation of optoelectronic devices; however this approach is even extended to non-optoelectronic devices. The transparent devices improve security system and facilitate electrical energy from the window panels, create visible space around the user. These devices find use in military applications and real-time wearable displays. A widely used method for making

transparent devices is to reduce the thickness of active material down to its optical absorption length, which may not be possible with all the devices. In practice, a transparent device demands active materials, electric contacts/connections, dielectric/passivation layers and carrier blocking layers etc., all to be transparent to the visible light, which is truly a challenge! Overcoming these hurdles, few transparent devices have been fabricated as depicted in Figure 1.7.

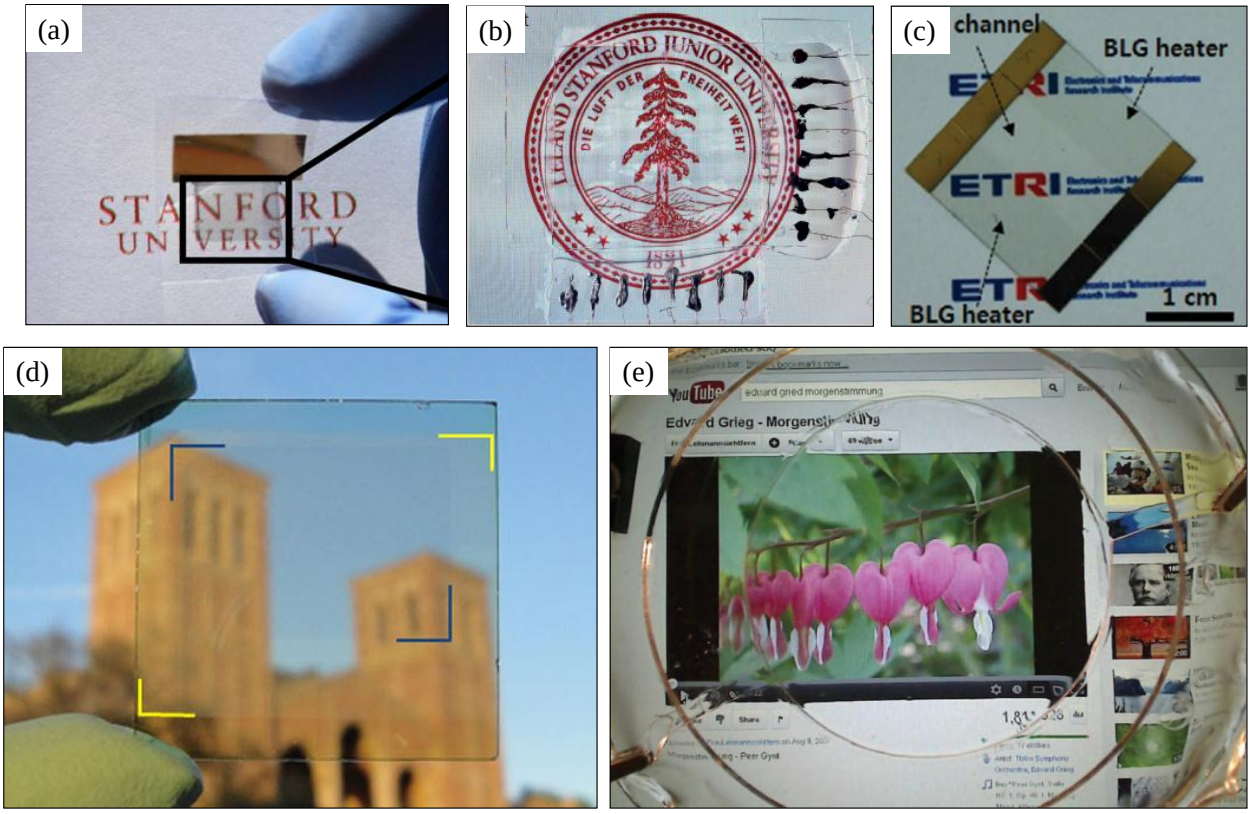

Figure I.7 Photographs of various transparent devices (a) battery, (b) strain sensor, (c) gas sensor, (d) polymer solar cell and (e) loud speaker.[51]

In order to bring transparency in portable electronics, one of the main constraints is to fabricate a transparent battery. Fabricating suitable transparent active materials for battery usage is a difficult task. Patterning active materials in form of grid like structures is a new approach. The battery appears transparent (see Figure 1.7a) as the patterned electrode materials cover only a small portion of the whole area and the pattern features are smaller than the detection limit of the human eye. Fabricated batteries showed transparency of 78, 60, and 30% and corresponding

energy density of 5, 10, and 20 Wh/L with packaging.[51] In another case, CNT network with thickness less than the optical absorption length was employed in strain sensor fabrication on an elastic substrate (see Figure 1.7c).[52] A transparent gas sensor on the other hand, requires not only transparent active materials but also a transparent heater; the latter is used generally to enhance the sensing performance of the active material. For this purpose, gas sensors are fabricated with single layer/ double layer graphene, serving as gas sensor and transparent heater. The graphene based gas sensor has shown NO_2 gas sensing with fast response and sensitivity even at low concentrations.[53] There are few attempts in the literature to fabricate transparent polymer solar cell. Figure 1.7d shows a photograph of a transparent polymer solar cell from the literature. The optimized devices have a maximum transparency of 66% at 550 nm with 4% power conversion efficiency.[54] Transparent loud speaker is a recent example for transparent electronics. The device is fabricated with hydrogel TCEs and elastomeric dielectric, and is highly

I.7 Roll-to-roll processing in Nanoelectronics

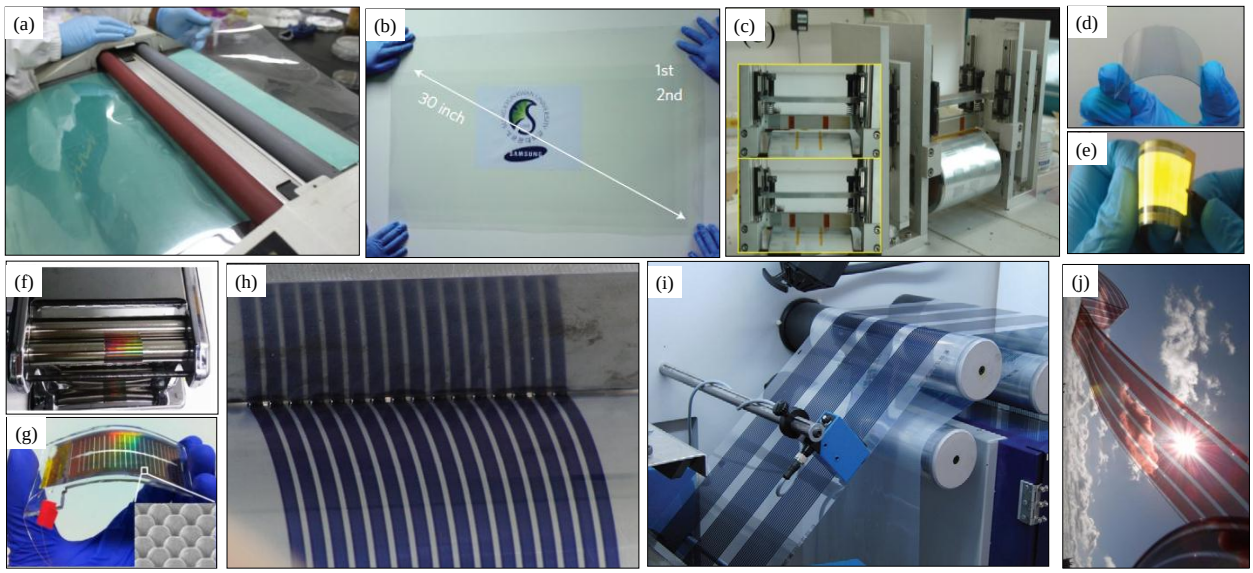

Figure I.8 Photographs of various roll-to-roll fabrication setups and large area devices (a), (b) graphene TCEs, (c)-(e) organic light emitting didoes, (f), (g) amorphous Si solar cells and (h)-(j) polymer solar cells.[56-59]

transparent as shown in Figure 1.7e.[55] These are few examples of transparent devices fabricated in the literature. The surge of transforming all opaque nanoelectronic devices into transparent devices is on. This thesis attempts to provide a meaningful solution towards this end.

Technological advances in nanoelectronic devices are taking place at very fast rate. In order to meet the criteria of low cost fabrication and high throughput, roll-to-roll fabrication is essential. Roll-to-roll processing, also known as web processing, reel-to-reel processing or R2R, is the process of creating electronic devices on a roll of flexible plastic or metal foil. The roll-to-roll cohesive coating system utilizes only natural gravity and the surface tension of the solution to flow out from the capillary to the surface of the substrate. The general fabrication methods of spin coating and high vacuum thermal evaporation are not compatible with large area roll-to-roll (R2R) processing. The large area processing requires environment benign solvents, fabrication in environmental conditions and uniform performance of the devices from one end of the roll to the other. As a consequence large area devices have shown less performance as compared to small area devices (few mm^2 areas). In the recent past, there have been continuous efforts to fabricate large area R2R processed devices, some examples are shown in Figure I.8.

Figures 1.8a and 8b show roll-to-roll production and wet-chemical doping of predominantly monolayer 30-inch graphene films grown by chemical vapour deposition onto flexible copper substrates. The films have sheet resistances as low as ~125 Ω/sq with 97.4% optical transmittance. The flexibility of the graphene and copper foils further allowed efficient etching and transfer processes that use a cost- and time-effective roll-to-roll production method.[56] The roll-to-roll cohesive coating enables coating of nanoscale thin films with fine control by modification of the surface energy and without wasting the solution. This paved a way for roll-to-roll fabrication of polymer light-emitting diodes using indium tin oxide-PET as a TCE

(Figure 1.8c and 8d). The optimized maximum current and power efficiencies of the device are around 6.1 cd/A and 5.1 l m/W, respectively, which are comparable to ITO-glass based device in few mm^2 areas.[57] In another case, as shown in Figure 1.8f and 8g, regular arrays of 3-D nano-spikes were fabricated using nanoimprint lithography on flexible aluminum foil with a roll-to-roll compatible process.[58] These structures facilitated in improving the performance of amorphous-Si solar cells. The organic solar cells (OSCs) have huge potential to enable roll-to-roll production over ultra-large areas. Figure 1.8h and 8i shows the photographs of mass production of organic solar cells during slot-die coating of the active layer. Thus fabricated ultra-large area OSCs photograph is shown in Figure 1.8j. Here, power conversion efficiencies are ~1.8%.[59] In order to see OSCs as a matured technology, more effort must be directed towards large area fabrication.

I.8 Objective and outline of the thesis

The overall objective of the thesis work was to realize stand-alone devices using nanomaterials. Two important device types have been considered, namely transparent conductors and multi-level memory switches. The methodologies attempted in this thesis have been focused on the following factors- low infrastructural, power and material requirements involving few, environmentally benign process steps, all ensuring low cost fabrication. Large area fabrication on flexible substrates, employing self-assembly approaches where applicable, are additional factors that have been given due attention without compromising on reliability and uniform performance parameters. Three important fabrication recipes have been realized, namely metal wire network derived TCEs via crackle lithography, resistive switching for multi-bit memory devices by electroforming and selective soldering of CNTs via self-assembly.

Chapter-II deals with characterization tools and techniques used in the thesis. **Chapter-III** is focused on fabrication of next generation TCEs. Here, a colloidal dispersion was made to evaporate spontaneously in the form of a film, producing uniforms and interconnected cracks over large areas. The cracked film has been used as a sacrificial template for various metal depositions, which following lift-off, yielded metal wire network derived TCEs. A broad spectrum of flexible and transparent devices has been realized with these TCEs**. Chapter-IV** deals with fabrication of new type of resistive switching memory devices based on chemically grown PdO thin films. Following integration and 'forming', the device showed multi-level resistive switching with high level of endurance and retention. **Chapter-V** is focused on making CNT circuits by soldering CNTs across gap electrodes in a lithography-free manner. For this purpose, the soldering precursor was self-assembled on Au electrodes. The CNTs were soldered by joule heating as well as external heating. The soldered CNTs formed ohmic contact with the electrode; these contacts are robust and flexible. The following thesis chapters contains detailed introduction to each of these topics and related discussion of results obtained as well as critical analysis and comparison with the literature. **Chapter-VI** presents over view and future outlook for the thesis.

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Chapter II

Characterization techniques

Several spectroscopic and microscopic techniques have been used to characterize the prepared samples reported in this thesis. In the following paragraphs, the details of instruments used and the sample preparation methods are described.

Scanning electron microscope (SEM): Scanning electron microscopy (SEM) measurements were performed using a Nova NanoSEM 600 equipment (FEI Co., The Netherlands). Energy dispersive spectroscopic (EDS) mapping was performed using EDAX Genesis V4.52 (USA) attached to the SEM column. The EDS mapping was performed at 10 kV (energy window, 10 eV) with a beam current of 1.1 nA.

Transmission electron microscope (TEM): Transmission electron microscopy (TEM) measurements were carried out with a JEOL-3010 instrument operating at 300 kV (λ= 0.0196 Å) and selected area electron diffraction (SAED) patterns were collected at a camera length 20 cm (calibrated with respect to the standard polycrystalline Au thin film). Samples for TEM were prepared by depositing a drop of the nanomaterial on a holey carbon copper grid, allowing it to dry in a desiccator overnight. The carbonaceous platforms have been performed on the holey carbon film of the Cu TEM grid. This grid was used for TEM and selected area electron diffraction (SAED) analysis.

Atomic force microscopy (AFM): Atomic force microscopy (AFM) experiments were carried out using Veeco diInnova SPM with Nanodrive controller. Tapping and contact (lateral force) mode imaging was carried out using standard etched Si or Si_3N_4 cantilevers, respectively. The scanner was calibrated using a standard Pt coated Au grid with a pitch of 1 μm. Both height and deflection/amplitude information were recorded at a scan rate of 1 Hz, and stored in a 512x512

pixel format. Both intermittent contact (dynamic AFM) and direct contact scanning modes were used. Images were processed using the Nanoscope version 7.15 software.

Optical and stylus profiler: For film thickness measurements, a Wyko NT9100 (Veeco, USA) optical profiler (OP) and a stylus profiler Dektak 6M (Veeco, USA) were used. In OP, the vertical scanning interferometry (VSI) for roughness of samples more than 160 nm and phase shifting interferometry (PSI) mode for roughness of samples less than 160 nm were employed with a field of view and objective lens magnifications from 0.5x – 2x and 5x – 50x respectively.

X-ray photoelectron spectroscopy (XPS): X-ray photoelectron spectroscopy (XPS) was carried out with OMICRON spectrophotometer (1x10-10 Torr vacuum) with nonchromatic X-ray source of Al Kα (E =1486.6 eV). Samples for XPS (solid substrates) were mounted on the stub using high vacuum compatible Ag paint and drying in a vacuum.

UV-Vis and IR: UV-visible spectra were recorded using a Perkin-Elmer Lambda 900 UV/vis/NIR spectrophotometer. The photoluminescence (PL) spectra were taken with different excitation wavelength from the spectroflurometer. PL was measured on Perkin- Elmer LS55 Luminescence spectrometer. Fourier transform infrared (FTIR) measurements were done using a Bruker IFS66v/s spectrometer with a resolution of ~ 2 cm^{-1}.

Optical and confocal microscopes: The optical images were procured with the microscope of Laben, India with a zoom-in lens of 100x. The images were captured using pixel link software. The confocal images were taken by using a Zeiss LSM 510 laser scanning confocal microscope at different excitation wavelengths.

X-ray diffraction (XRD): Powder X-ray diffraction measurements were performed using a Siemens Seifert 3000TT diffractometer employing Cu Kα (λ = 1.5406 Å) radiation. Samples were prepared by depositing the materials in the form of films on glass slides and typical scan

rate was 1 deg.min-1. The X-ray tube was set at 40 kV and 30 mA. With a receiving slit of 0.3 mm wide and a scintillation counter as detector, the θ -2θ scans were performed.

High-purity silicon powder was used as an internal standard. The coherently diffracting crystallographic domain size (D) of the nanoparticles was calculated from X-ray diffraction (XRD) line broadening after subtracting the contribution from the Cu Kα component (Rachinger correction) and correcting for the instrumental width. The integral line width was used in the Scherrer formula to calculated XRD of the high intensity peak.

$$D = 0.9\lambda/\beta\cos\theta$$

where λ is the wavelength of the X-ray beam, β is the angular width at the half-maximum intensity and θ is the Bragg angle.[1]

Reference

[1] B. D. Cullity and S. R. Stock, Elements of X-Ray Diffraction, Prentice-Hall Inc., 2001.

Chapter III

IIIA: Fabrication of Transparent conducting electrodes

Summary

In optoelectronics, a competent alternate to the expensive and brittle indium-tin-oxide (ITO), is the need of the hour. This study is focused on developing an extremely simple, three step process of filling networked crackles formed in a dried colloidal layer, with a desired metal to produce *metal in crackle pattern* (MCP) based transparent conducting electrode (TCE). By design, TCE consists of a single metal micro/nanowire network with extremely smooth surface (roughness, ~ 9 nm) and seamless junctions over several tens of cm^2 area on common substrates such as glass. This method allows fabricating TCE even on curved surfaces such as a quartz tube. The metal can be deposited either by physical methods or by solution processed method. MCPs with M as Au, Ag, Cu, Pd, Al, and Zn as well as of Au and Al over Cu have been prepared. The TCEs are high performing; a sheet resistance of ~ 2.4 Ω/sq at ~ 90% (550 nm) transmittance has been achieved, AuCP/quartz showed high transmittance even in UV and IR regions. While MCP on polyethylene-terephalate (PET) produced a flexible and highly robust as well as chemically stable TCE.

IIIA.1 Introduction

Light transmission through a material requires a band gap spanning visible wavelengths, which is inherently opposed to what electrical transport requires. Meeting these contrasting properties in a single material, commonly referred to as transparent conducting electrode (TCE), is rather rare. Indium oxide optimally doped with tin (ITO) is unique in this respect. It retains its optical band gap (~ 4 eV) yet exhibits high conductance arising because of tin donating electrons to the conduction band.[1] A well-prepared ITO film can transmit up to ~ 92% of visible light

and show a sheet resistance (R_s) of ~ 10 Ω/sq, which explains its widespread use as electrode material in display devices. In recent years, as In is fast depleting on earth[2] and price steadily increasing, many alternatives such as fluorine doped tin oxide (FTO),[3]doped ZnO[4] and other oxide systems[5,6] have been explored but their performance can suit only certain applications. Oxides are poor IR and UV transmitters[7] and are brittle, not suitable for flexible applications.[8] Given these issues, the search for substitutes is a great deal of activity in the literature.[8,9] An attractive alternate is graphene;[10] however, obtaining extended layers of graphene can be process intensive and cost forbidding.[11] The organic equivalent to ITO is poly(3,4-ethylenedioxythiophene) (PEDOT) and its derivatives, but they suffer from limited conductivity and stability besides being expensive.[12]

An alternate approach is to decouple the contrasting properties namely transmittance in the relevant wavelength range and electrical conduction. Thus, TCEs have been realized by creating networks of carbon nanotubes (CNTs)[13,14] and metal nanowires[15-19]on substrates such as glass and polyethylene terephthalate (PET). Electrical conduction through the network of discrete objects is, however, percolation limited[20] and contact resistance dominating.[21-23] With this, arise issues related to increased absorbance and surface roughness often from redundant wires that are not part of the network.[24] High electrode roughness can cause electrical shunts in thin film devices such as polymer solar cells.[25] These issues have been compromised by thermal[26] or electrical current[27] induced annealing, mechanically pressing[17,24] or by acid treating[21,28] the nanowire/tube junctions. What is desirable is a process, which ensures high degree of wire connectivity with minimal surface roughness.

Fabrication of metal network in the form of a mesh has recently emerged out as a new approach to overcome these issues.[19] Recently, grain boundary lithography[29] has been

employed for the fabrication of random nanostructured Au mesh. Growth patterns of sodium carbonate crystals have been used as template for the fabrication of Ag metal network.[30] Similarly, self-assembled surfactant bubbles have served as template for Ag mesh based TCE.[31] Unfortunately, realizing large area TCE using these methods is rather difficult due to limited extension of the templates.[32-36]

IIIA.2 Scope of the present investigation

The quest is to develop a simple and inexpensive lithography, particularly for the fabrication of large area transparent conducting electrodes. This study explores the possibility of developing crack based templates, capable of hosting highly interconnected narrow cracks for metal deposition. For large area device applications using metal wire networks, it is important that the cracks in the template are of suitable dimensions, highly interconnected into a single network. The fabrication of crackle template on various substrates and surfaces is crucial for the fabrication of optoelectronic devices. Attempts have been made to use crackle templates for various metal deposition and fabricated TCEs with different work functions.

IIIA.3 Experimental Section

Fabrication of transparent conducting electrode: Colloidal systems such as coffee fine powder and TiO_2, SiO_2 nanoparticles, which are known to crack spontaneously upon drying, were explored as sacrificial layers. Among all, an acrylic resin water based dispersion available commercially as crackle nail polish [37] (Ming Ni Cosmetics Co., Guangzhou, China) was found adequate, after treatment. Dispersion in water/diluter (0.3 g/ml) was rigorously ultrasonicated for 30 min before filtering using Whatman filter (1 μm GF/B w/GMF). The filtrate was left overnight in an air-tight bottle. The suspended solution was extracted as needed and ultrasonicated prior to drop or rod coating on a substrate. Commonly available glass and quartz

plates and PET sheets (125 µm thickness) were used as substrates after washing with water, acetone and isopropyl alcohol and purging with nitrogen. K control coater from RK print coat instruments (UK) was used for rod coating. Electron beam evaporation (Telemark, USA) or physical vapour deposition system (Hind High Vacuum Co., India) were used for deposition of metals.

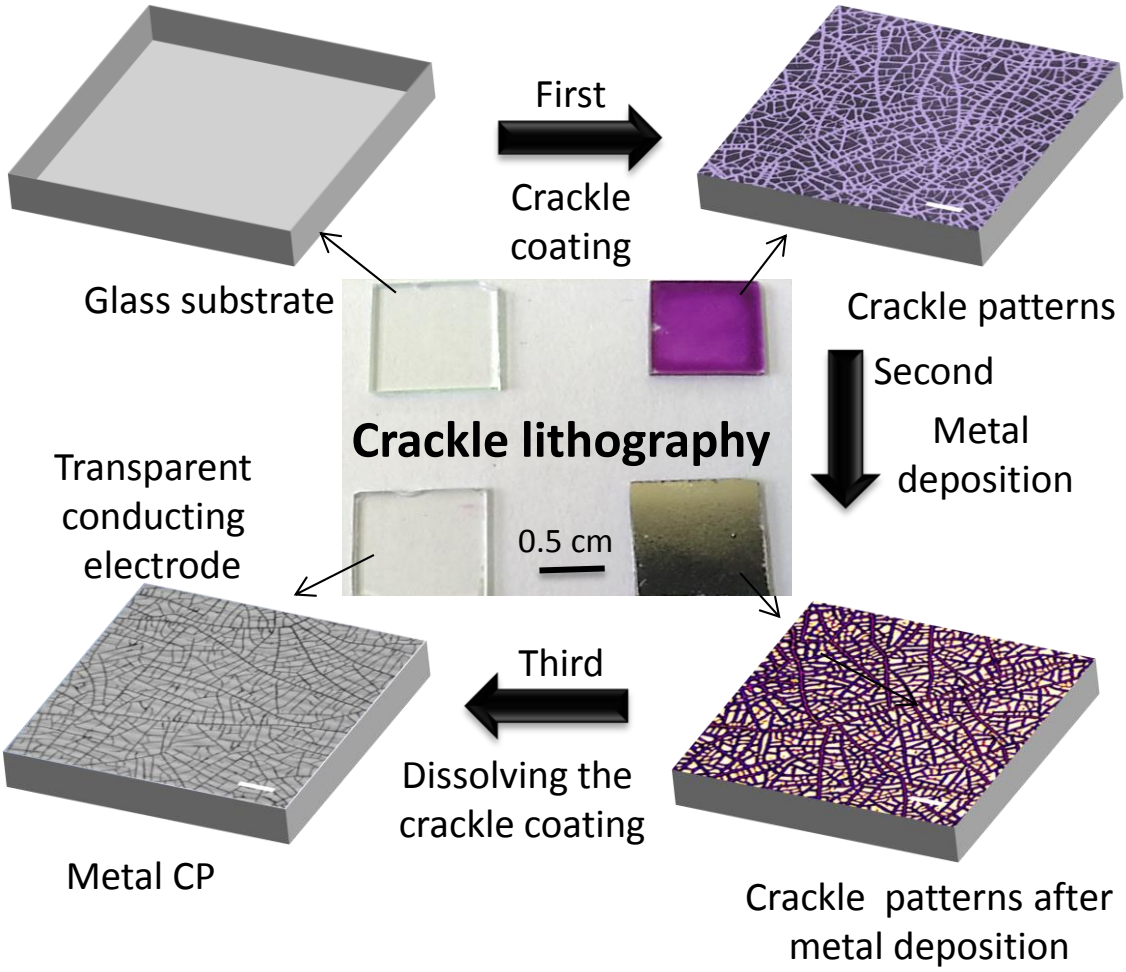

Figure IIIA: Schematic illustrates fabrication of a transparent conducting electrode. A digital photograph of the substrates during crackle lithography is shown at the center.

As shown in the schematic (Figure IIIA), a clean substrate is taken and a crackle polymer (as described above) in solution form is spin coated/rod coated/drop coated on glass substrate. After solvent evaporation, spontaneously interconnected crackles get formed from one end of the substrate to other end. In the second step, a desired metal is deposited by vacuum evaporation.

The crackle film is then dissolved in chloroform. After dissolving, a network of interconnected wires of the deposited metal are formed throughout the substrate. The metal networks are highly interconnected throughout substrate without breaks. The digital image of a clean glass, crackle patterned glass, subsequently metal deposited glass and the glass substrate after dissolving the polymer is shown at the center of the schematic. The glass substrate with metal network after crackle lithography is nearly as transparent as glass with conductivity similar to the metal.

Characterization of transparent conducting electrode: The following are the characterization tools used for all the measurements in Part-IIIA and IIIB. Transmittance was measured using a Perkin−Elmer Lambda 900 UV/visible/near-IR spectrophotometer. Sheet resistance was measured using a 4-Point Probe Station (Jandel Model RM3, London and Techno Science Instruments, India). Current–voltage measurements were performed using a source and measurement unit (Keithley 236). Low temperature measurements were done using THMS600 stage (Linkam Scientific Instruments Ltd., UK). SEM was carried out using a Nova NanoSEM 600 instrument (FEI Co., The Netherlands). Energy-dispersive spectroscopy (EDS) analysis was performed with an EDAX Genesis instrument (Mahwah, NJ) attached to the SEM column. AFM measurements were performed using di Innova (Bruker, USA) in contact mode. Standard Si cantilevers were used for normal topography imaging. Wyko NT9100 Optical Profiling System (Bruker, USA) was used for height and depth measurements. ImageJ software was used to perform analysis of the crackle patterns. Flexibility test was done using an automated Mechmesin Multitest 2.5i unit (UK). In-situ thermal images of the TCEs while applying voltage was captured using a thermal imager (Testo 885-2, USA) with 640×480 pixels, thermal sensitivity of 0.03 °C, 30° field of view covering long wavelength infrared spectral range of 8-14 µm. The imager also provides relative surface humidity maps based on the ambient temperature,

humidity and surface temperature values. The thermal images were acquired from the back side of the electrodes. The data points for temperature profile were obtained from the clip recorded during the measurement. A digital multimeter with DMM Viewer was used for recording the resistance changes with time.

IIIA.4 Results and discussion

The crack template formation is illustrated in Figure IIIA.1. A colloidal dispersion of an acrylic resin was drop coated on a glass substrate (Figure IIIA.1a). The dispersion contained particles of diameter ~ 40 - 80 nm (see Figure IIIA.1b). Initially (t = 0 s), the colloidal dispersion forms a non-uniform and unsteady thick deposit (see Figure IIIA.1c) which just after 180 s, settles into a relatively uniform film. In the following minutes as the drying process sets in, the colloidal film begins to crack. Initial cracks which appear around 240 s, tend to spread and crosslink within the next 30 s. Under the given conditions, the crack width is found to increase linearly at a rate, R_1 of ~ 0.5 μm/s initially and after a while (15 s), the rate decreased to R_2 of ~ 0.1 μm/s (Figure IIIA.1d). It is well known in the literature that colloidal dispersions upon drying on a substrate tend to crack due to the interfacial stress as the particle-particle and particle-substrate adhesion forces limit the drying layer from shrinkage.[38-41] The nature of crack network depends crucially on the uniformity of the layer thickness and also on the size, shape, and hardness of the colloidal particles. Hard particles are expected to produce broad cracks, while a layer containing soft particles may not crack at all.[42] Acrylic resin particle dispersion (see Figure IIIA.1b) used in this study, comes with the desired properties thus producing a highly interconnected crack pattern over large area (see Figure IIIA.1e and Figure IIIA.2). This is generally not true of other commonly used colloidal dispersions. This important aspect becomes clear during the fabrication steps, discussed in detail at a later stage.

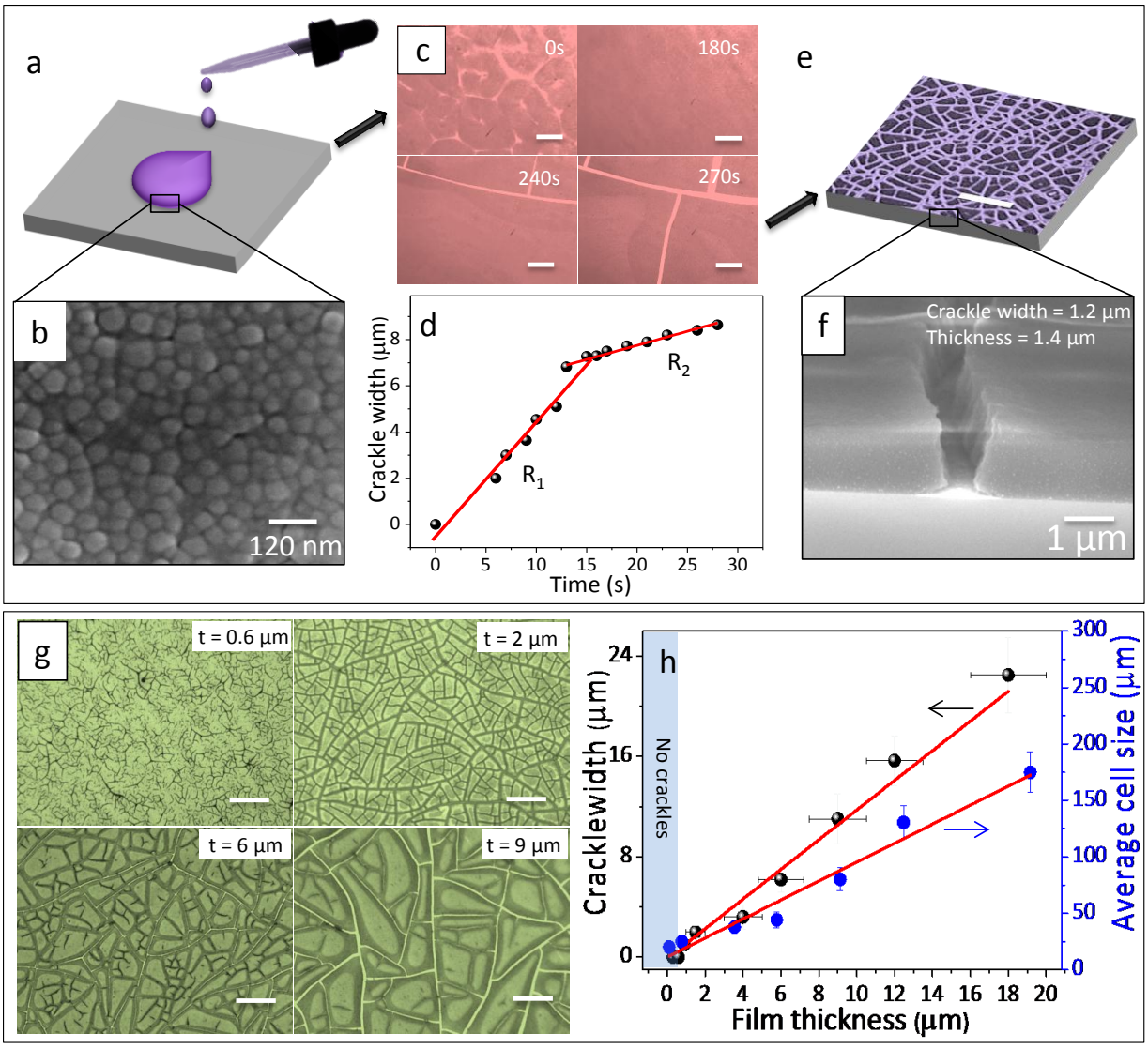

Figure IIIA.1 (a) Schematic illustration of crackle dispersion being drop coated on glass. (b) SEM image of acrylic resin nanoparticles (average diameter, ~ 40 to 80 nm) present in crackle solution. (c) Optical micrographs of crackle patterns during drying, for t = 0, 180, 240 and 270 s, respectively. Scale bar, 50 µm. (d) Variation in crackle width with time, red lines are linear fits for experimental data (solid circles). (e) Optical micrograph of crackle patterns after complete drying. Scale bar, 50 µm. (f) Tilt SEM image showing a crackled region. (g) Optical micrographs of crackle template of four different thicknesses. Scale bar, 100 µm. (h) Crackle width and average cell side as a function of crackle film thickness; red lines are linear fits to the data. The average cell side is square root of the average (polygonal) cell area.

The trend seen in Figure IIIA.1d may be related to diminishing stress as cracks grow and get interconnected into closed polygonal cells. The slope of the plot in Figure IIIA.1d is directly proportional to rate of evaporation of solvent i.e release of stress in the film. Initially rate of evaporation of an individual crackle is high (high slope, R_1) before it interconnects with the other

crackle, after the interconnection, the rate of evaporation decreases (less slope, R_2). A sharp jump in the slope is observed due to the interconnection of the crackles. The cracks appear as U-shaped grooves (Figure IIIA.1f), importantly, with no residual layer at the bottom, which is crucial for lithography. Therefore, more appropriately referred them as crackles. In crackle lithography, the crackle network is used as a template for deposition by vacuum evaporation or other methods, to produce a Material in Crackle Pattern (MCP). The crack width and spacing in the template are variables; they depend on the thickness of the drying layer, which is well known in the literature.[38, 39] In the given instance, no well-defined cracks were seen for thicknesses up to 700 nm, which is the critical thickness (see Figures IIIA.1g and 1h). With increase in the layer thickness, both the crackle width and spacing (cell side) increased linearly (Figure IIIA.1h and Table IIIA.1). Importantly bove the critical layer thickness, the crackle interconnectivity was always to be found (see Figure IIIA.1g).

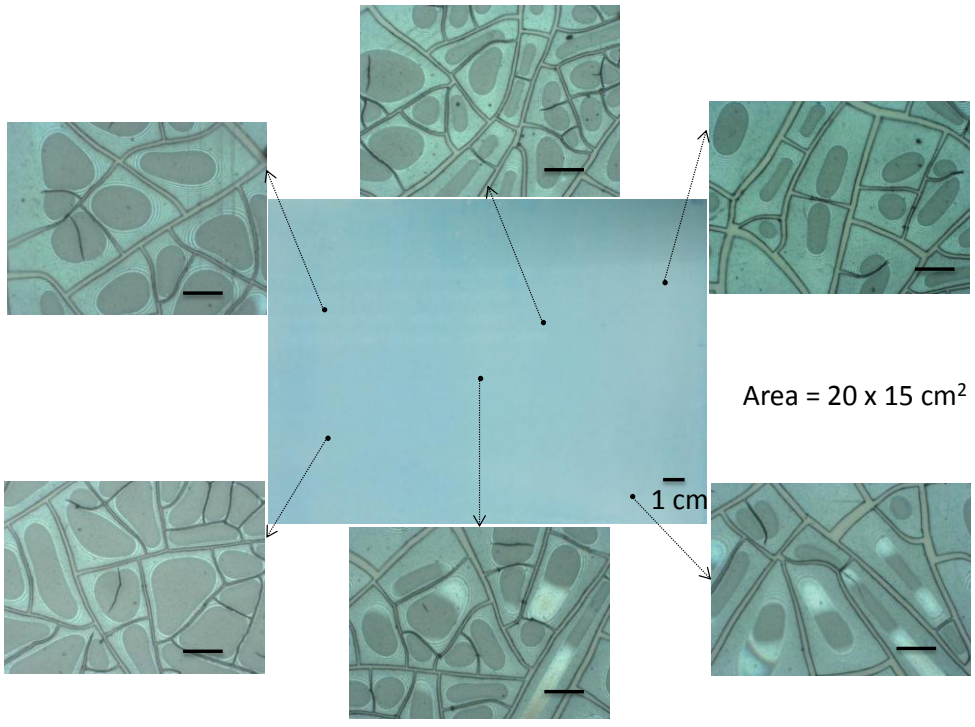

Figure IIIA.2 Photograph of crackle template on PET sheet over 20 × 15 cm^2 area, surrounded by optical micrographs taken at random locations indicated with black dots (scale bar 50 µm).

Table IIIA.1

Optimization parameters for crack template formation: varying crack widths and average cell sizes.

S.No.	Drop coating volume (µl) concentration (0.3 g/ml)	Average Crack width (~µm)	Average cell size (~µm)	Film thickness (~µm)
1	20	2	25	1.0
2	30	3.2	38	1.6
3	40	4.1	40	2.5
4	50	6.2	45	4.0

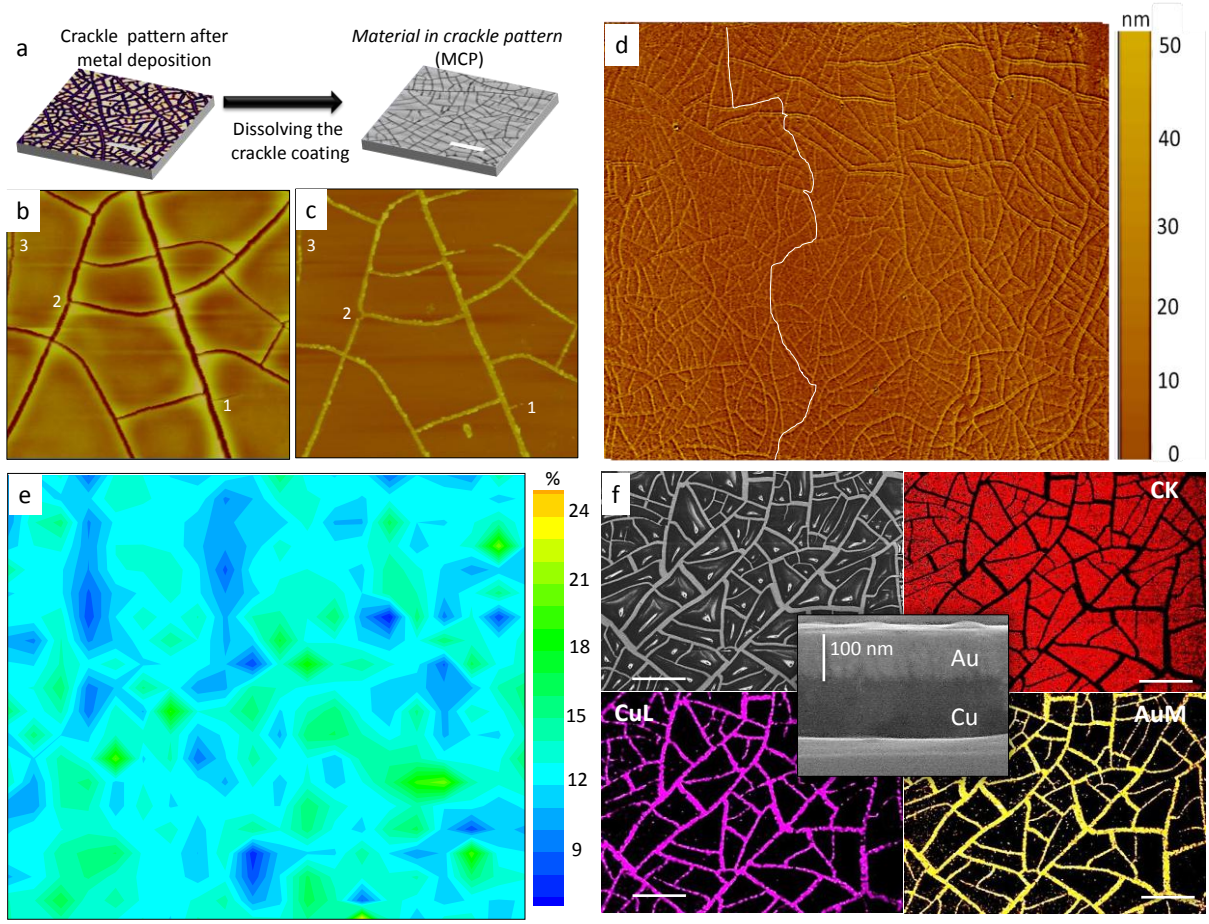

Figure IIIA.3 (a) Schematic illustration of the lift-off process using optical microscopy images after metal deposition (left) and after dissolving away the crackle layer in chloroform (right). Scale bar, 50 µm. AFM topography images (80 x 80 μm^2) of (b) the crackle pattern for a layer thickness of ~ 950 nm, and (c) Au in crackle pattern (AuCP). (d) Optical profilometric image of AuCP/glass over 1.1 x 1.3 mm^2 area. White line traces a single wire across the image area. (e) Spatial distribution of the 2D metal fill factor (in %) estimated from 400 SEM images (each, 60 x 60 μm^2) covering 1.2 x 1.2 mm^2 area of a AuCP/PET. (f) SEM image and EDS maps from the same region corresponding to CK, CuL and AuM levels from a hybrid electrode, Au-Cu/PET. Scale bar, 100 µm. Note: As the substrates are insulating, SEM images show unusually bright contrast. The inset in the center shows cross sectional image of the hybrid structure.

The effectiveness of the crackled layer as a template in lithography is demonstrated by vacuum depositing Au (100 nm thick) as an example. Following lift-off in chloroform produced an interconnected Au wire network on glass (Figure IIIA.3a), briefly AuCP/glass. From the AFM topography images, observed Au wire network (Figure IIIA.3c) appears very similar to the crackle pattern (Figure IIIA.3b). For instance, the small notches formed in the crackle pattern denoted by '1' and '2' in Figure IIIA.3b, are seen neatly replicated in the Au network (Figure IIIA.3c) along with a narrow crackle (~ 900 nm) marked as '3'. If the two images are overlaid (see Figure IIIA.4), it becomes apparent that the AuCP simply mimics the CP itself implying a successful lift-off. From the image, the estimated 2D metal fill factor is 15%. The connectivity in

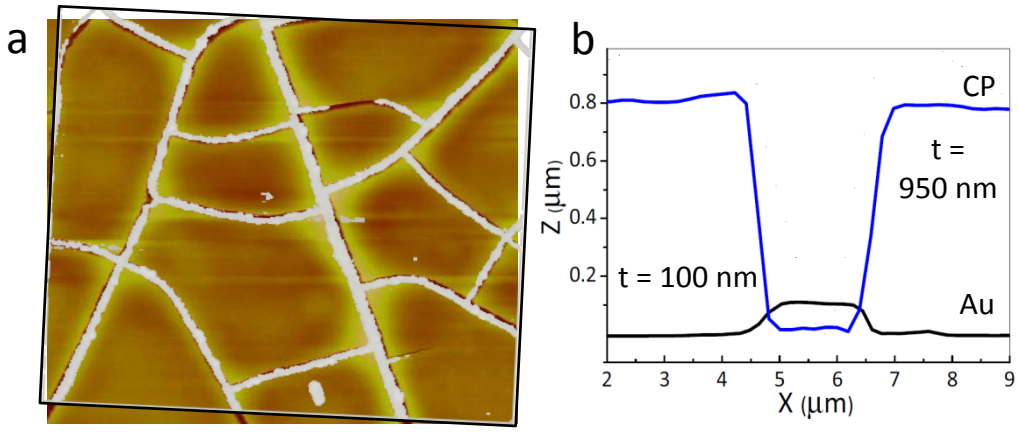

Figure IIIA.4 (a) AFM topography images (80 × 80 µm^2) from Figures IIIA.3b and 3c overlaid (AuCP is shown in white color). (b) Depth profile of a crackle groove (blue curve) and height profile of AuCP (black curve).

the wire network was examined in more detail. From the optical profilometry (OP) image in Figure IIIA.3d, one can actually follow individual wires and realize how they branch out and connect endlessly from one end to the other. The wire surface is quite smooth. The estimated surface roughness from 1.1 × 1.3 mm^2 area is ~ 9 nm, while that obtained from AFM image in Figure IIIA.3c, ~ 4.9 nm. The uniformity of the wire density in a AuCP/PET derived MCP was examined under SEM over 1.2 × 1.2 mm^2. As many as 400 images (each, 60 × 60 µm^2) were collected (see Figure IIIA.5) so as to cover this area and the estimated metal fill factors are

depicted in the form of a map in Figure IIIA.3e. The fill factor shows a standard deviation of only 2.1% for mean value of 14.8%. From the AFM, OP and SEM images, it became clear that the Au wires are distributed in a continuous network leaving no region larger than an average polygon and that no residual crackle layer was left behind during lift-off.

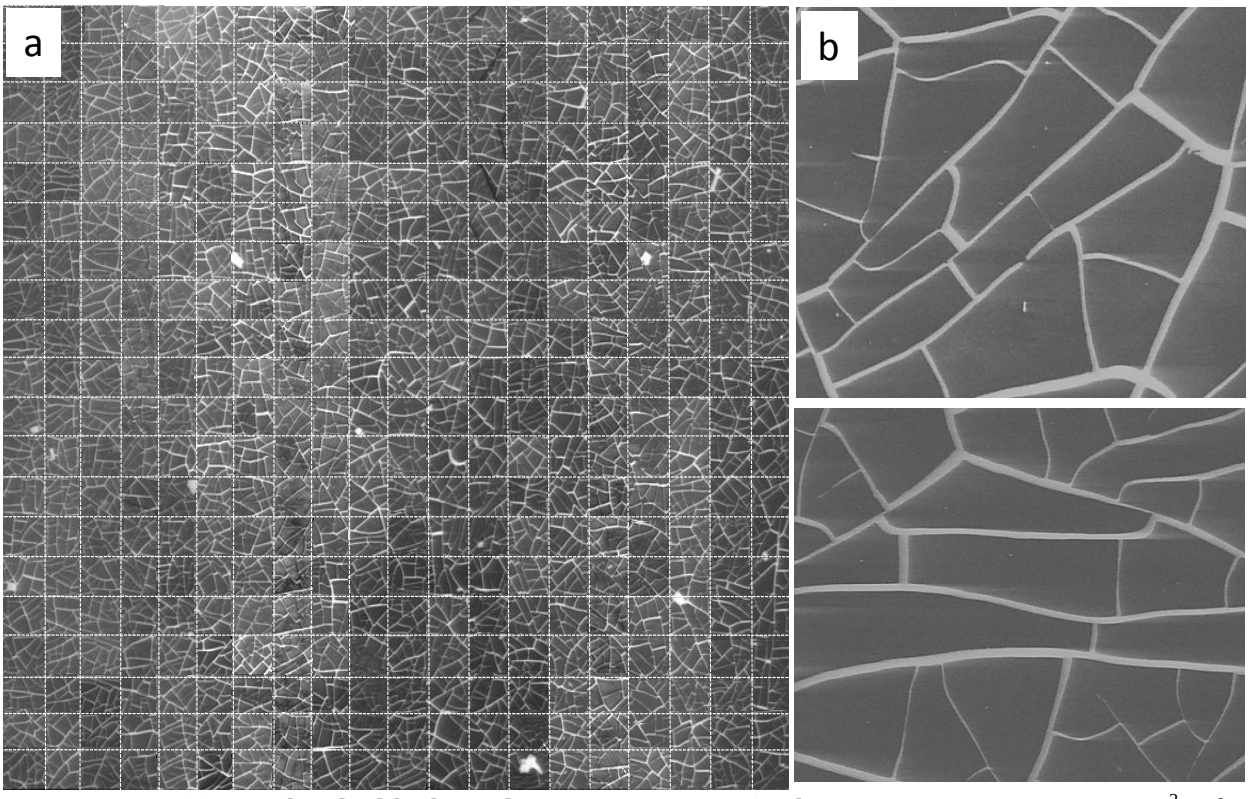

Figure IIIA.5 (a) Four hundred high resolution SEM images (each square region is 60 × 60 μm^2) of a AuCP/PET stitched to cover 1.2 × 1.2 mm^2 area. (b) Full size SEM images are given (scale bar, 100 μm). Note: The contrast is slightly varied due to charging during imaging. Image-J software is used to estimate fill factors shown in the form of a map in Figure IIIA.3e.

Crackle lithography offers a possibility of forming hybrid wire networks as well. As an example shown in Figure IIIA.3f, a crackle pattern on PET was deposited with Cu first (thickness, ~ 160 nm) followed by Au (~ 100 nm) to result in Au-CuCP/PET. This way, a cheaper metal network such as Cu, can be used as an electrical backbone while the top metal (Au) provides the desired surface properties (passivation, work function etc.) in a device. In another instance, Al was deposited on Cu in crackle grooves prior to lift-off, to produce Al-

CuCP/PET. The Kelvin probe force microscopy profile images shown in Figure IIIA.6 clearly demonstrates work function for Cu and Al metals, 4.8 and 4.3 eV, respectively.

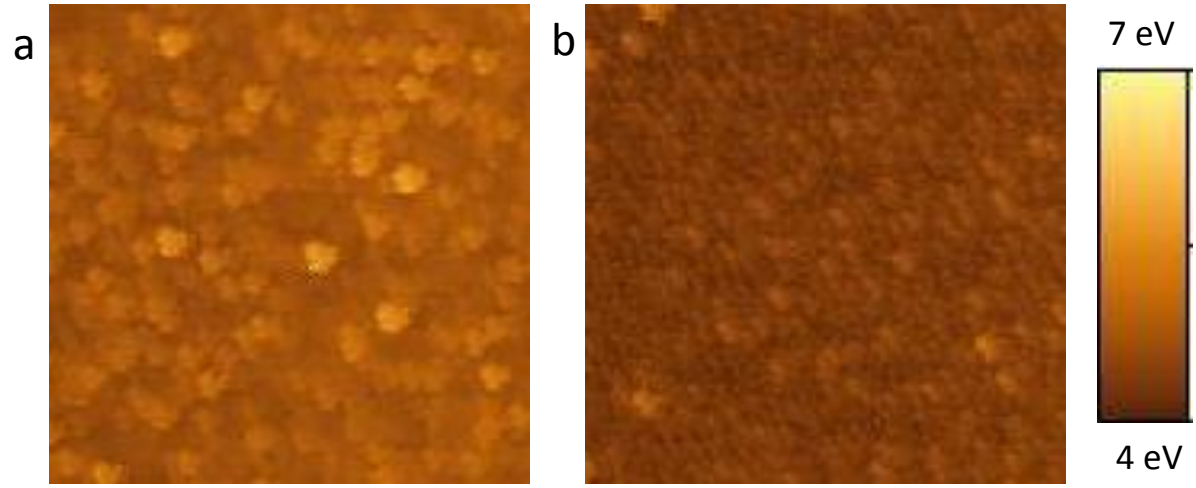

Figure IIIA.6 (a) & (b) Kelvin probe force microscopy image (10 × 10 μm^2) of CuCP (work function, 4.8 eV) and AlCP (work function, 4.3 eV) recorded with tip lift height of 100 nm. The scale bar represents the work function from 4 to 7 eV.

As is clear from the above discussion, crackle lithography has many unique features to offer- the template preparation is simple, virtually unlimited in terms of areal spread and crackle formation is spontaneous; crackle dimension lies in μm to sub-μm range; fill factors are low and lift-off process is neat etc. The resulting pattern is essentially single wire network, which is here explored as TCE. Beginning with rod coating of the crackle dispersion, a AuCP/PET based TCE of size ~ 15 × 20 cm^2 was made. When used as a window for a display (Figure IIIA.7a), it was quite transparent with no visual sign of the metal wire. In the given example, the TCE window stands in series with the LED array, which demonstrates its good conducting ability. Obviously, this is due to the invisible Au wire network over the PET substrate (Figure IIIA.7b). A AuCP/PET based TCE was fabricated over a PET area of 15 × 20 cm^2 by rod coating the crackle solution, followed by Au deposition and lift-off. The photograph in Figure IIIA.7b demonstrates the transparency of the TCE. The optical micrographs surrounding the photograph in Figure

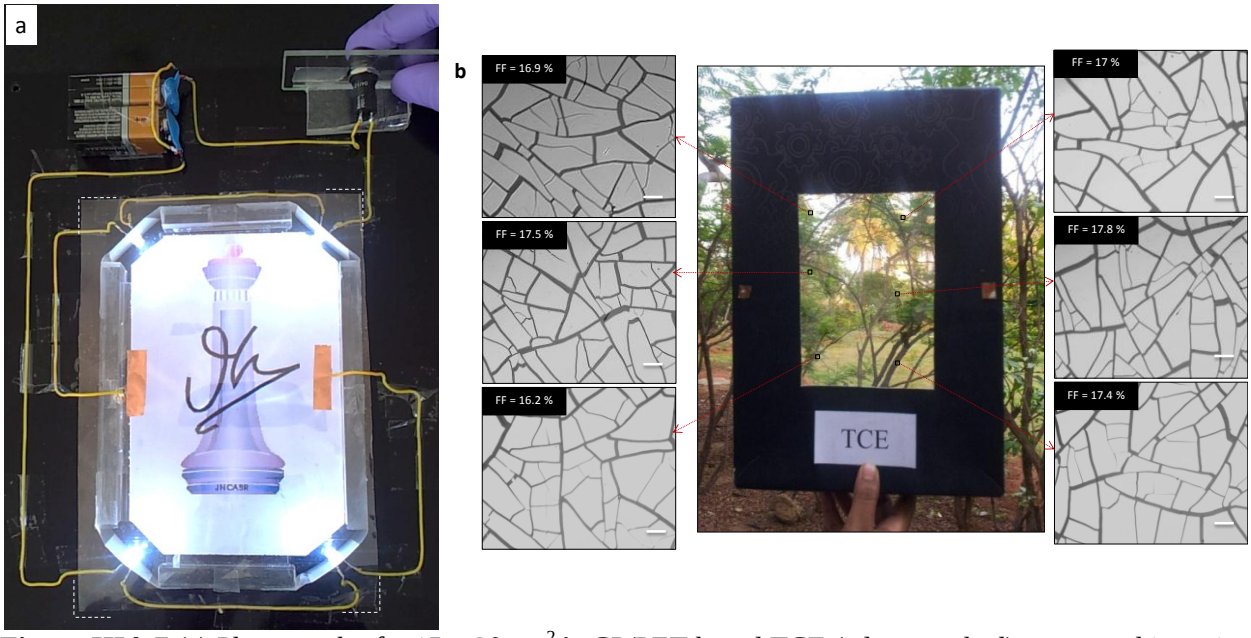

Figure IIIA.7 (a) Photograph of a 15 x 20 cm^2AuCP/PET based TCE (edges marked) connected in series with four LEDs illuminating the JNCASR emblem, which is viewed through the TCE. (b) A garden viewed through a AuCP/PET based TCE (15 × 20 cm^2). Optical micrographs from the marked regions are shown alongside (scale bar, 40 μm).

IIIA.7b, have been chosen randomly from different parts of the TCE to show the uniform spread of the Au wire network. The Au fill factor is found to vary in a narrow range, 16.2% to 17.8%. The sheet resistance of the TCE was 3.8 Ω/sq. Importantly, the TCE fabrication by crackle lithography need not restrict to cm^2 areas; with proper coating and deposition arrangements, TCEs over ultra-larges areas can be realized without comprising uniformity in parameters.

The TCE fabrication using crackle lithography was also extended to curved surfaces such as a cylindrical surface shown in Figure IIIA.8a. For sake of demonstration, a LED was placed inside the tube and the curved TCE was connected in series to the external circuit to light the LED (see Figure IIIA.8a). Non-cylindrical curved surfaces also will do. The fabrication of TCE over the quartz tube was done using a custom made setup as shown in Figure IIIA.8b, which was used to rotate the quartz tube while coating the crackle template and depositing metal inside physical vapour deposition chamber. As shown in the optical micrograph of Figure IIIA.8c, the metal

wire network is interconnected even on curved surfaces. The optical profile image reveals thickness of the metal wires and the curvature of the quartz tube.

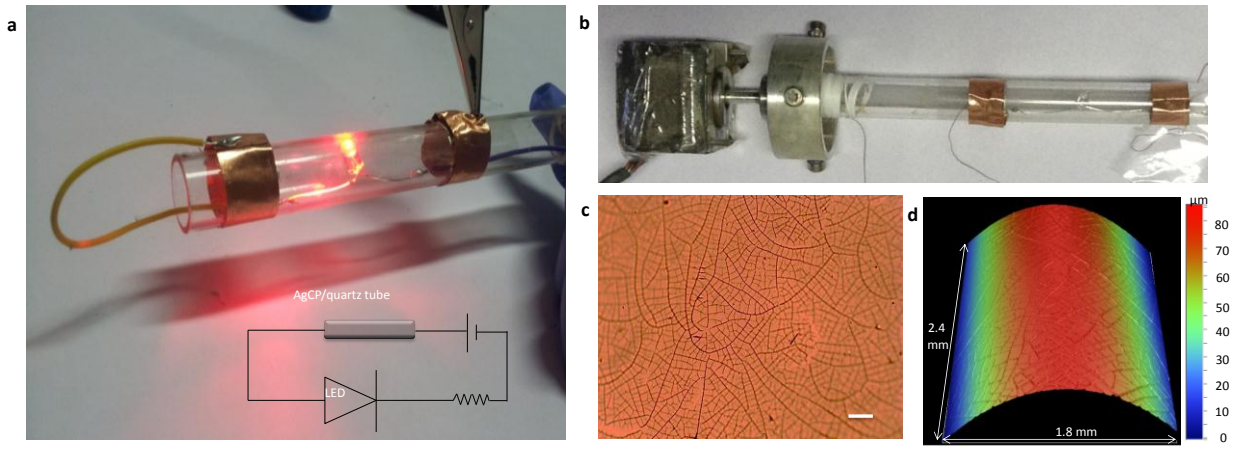

Figure IIIA.8 (a) Photograph of the quartz tube patterned with AgCP around the tube (diameter, 12 mm and length, 8 cm). The TCE thus made is connected in series with a LED circuit (shown in the inset). (b) A quartz tube (1.2 cm diameter) used as an example of curved surface, is shown mounted on a setup for rotating the tube during metal deposition inside the evaporation chamber. The copper rings on either side establish electrical contact with AgCP. (c) Optical micrograph of the Ag network on the quartz tube (Scale bar 100 μm). (d) Optical profilometric image of a curved quartz tube surface deposited with AgCP.

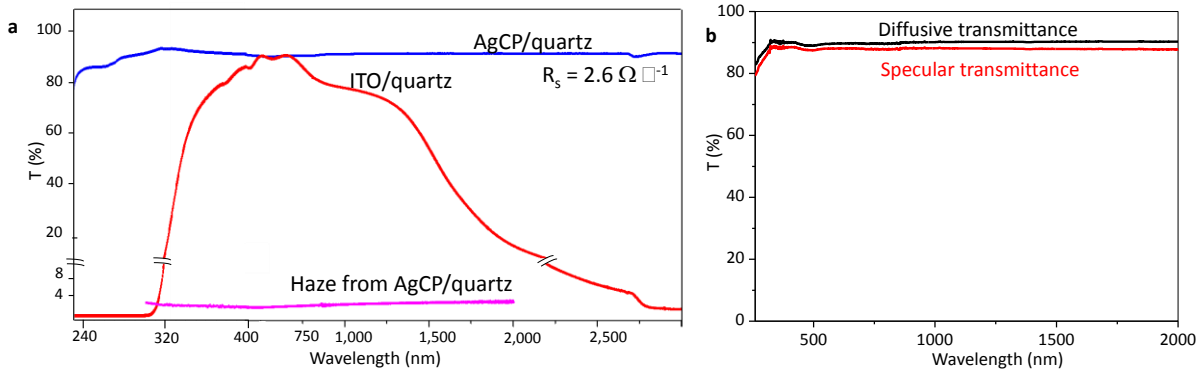

Figure IIIA.9 Transmittance of MCP derived TCEs. (a) Transmittance spectrum of AgCP/quartz compared with that of ITO/quartz over a broad wavelength range covering UV, visible and IR (with UV region expanded). The haze data (pink curve) is shown in the range 300-3000 nm. (b) Diffusive and specular transmittance of AgCP/quartz in the range 300-2000 nm.

As light transmission is determined by the optical properties of the insulating substrate, a substrate such as quartz which is transparent from UV to IR, can offer as an interesting possibility. A AgCP supported on quartz (Figure IIIA.9a, blue curve), exhibited average T of 90.5% in a wide spectral range, 240 to 3000 nm (~ 82% in the UV region). This TCE showed a

low R_s value of 2.6 Ω/sq. Thus, its transmittance value is comparable to that of 2-3 layer graphene based TCE,[11] but appreciably, R_s is one order better. This TCE may also be compared with ITO, which is inherently a poor transmitter in UV and IR regions (red curve in Figure IIIA.9a).[7] In order to determine haze of the TCE, diffusive and specular transmission was done as shown in the Figure IIIA.9b. Haze calculation was done using the following equation,

$$\mathbf{H = \Delta T/T_{dif} \times 100}$$

Where $\Delta T = T_{dif} - T_{sp}$
T_{dif} = Diffusive transmittance
T_{sp} = Specular transmittance

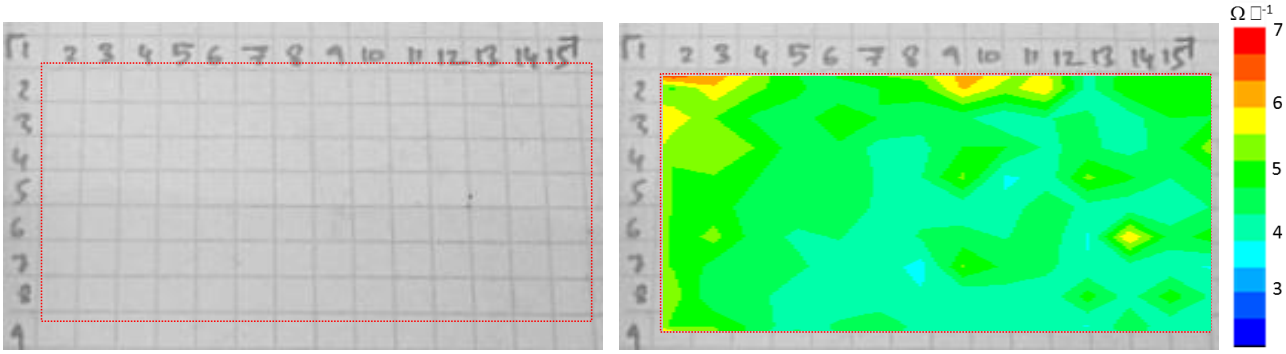

Figure IIIA.10 Top panel: Photograph of a AgCP/PET placed over a paper marked with a grid (3.5 x 7 cm^2), bottom panel: Spatial map of R_s corresponding to the grid.

The small difference (1-2%) in the specular and diffusive transmission is due to the scattering of metal wire network. Importantly, the haze value of the AgCP/quartz was notably small, ~ 2 to 3% (Figure IIIA.9a).

A sheet resistance map of a AgCP/PET produced using four-probe measurements (Figure IIIA.10), is uniform except at the edges; the mean R_s value is found to be 4.7 ± 1 Ω/sq. The uniform sheet resistance of AgCP is attributed to interconnectivity and uniform fill factor (see Figure IIIA.3e) of the Ag wire network over large area. Such TCE play crucial role in fabrication

of large area optoelectronic devices. Thus, the fabricated TCE derived from crackle lithography not only have high transmittance but also low and uniform sheet resistance over large areas.

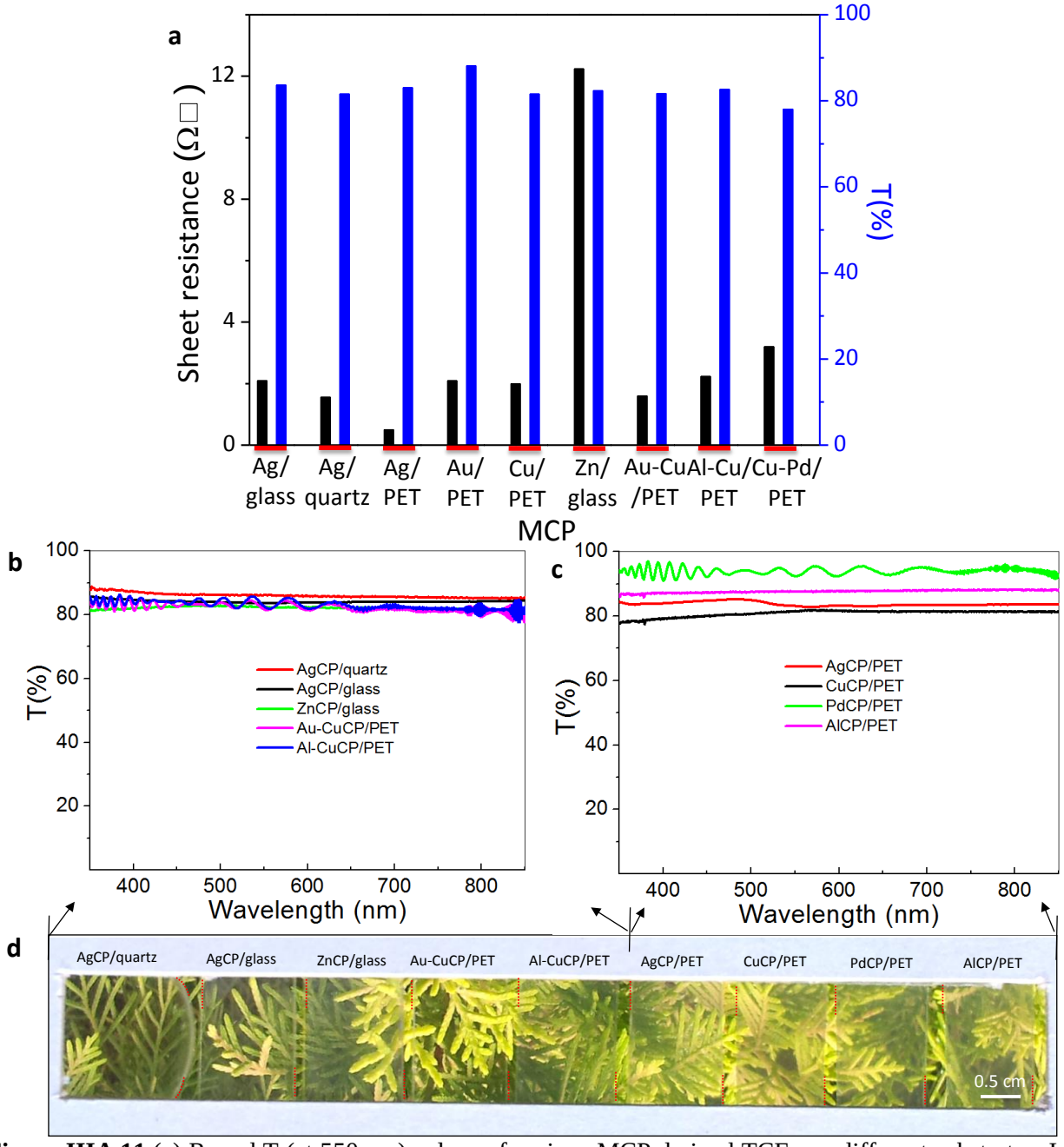

Figure IIIA.11 (a) R_s and T (at 550 nm) values of various MCP derived TCEs on different substrates. In each case, left histogram bar refers to sheet resistance and the right bar, T.(b) & (c) Transmittance of various MCP derived TCEs on different substrates, (d) A photograph of a plant seen through a rectangular cardboard slot to which the various TCEs are stuck. Dashed red lines indicate the edges of the TCEs.

In similar way, several MCP derived TCEs (different metals on different substrates) were made as listed in Table IIIA.2. Figure IIIA.11a depicts T and R_s values of single and two metal electrodes made in this study. All the MCPs showed low sheet resistance except what is noteworthy is that the R_s values in all the cases are noticeably low, although the conduction is through a network structure. ZnCP/glass showed relatively high sheet resistance due to the oxidation of Zn when exposed to air. The transmission spectra of MCP derived TCEs is shown in Figure IIIA.11b and 11c, reveals similar transmission independent of metal. This is attributed to the low fill factors of metals, which can be easily controlled during the crackle template fabrication.

Table IIIA.2: Characteristics of MCP derived TCEs

S.No.	MCP/substrate	Sheet resistance (Ω/sq)	Specular transmittance at 550 nm (%)	Wire thickness (nm)
1	AgCP/glass	2.1	83.7	110
2	AgCP/quartz	2.6	86.1	90
3	AuCP/PET over 15 x 20 cm^2 area	4.5	88	100
4	AuCP/PET	3.8	88.1	100
5	AlCP/PET	52.8	87.6	110
6	CuCP/PET	2.0	81.6	160
7	ZnCP/glass	12.2	82.4	240
8	Au-CuCP/PET	1.6	81.7	260
9	Al-CuCP/PET	2.2	82.6	220
10	Cu-PdCP/PET	3.2	78.1	720

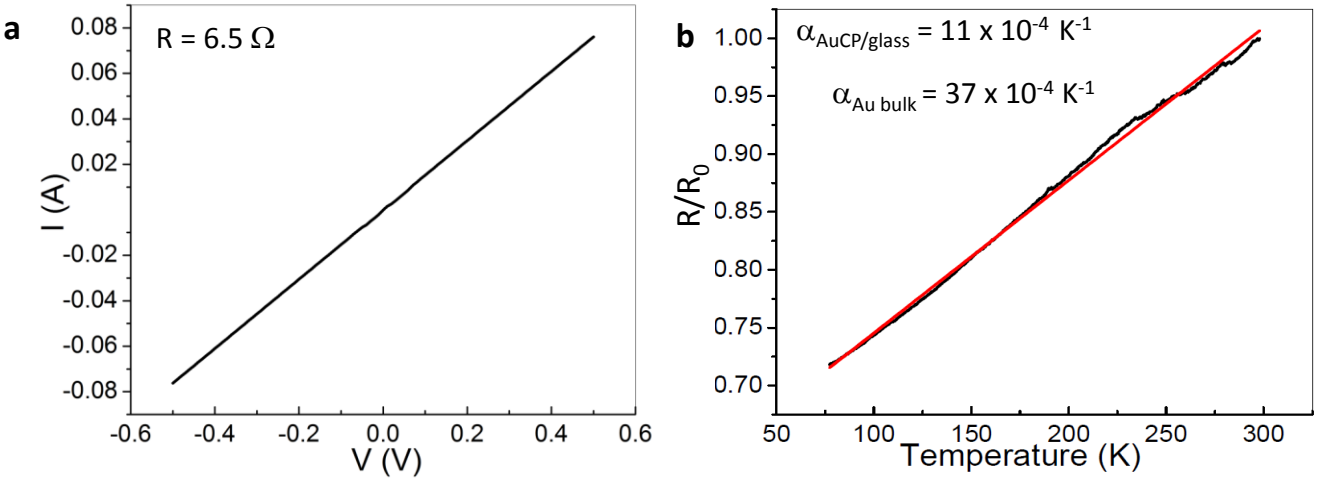

Figure IIIA.12 (a) I-V characteristics of AuCP/glass derived TCE at room temperature. (b) Temperature dependence of the resistance, normalized with respect to room temperature, from 298 to 77 K (black curve). The red line is a linear fit to the data.

In order to determine mode of the conduction in AuCP/glass, the electrical measurement were performed (see Figure IIIA.12). The two probe I-V characteristics are linear with the two probe resistance of 6.5 Ω for an electrode spacing of 1 mm, MCP thickness 55 nm (see Figure IIIA.12a). The temperature dependent resistance was measured from 298 to 77 K (see Figure IIIA.12b). The decrease in resistance with decreasing temperature demonstrates, as expected, the metallic behavior of the Au network, the slight deviation from linearity being due to the presence of boundary wall.[43] Temperature coefficient of resistance (TCR) was calculated to be $\alpha = 11 \times 10^{-4}$ K^{-1}, which is nearly three times less compared to the bulk value ($\alpha = 37 \times 10^{-4}$ K^{-1}). The observed lower value of TCR is due to the scattering of electrons at the edges and boundaries of the Au network. However, this value is close to that obtained in the case of Au thin films ($\alpha = 6.67 \times 10^{-4}$ K^{-1}). The resistivity was calculated by the following equation,

$$\rho_{CP} = R_s \times t_{CP}$$

$$\text{and } V_{CP} = L \times W \times FF \times t_{film}$$
$$= L \times W \times \left[FF \times t_{film}\right]$$
$$= L \times W \times t_{CP}$$

where ρ_{CP}= Resistivity of MCP

R_s = Four probe sheet resistance of MCP = 3.8 Ω/sq

t_{CP} = Thickness of MCP film = 20 nm

V_{CP}= Volume of MCP = 10.8×10^{-6} mm^3

W = Width of the electrode = 0.45 mm

L = Length of the electrode = 1.2 mm

FF = Metal fill factor = 20%

t_{film}= Thickness of metal film = 100 nm

The resistivity of AuCP/glass ($\rho_{AuCP/glass}$ = 6.2×10^{-8}Ω-m) is comparable to the bulk resistivity of Au ($\rho_{Au\ bulk}$ = 2.4×10^{-8}Ω-m). This is understandable as the conduction is through a single metallic network with seamless junctions where the issue of contact resistance of crossbar junctions does not arise.[17, 24, 26] Moreover, the TCEs fabricated through crackle lithography are quite stable even after 8 months.

Crackle lithography offers many other possibilities. Crackles of varying widths can be produced merely by controlling the thickness of the crackle layer in the first step (see Figure IIIA.1g), which, by design, can be translated to the MCP itself. For average wire widths of 2 to 6 μm (see Figure IIIA.13a). The average crackle width is calculated as shown in the inset of optical micrograph Figure IIIA.13b through the following formula.

(Metal wire area) / (Metal wire perimeter excluding the edges) = (a × b) / (2 × b)

= a/2 (half of average wire width)

Image J software is used to calculate the fill factor and crackle width. The cell size is increasing with the average wire width, keeping the fill factor almost constant (see Figure IIIA.13b). The optical micrographs of the Ag network with 2, 3.2, 4.1 and 6.2 μm, corresponding the crackle coating thickness 0.95, 1.39, 2.71 and 3.65 μm respectively, as shown in Figure IIIA.13c.

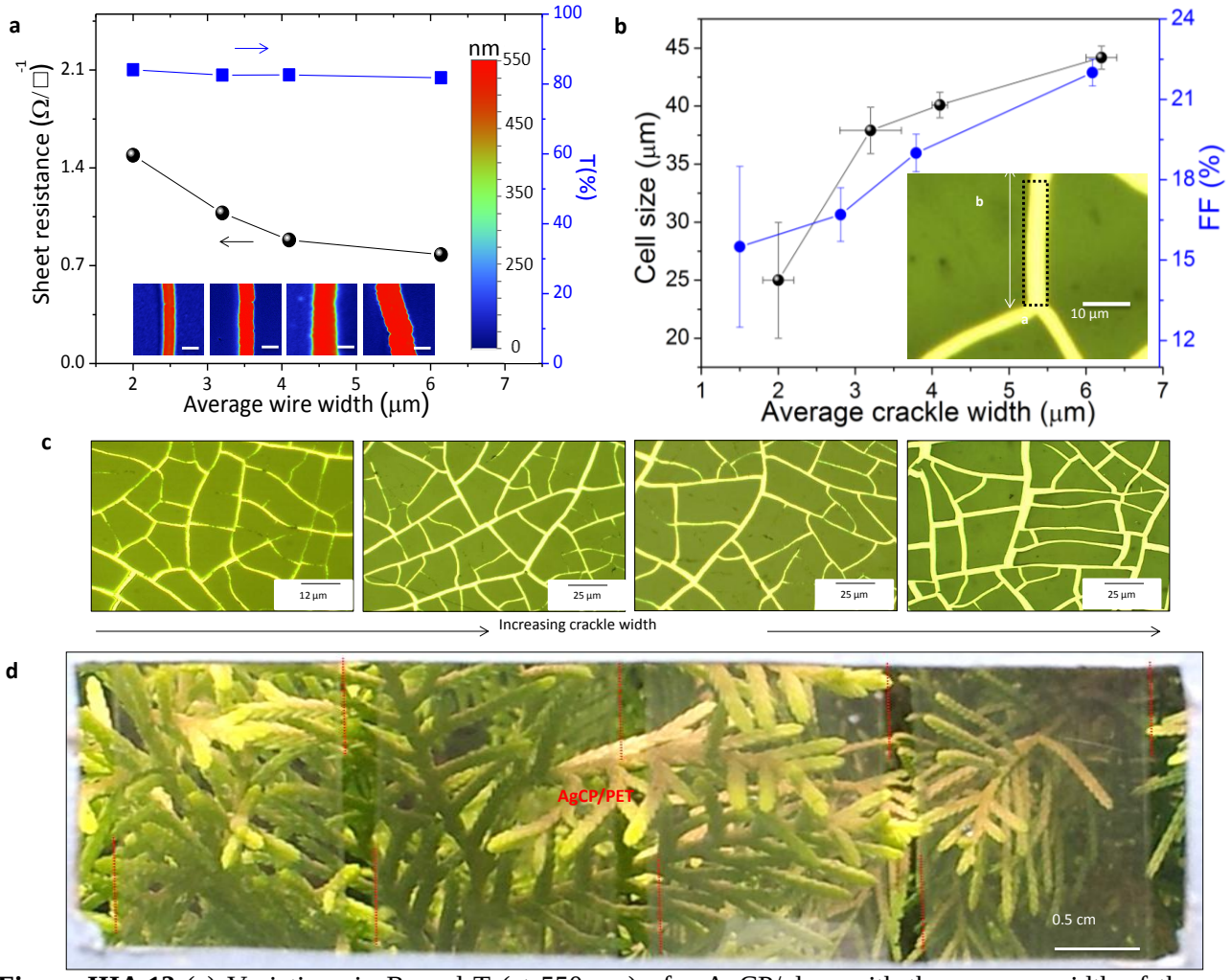

Figure IIIA.13 (a) Variations in R_s and T (at 550 nm) of a AgCP/glass with the average width of the patterned metal wire (thickness, 550 nm). (b) Variations in the average cell size (square root of area) and metal fill factor (FF%) with the average crackle width. Inset shows an optical micrograph of the Ag wire with 5 μm. (c) Optical micrographs of AgCP/PET with average crackle widths of 2, 3.2, 4.1 and 6.2 μm, respectively. (d) TCEs stuck on a cardboard slot and the view of a plant behind.

Photograph of AgCP/PET derived TCEs is shown in Figure IIIA.13d.With increase in the crackle width cell size increases linearly as shown in Figure IIIA.13b. On the other hand the metal fill factor increased slightly from 15% to 21% with crackle width. As a consequence the transmittance decreased from 84% to 81% and R_s also decreased as expected, 1.49 to 0.77 Ω/sq. The wire thickness variation is another interesting situation (see Figure IIIA.14 and Table IIIA.3).

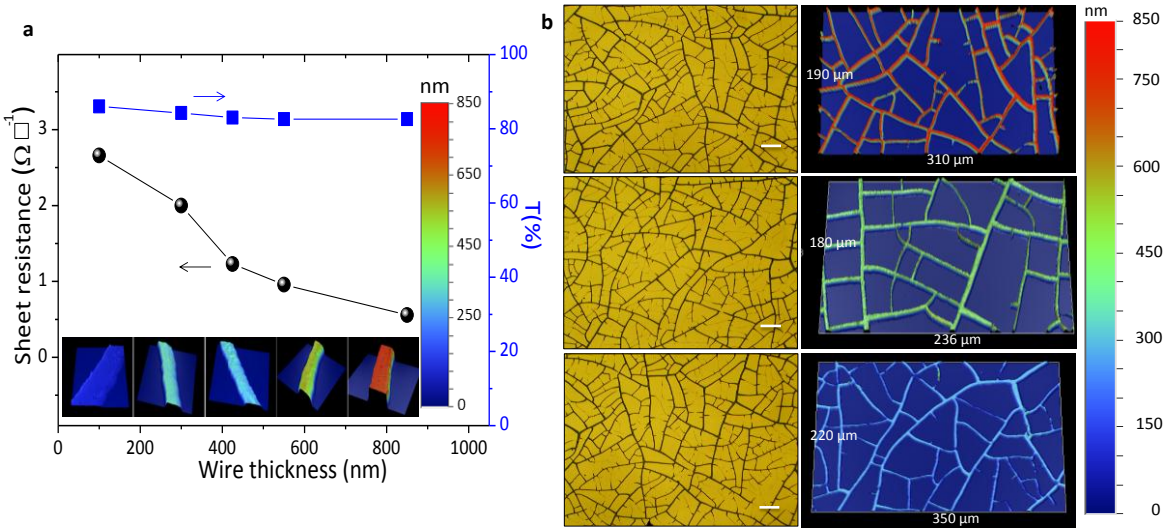

Figure IIIA.14 (a) Variations in R_s and T (at 550 nm) of a AgCP/glass with the Ag thickness deposited (for average wire width of 4 µm).(b) Optical micrographs and optical profile images of the TCEs with various average wire thicknesses 850 nm, 550 nm and 300 nm (scale bar 50 µm).

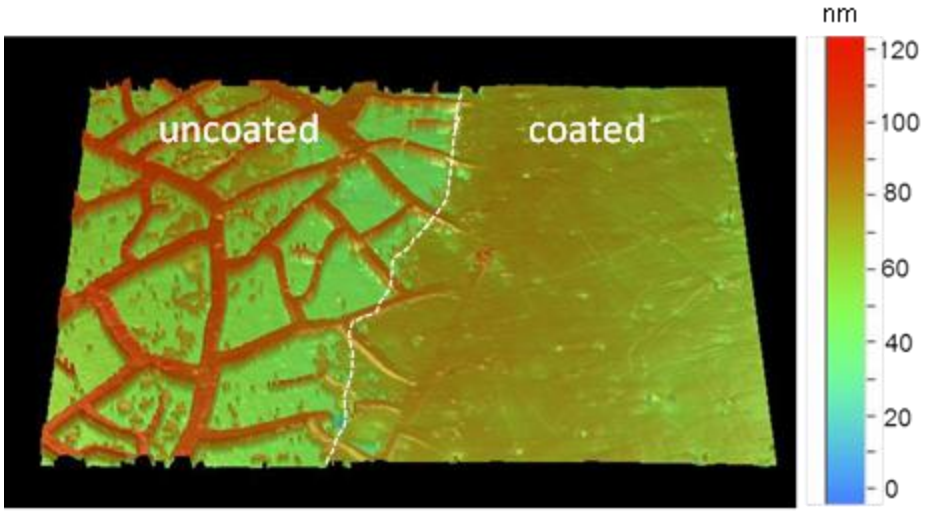

Figure IIIA.15 Optical profiler image of AgCP/PET derived TCE coated with PEDOT: PSS.

Given that the crackle template is a micrometer deep groove (Figure IIIA.1f), metal deposition in the second step need not restrict to low thicknesses. As shown in Figure IIIA.14b, the metal fill factor and wire width is constant (~ 4 µm), but thickness is increased from 300 to 850 nm. The increase in the thickness is revealed in optical profiler images in Figure IIIA.14b. Indeed, wall-like metal structures (~ 850 nm in Figure IIIA.14a) can be easily made to improve sheet

Table IIIA.3: AgCP/PET derived TCEs with various wire widths and thicknesses

S.No.	Average wire width (~µm)	Wire thickness (nm)	Sheet resistance (Ω/sq)	Specular transmittance at 550 nm (%)
1	2	550	1.49	83.7
2	3.2	550	1.07	86.1
3	4.1	550	0.88	83.1
4	6.14	550	0.78	88.1
5	4	100	2.66	87.6
6	4	300	2.00	86.0
7	4	425	1.23	83.1
8	4	550	0.95	84.6
9	4	850	0.55	82.5

resistance without compromising much in transmittance, as in grating structures.[44] The later however, suffer from diffraction related losses unlike the random networks dealt in this study.[45] In many TCEs, reducing sheet resistance demands a higher thickness at the cost of transmittance.[28,46-48] The crackle lithography allows to fabricated TCEs with ultralow sheet resistance (see Table IIIA.3) in two approaches one is increasing the wire width and keeping the wire thickness constant and in second approach increasing the wire thickness and keeping the wire width constant. Such ultralow sheet resistance TCEs finds importance in fabrication of high

performance optoelectronic devices. Finite thickness is sometimes a disadvantage in applications such as solar cells. Many recipes have emerged to deal with issues of topography of the wire network by embedding electrodes in substrate or coating with a conducting polymer (PEDOT:PSS). The wire thicknesses are ~ few hundreds of nms, the wire network may be embedded (partially as required) in the substrate as shown in Figure IIIA.15. The method of embedding grid electrodes is well established in the literature.[49] This is a useful step for the fabrication of thin film devices.

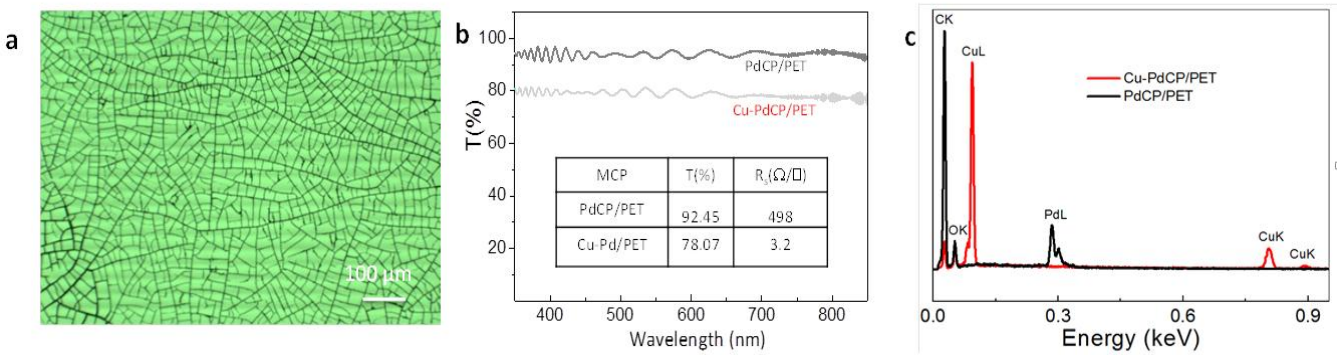

Figure IIIA.16 (a) Optical micrograph of the PdCP/PET seed layer, (b) transmittance spectra of Cu-PdCP/PET before (with only Pd seed layer) and after electroless deposition of Cu. The corresponding sheet resistance values are also indicated. (c) EDAX spectrum of Pd seed layer and electroless deposited Cu layer.

In order to demonstrate the versatility of TCE fabrication, a thin film of Pd (30 nm) was deposited on the crackle coat and after lift-off, PdCP/PET (Figure IIIA.16a) with T of 92% and R_s of 498 Ω/sq, resulted (Figure IIIA.16b). This TCE served as a seed layer for electroless deposition of Cu. It was dipped in Cu plating solution (Copper A: formaldehyde (10:1)) for 5 min. The uptake of Cu is established by the EDS data in Figure IIIA.16c. Due to increased wire thickness (from 30 to 720), the sheet resistance improved to 3.2 Ω/sq while the T decreased slightly (78%) as shown in Figure IIIA.16b. This experiment clearly demonstrates the possibility of making TCEs via solution processed (chemical) deposition. Solution based deposition in the

crackle grooves widens the scope of this method and can cut down process costs. Such low cost fabrication methods ease the manufacture of roll-to-roll TCE over ultra large areas.

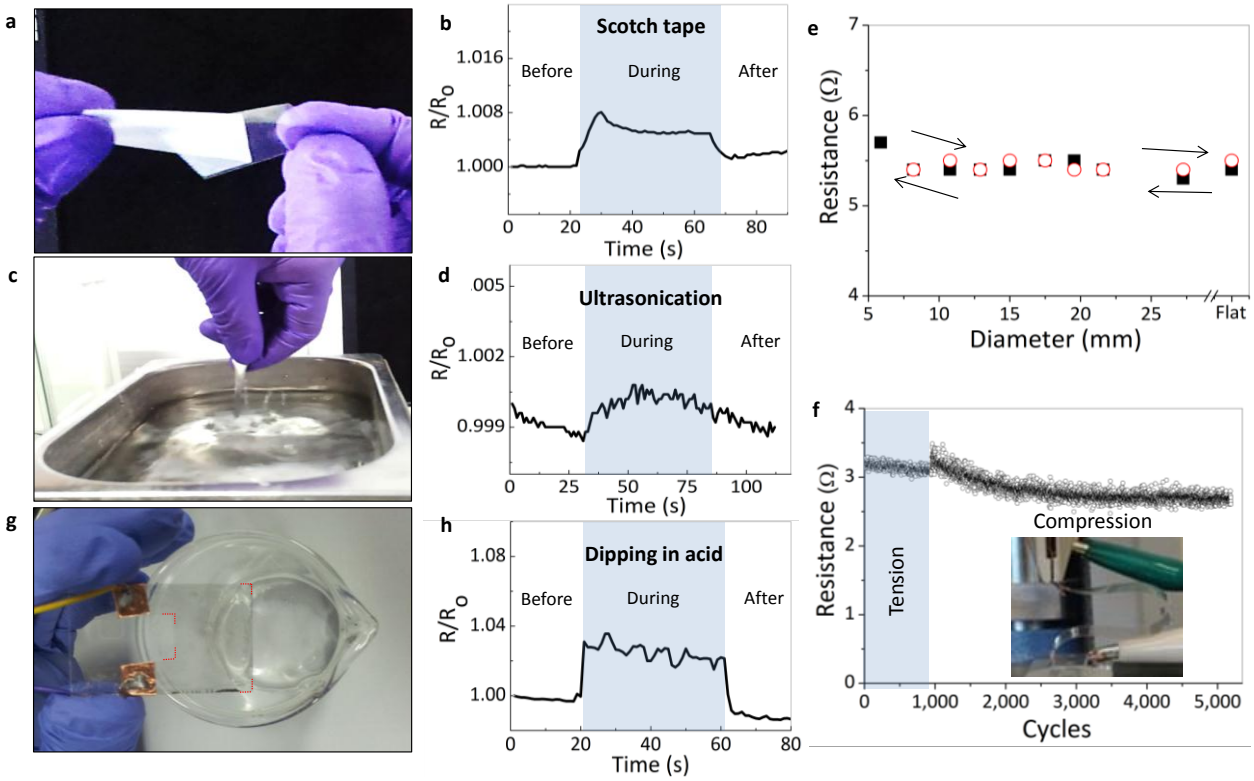

Figure IIIA.17 Mechanical, chemical stability and flexibility tests of AgCP/PET. (a) Adhesion tolerance test on a AgCP/PET using a scotch tape and (b) the relative change in resistance during the scotch tape adhesion test. (c) AgCP/PET subjected to ultrasonication (d) the relative change in resistance during the sonication test. (e) Resistance of AgCP/PET as function of bending diameter, during bending (solid black squares) and relaxing (open red circles). (f) Resistance variation over a large number of tension and compression cycles recorded using an automated setup (inset). (g) A Au-CrCP/glass derived TCE (2 × 2.5 cm^2 area) dipped in concentrated sulfuric acid in a beaker, (h) the relative change in resistance during the acid-dip test.

For flexible electronic applications, PET is the most preferred substrate as it, besides being flexible, offers good adhesion to metals.[50] In order to access the suitability of the MCP based TCEs, several mechanical tests have been carried out on a AgCP/PET. During the scotch tape test (Figure IIIA.17), its resistance was found practically unaffected (Figure IIIA.17b) and there was no noticeable sign of damage due to peeling off the adhesive tape (for optical micrographs see Figure IIIA.18). The same substrate was then dipped in an ultrasonic bath

(Figure IIIA.17c) and the resistance change was again insignificant (see Figure IIIA.17d). The AgCP was indeed intact, as can be seen from the optical micrographs, the wires are intact on the PET substrate with no visible damage. Regions 1, 2 and 3 have been marked to guide the eye in Figure IIIA.18. There is a small and partial reversible change ($\delta R = 0.001$) in the resistance during the ultrasonication, which may be due to the local temperature rise in the ultrasonication bath. The metal adhesion on PET has been studied in detail. The kinetic energy of the metal atoms is used to melt the polymer surface leading to good mechanical adhesion. Moreover, during the metal evaporation the more diffusion and less lateral mobility of metal atoms inside the PET improves the adhesion.[50]

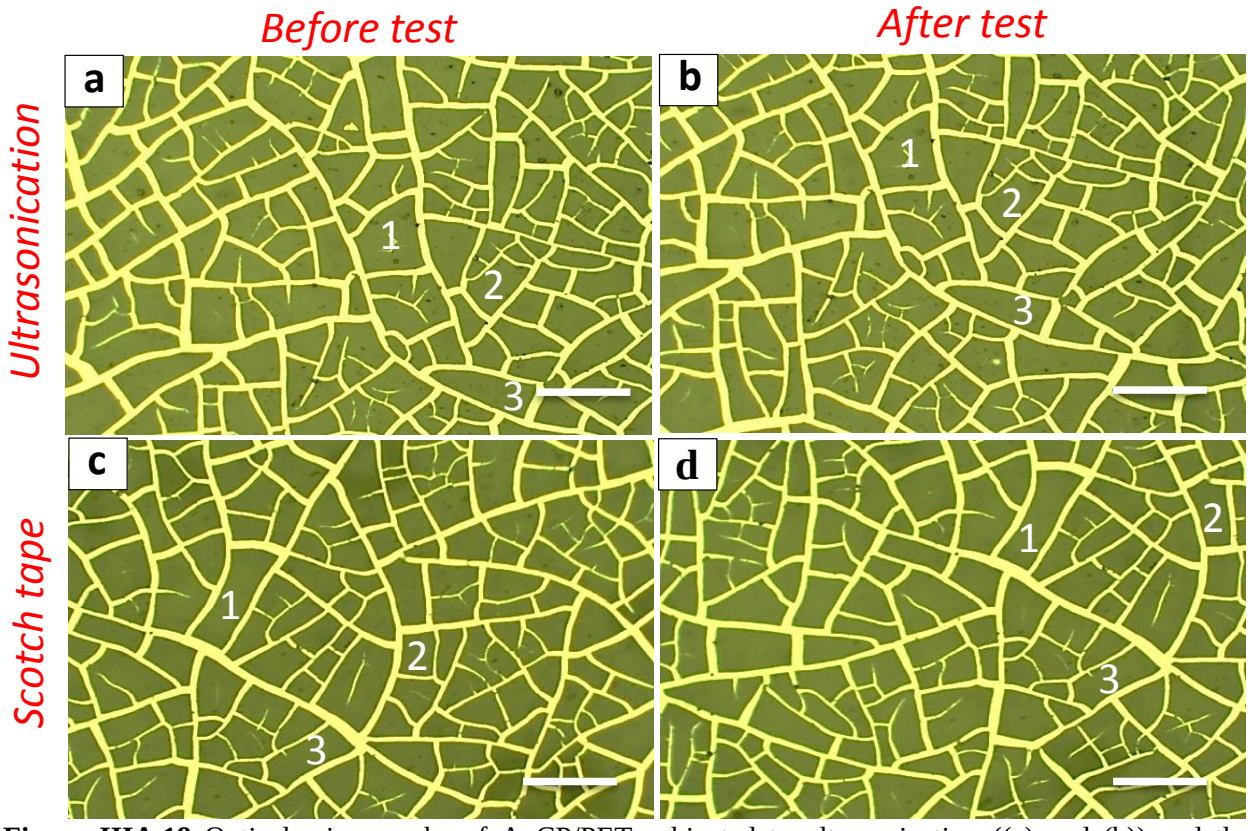

Figure IIIA.18 Optical micrographs of AgCP/PET subjected to ultrasonication ((a) and (b)) and the scotch tape adhesion tolerance tests ((c) & (d)). Left images are before and right ones are after the tests. Scale bar, 100 µm.

During the bending test (Figure IIIA.17e), it was gradually bent to 5.9 mm diameter with a force of 0.89 N (black squares) and relaxed (red circles). The bending cycle was repeated over several thousand times in tension and compression modes (Figure IIIA.17f) using an automated setup (see inset) and the change in the resistance was less than ~ 0.5 Ω. The above tests clearly demonstrate the mechanical robustness of the AgCP/PET electrodes produced using crackle lithography. In another instance using glass as substrate, a Au-CrCP electrode was dipped in concentrated sulfuric acid (Figure IIIA.17g and 17h), and the electrode could withstand the harsh chemical bath. The partial and reversible resistance change ($\delta R = 0.04$) in the MCP is may be due to reversible adsorption of cations/water on metal surface. The MCP electrodes are stable in organic solvents such as chloroform, toluene and isopropyl alcohol as well.

Figure IIIA.19 Photograph of the Ag metal recovered from the crackle coating after liftoff**.**

While the presented method is subtractive, it does enable complete excess metal recovery, as the template is highly soluble in solvents. During the fabrication of a MCP derived TCE, metal is deposited on top the crackled coat and after lift-off, only the metal deposited inside the crackle is retained on the substrate while the rest deposited on the planar regions of the coat, outside of the crackle, gets washed away with the developing solvent (chloroform). The

developed solution was washed in chloroform, after solvent evaporation, Ag is recovered. The photograph of recovered Ag metal is shown in the Figure IIIA.19. The metal recovery is up to 76 - 85% of the metal deposited (metal fill factor is 15% to 24%). In principle all the metals can be recovered in similar manner. Thus, the metal washed away during lift-off can be easily recovered, which is an important aspect during large-scale fabrication.[51]

IIIA.5 Conclusions

This study develops a low cost, three step method to produce large area transparent conducting electrodes using crackle lithography. It makes use of environment-friendly solvents, common glassware, cheap sacrificial layer and a simple physical vapor deposition system. The sacrificial layer is vacuum compatible. It takes just few hours to make a TCE with reproducible metal fill factor over large area. The method can potentially be adopted for roll-to-roll processing as well. Compared to many literature methods,[52] this templating procedure is subtractive. The MCP based TCE is a single continuous network of smooth metal micro/nanowires with seamless junctions. Several TCEs (M = Au, Ag, Cu, Pd, Al, Zn) on different substrates, glass, quartz and PET, have been successfully made. Patterning TCE on curved surfaces is an additional possibility. With this method, low values of sheet resistance, 0.5 Ω/sq at T ~ 83% could be obtained by controlling the wire thickness. Compared to ITO and other literature examples, the TCEs reported here excel in wide spectral range transmittance. Compared to ITO and other literature examples, the TCEs reported here excel in wide spectral range transmittance, and also exhibit high performance in terms of flexibility, chemical and mechanical stability.

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Chapter III

IIIB: Applications of transparent conducting electrodes

IIIB.1 ITO-free organic solar cell

Summary

This Part deals with the incorporation of Ag wire network derived TCE from crackle lithography in organic solar cell. A 135 nm ZnO thin film was used in the fabrication of (P3HT:PCBM) organic solar cell, which buried only not the roughness of Ag wire network but also accomplished as a barrier layer for charge extraction. The performance of the fabricated organic solar cell has a comparable performance to that of conventional ITO electrodes. This is a general approach to replace ITO in diverse thin film devices.

IIIB.1.1 Introduction

Organic solar cells (OSCs) are an attractive option for large area and inexpensive production of modules. This is because OSCs are well suited to low cost manufacturing due to simple processing[1] steps that are easily translated to roll-to-roll mass production[2] and leading to near commercialization. In the recent past, extensive research has been carried out on the active semiconductor ingredients[3] and electrode optimization,[4] in order to improve the OSC performance,[5] which is typically poorer compared to other types of solar cells such as dye sensitized solar cells[6] and silicon based solar cells.[7, 8] Nonetheless, OSCs occupy unique position in photovoltaic roadmap as solid state, flexible, environmentally benign and ultralight large area devices.[9]

In OSCs, indium tin oxide (ITO) is the most commonly used transparent conducting electrode. Best ITO films exhibit transmittance of 92% in the visible region and a sheet resistance of 10 ohm/sq.[10] Indium is scarce and expensive;[11] ITO requires high temperature processing and is brittle, develops cracks on flexible substrates.[12] In order to address these issues, there has been much effort in the literature towards alternate electrodes. Graphene,[13] carbon nanotubes (CNT),[14, 15] and Ag nanowires[16, 17] have been proposed as alternatives to ITO and used in the fabrication of OSCs. Graphene and networked TCEs suffer from optoelectronic and fabrication related issues as discussed in Part-IIA section IIA.1.

IIIB.1.2 Scope of the present investigation

Perforated metallic films in the form of meshes or grids offer as attractive alternatives to the above TCEs.[18-20] Indeed being free of junctions, they exhibit high performance in terms of transmittance and sheet resistance, and have been successfully used in optoelectronic devices including OSCs. Typically, they are produced by patterning using lithographic techniques such as photolithography,[18] soft lithography,[19] phase shift lithography[20] and nanoimprint lithography.[21] Simpler recipes producing Ag grids using inkjet printing on polyethylene terephthalate (PET) suffer from relatively large feature sizes.[22, 23] Such printed patterns are often used as current collecting grids.[24-25]

In this Part, Ag metal wire network fabricated through crackle lithography have been tried to incorporate as a TCE in the fabrication of OSCs. The Ag wire thickness may cause shunting while integration of TCEs in the OSCs. For this purpose, ZnO barrier layer with higher thickness was endeavored to decrease the peak-to-valley roughness. The fabricated OSCs are well characterized using external quantum efficiency (EQE) measurements. The ITO reference OSC was fabricated to compare the performance of the devices.

IIIB.1.3 Experimental Section

Ag wire networked TCE was fabricated as discussed in the experimental Part-IIA. The Ag network derived TCE and ITO were cleaned with ethanol and dried with N_2 gas. A Zinc acetate solution (109.75 mg zinc acetate dihydrate, 30.5 µL ethanol amine and 1ml methoxyethanole) was mixed, stirred for at least two hours and filtered with 0.2 µm hydrophilic filter. To obtain 55 nm thick ZnO layer, 100 µL of zinc acetate solution was spin coated on TCE at 4000 rpm for 50 s, followed by heating at 150 °C for 5 min to convert zinc acetate to zinc oxide.[26] Different thicknesses for ZnO layers were obtained by repeating the above procedure. A 2.7 wt% of PCBM:P3HT (0.8:1) in chlorobenzene solution was stirred for 2 hours and filtered with 0.2 µm hydrophobic filter. A 80 µL PCBM:P3HT solution is spin coated on the ZnO coated TCE at 700 rpm for 60 s, followed by annealing at 130 °C for 15 min inside glove box. HTL – Solar PEDOT:PSS (Heraeus-Clevios) was ultrasonicated for 10 minutes and filtered with 0.2 µm hydrophilic filter. A 100 µL of the solution was spin coated on the active layer at 4000 rpm for 90 s and followed by annealing at 130 °C for 15 min in air. In the final step, 60 nm Au was evaporated on PEDOT layer using a thermal evaporator (BOC Edwards, Auto 306, FL 400). Four cells with different ZnO thicknesses (55, 95, 135 and 230 nm) were fabricated, each consisting of five cells (each cell, 0.2×0.8 cm^2).

Current-voltage characteristics were measured under standard AM 1.5 G spectral conditions at an intensity of 100 mW/cm^2 using a solar simulator (Newport-Oriel, 92250A-1000) and an electrometer (Keithley, Model 6517). Light source was regularly calibrated using a silicon solar cell (WPVS cell, ISE Call lab, Freiburg). External quantum efficiencies were measured with a PVE300 photovoltaic device characterization system (Bentham).

IIIB.1.4 Results and discussion:

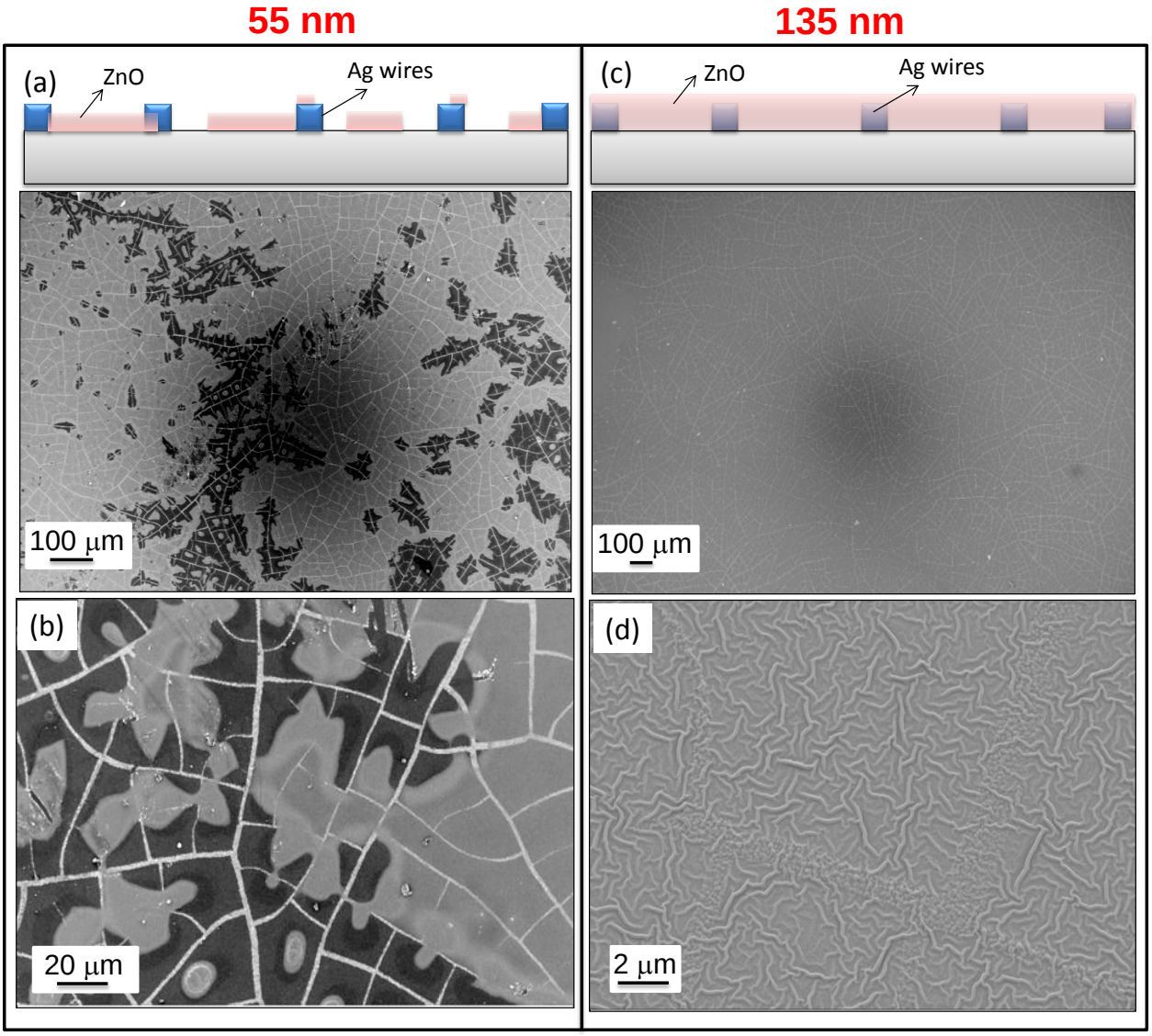

Figure IIIB.1.1 SEM images and schematic illustrations of Ag network TCE covered with ZnO for layer thickness of (a) & (b) 55 nm and (c) & (d) 135 nm.

The Ag wire network was fabricated on glass as described in Part-IIA. The metal fill factor is estimated to be ~ 20% with structural width of ~ 2 μm and average cell size (spacing between the Ag structures) of 20 to 60 μm. The surface roughness of network is estimated to be ~ 5 nm while the peak to valley roughness, which corresponds to network thickness, is 55 nm. Accordingly, the sheet resistance was found to be ~ 10 ohm/sq, which is rather low considering

the thickness of only 55 nm. The transmittance of Ag network was ~ 86% at 550 nm and the overall transmittance in the visible region is comparable to that exhibited by ITO but importantly, extends down to UV region.

In the next step of solar cell fabrication, ZnO barrier layer was brought in by decomposing zinc acetate film at 150 °C in air (see experimental part for details). For a proposed thickness of 55 nm of ZnO, the obtained layer was non-uniform and discontinuous (Figure IIIB.1.1a and 1b) as evident from the dark and grey regions, the latter corresponding to ZnO covered network. The non-uniformity in the ZnO layer thickness is attributed to the peak-to-valley roughness of Ag wire network. With increasing thickness (95 nm, 135 nm and 230 nm), an increment in the uniformity was observed. For example, SEM image of 135 nm ZnO layer shown in Figure IIIB.1.1c and 1d, ZnO film is seen to be uniformly submerging the entire Ag network. It w found to be the optimal ZnO thickness required to submerge Ag network so as to have reproducible devices without shorting.

Four bottom-illuminated inverted photovoltaic cells (5 devices in each) consisting of poly-3-hexylthiophene (P3HT) and phenyl-C61-butyric acid methyl ester (PCBM) were fabricated on a glass substrate as shown in the schematic in Figure IIIB.1.2a with Ag network derived TCE. The bar graphs of solar cell parameters (V_{oc}, J_{sc}, FF and η) for all the four cells with varying thicknesses of ZnO barrier layer are shown in Figure IIIB.1.2b. In cell 1, all five devices with 55 nm of ZnO layer were defective due to shorting. The J-V characteristics of cell 2, 3 and 4 are shown in Figure IIIB.1.3a, 3b and 3c, respectively. For cell 2 with 95 nm ZnO layer, only two devices were working with moderate efficiencies and remaining 3 devices were shorted (Figure IIIB.1.3a). This may be due to the non-uniform and uneven ZnO layer as in the case of 55 nm thickness (Figure IIIB.1.1b). On the other hand, for cells 3 and 4 with 135 and

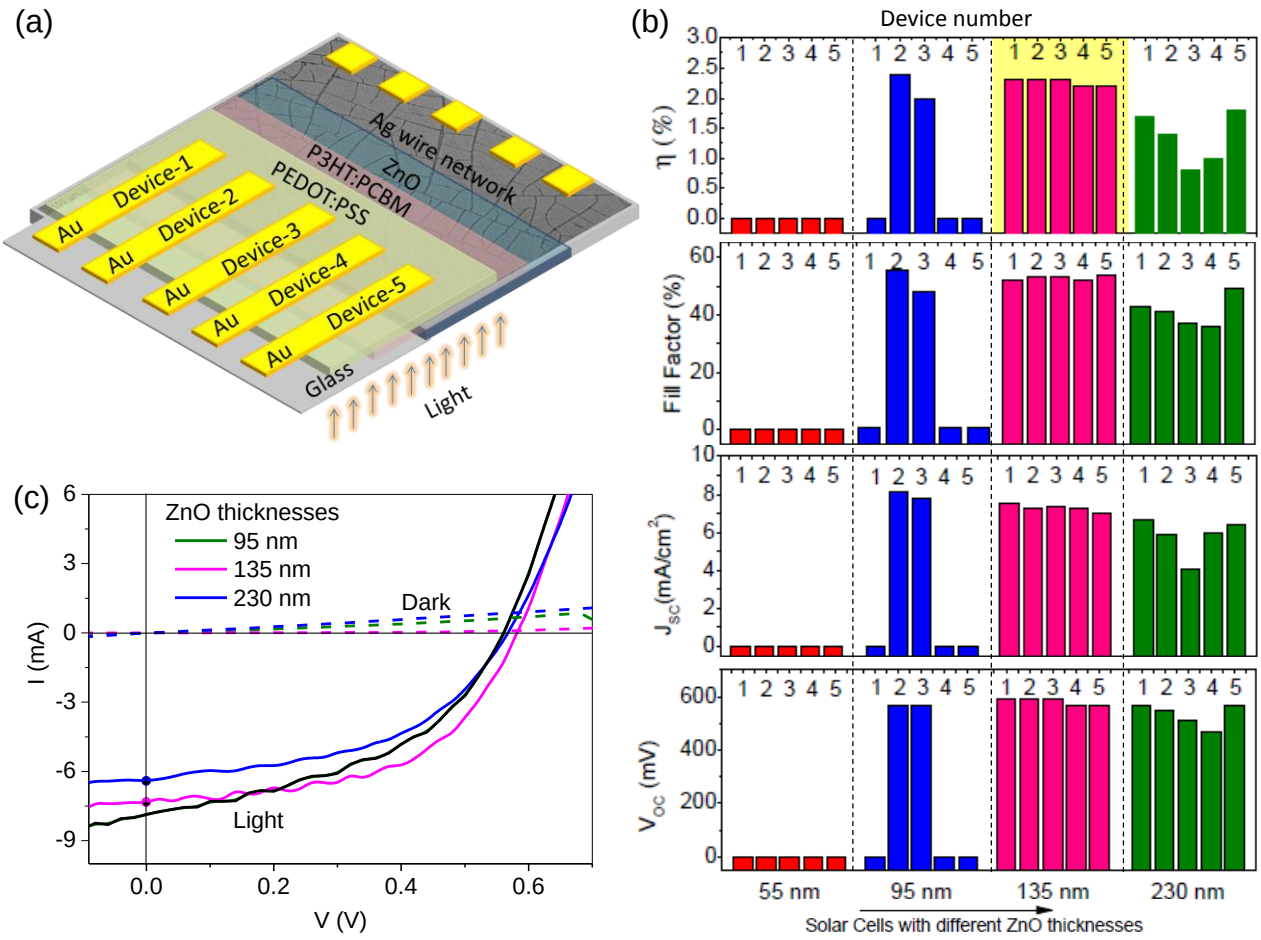

Figure IIIB.1.2 (a) Schematic illustration of the inverted P3HT-PCBM solar cell with Ag network TCE, (b) bar graph of cell parameters for solar cells of different ZnO layer thicknesses (55, 95, 135 and 230 nm), (c) examples of J-V characteristics of solar cells with different ZnO layer thicknesses in dark (dotted) and in light (continuous lines). Note that best performing solar cell is chosen from each cell.

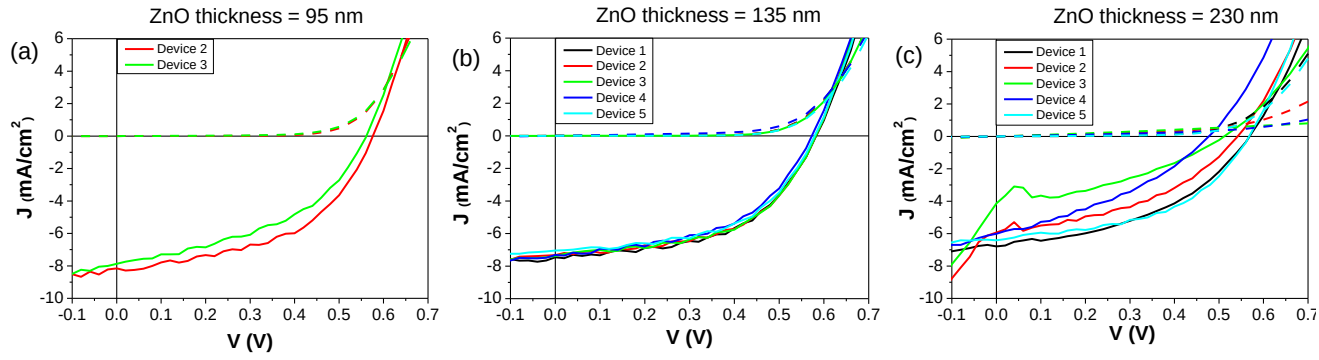

Figure IIIB.1.3 J-V characteristics of all working Ag wire TCE derived polymer solar cell with (a) 95 nm, (b) 135 nm and (c) 230 nm ZnO layer thicknesses.

230 nm ZnO barrier layer thicknesses respectively, all five devices were found to be functioning(Figure IIIB.1.3b and 3c). Significantly, with 135 nm ZnO (cell 3), the five devices showed uniform performance with average efficiency of 2.26 ± 0.05% while those from 230 nm ZnO, exhibited some variation in performance with lower efficiency (1.34 ± 0.43%, see Figure IIIB.1.2b). The decrease in the cell efficiency for higher ZnO thicknesses can be attributed to higher series resistance of the cell leading to lower current density and fill factor values.[27] Indeed, the variations in solar cell parameters among the five devices exhibited similar trend. J-V characteristics of typical solar cells with different ZnO layer thicknesses (95 nm, 135 nm, 230 nm) are shown in Figure IIIB.1.2c.

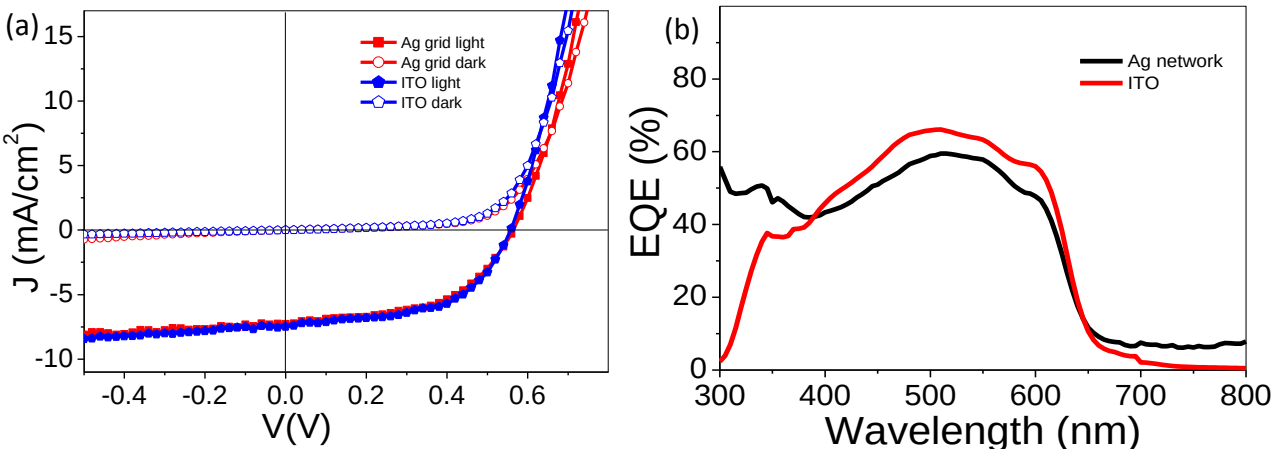

Figure IIIB.1.4 Comparison of (a) J-V characteristics and (b) EQE for optimized Ag network and ITO devices.

In Figure IIIB.1.4a, the J-V characteristics of a typical device fabricated using Ag network (from cell 3) compared with that produced using ITO as TCE (ITO: T= 93% and R_s= 16 ohm/sq). The Ag network cell has an optimum thickness of 135 nm of ZnO. For ITO device, the thickness of ZnO blocking layer was kept at 45 nm which is optimum for an inverted solar cell.[26] All other process parameters such as active layer thickness, top electrode, annealing temperature etc. were kept same for all devices. It is clear from the plot that Ag network TCE based solar cell follows a similar trend as the ITO based cell and the derived parameters are quite

comparable (see Table IIIB.1.1). Thus, the efficiency of Ag network TCE based solar cell was 2.14%, while that obtained for ITO based cell under similar conditions in ambient was 2.27%. These results presented here clearly demonstrate the potential of Ag network based TCE as an alternative to ITO in OSCs. However, a slightly thicker ZnO layer is required to cover the Ag network thickness. Since ZnO layer is filled in the interstitial domains between the metallic network, it improves the charge collection properties, which is similar to coating a PEDOT:PSS layer as reported for conventional metal grids.[28] The external quantum efficiency (EQE) measurements (Figure IIIB.1.4b) show that Ag network TCE based cell exhibited slightly less

Table IIIB.1.1: Summary of the solar cell parameters corresponding to J-V characteristics shown in Figure IIIB.1.4a.

TCE	ZnO thickness (nm)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	η (%)	R_{sh} Ω cm^2	R_s Ω cm^2 @ V_{oc}	R_s Ω cm^2 @ P_{max}
Ag grid	135	0.57	7.2	51.8	2.14	421	8.3	49.7
ITO	45	0.55	7.5	55.2	2.27	413	6.7	48.6

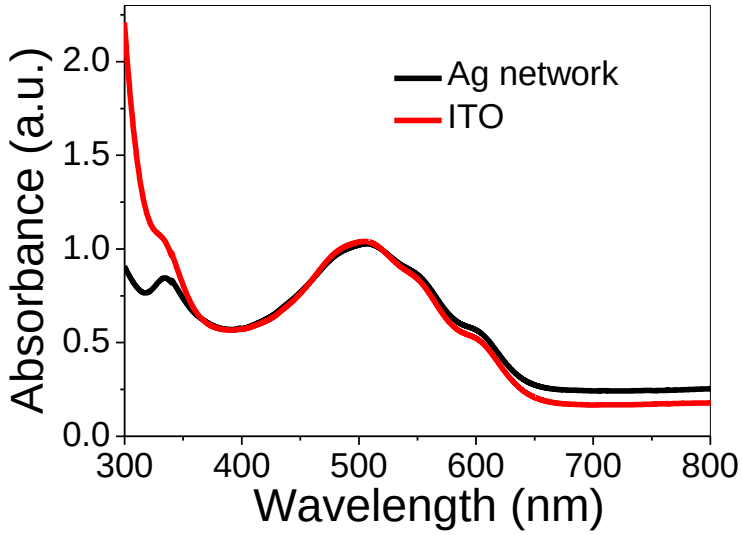

Figure IIIB.1.5 Absorbance of devices having Ag wire network and ITO TCEs.

values in the visible region compared to those derived from ITO cell, but in the UV region, the former excels which makes the overall performance similar for both cells. This can be clearly understood from the differences in transmission of the respective electrodes in the UV region. The same information can be inferred on comparing the absorption spectra of the two solar cells (see Figure IIIB.1.5) with their EQE spectra. The total absorbance of the (P3HT: PCBM) active layer together with ZnO layer, PEDOT:PSS and TCEs, (Ag network or ITO) is measured. As shown in Figure IIIB.1.5 the absorbance of the organic layer in both devices is very similar. The only difference corresponds to the difference in the absorption of ITO and Ag network in the UV region. However, the polymer ingredients (P3HT-PCBM) used are known to be UV degradable,[29] this study is meant to demonstrate the possibility of UV light harvesting using the metal network TCE.

The method developed in this study for TCE and associated OSC fabrication has several merits. While the present part has focused on only one type of metallic network, its scope of application can be easily extended to other thin film devices by varying the template thickness and other parameters in the initial stages of crack template formation. Few thin film devices have been demonstrated with the metal wire networks in the next parts of this thesis. Thus, it is possible to obtain TCEs with different network thicknesses, connectivity and importantly with different metals. Here, Ag was used as a typical example since the work function is favorable for inverted geometry P3HT-PCBM solar cell. However, it can be replaced with other metals such as Cu, Al, Pt depending on the need of application. The metal network based TCE used in the present study works as current collecting grid at tens of micrometer scale with a metal fill factor of 20%.

IIIB.1.5 Conclusions

The present study demonstrates the incorporation of a highly transparent and highly conducting Ag metallic network obtained using a crack template as described in Part-IIA, in a thin film organic solar cell. A 135 nm ZnO barrier layer was essential for the fabrication of OSCs without shorting. The performance of this highly scalable metal network as a TCE is comparable to that of conventional ITO electrode in the visible region, whereas in the UV region Ag network TCE performed better than ITO due to the wide spectral range transmission. This is a general approach to replace ITO in diverse thin film devices.

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IIIB.2 Semi-transparent organic solar cell and transparent capacitor

Summary

As transparency is becoming a desirable property in optoelectronic devices such as solar cell and even in non-optoelectronic devices, there is great impetus given to alternate materials and strategies replacing the conventional ITO. This part deals with the fabrication of semi-transparent solar cell and transparent capacitor with metal wire network derived from crackle lithography. Au wire network/PEDOT:PSS hydride TCE has been realized and integrated in semi-transparent organic solar cell. The semi-transparent solar cell has shown power conversion efficiency of 88.6% to that of standard reference device. The transparent capacitor was fabricated by sandwiching two Au wire networked TCEs in between a polymer ion-gel. The transparent capacitor thus fabricated with flexible PET as substrate, showed a capacitance of 2 $\mu F/cm^2$ at 1 Hz with average transmittance of ~ 68% and was stable after many bending cycles. Such a performance is made possible due to high transmittance (~86%) and low sheet resistance (~8 Ω/sq) of the Au wire network.

IIIB.2.1 Introduction

Solution-processed organic solar cells (OSCs) technology has made rapid progress as a potential alternative source of deriving solar energy in the past few years.[1,2] The research on organic solar cells have undergone major development in terms of active material with new acceptor and donor molecules,[3,4] electron and hole transport layers [5,6] and current collecting electrodes.[7,8] Primarily, upon moving from normal to inverted geometry of organic solar cells, vacuum evaporated, low work function Al metal is replaced with solution processed Ag.[9] Secondly, the use of transparent buffer layer at anode serves dual purpose of work function matching and also acts as hole transport layer thus increasing the performance of solar cells.[10]

In organic or dye sensitized solar cells,[11] the active layer at its optimized thickness is reasonably transparent to visible light which has prompted fabrication of transparent solar cells.[12-13] Taken together, all these developments have led to the possibility of semitransparent solar cells provided the anode is made visibly transparent.[13-15] The transparent solar cells are very attractive as a window panels or as a curtains, not only save space but also harvest energy.[16] Considering such advantages, there is a recent trend worldwide of extending these features even to non-optoelectronic devices. For instance, there have been reports on fabrication of transparent capacitors,[17, 18] transparent strain sensors,[19, 20] transparent speakers,[21] transparent batteries[22] and transparent gas sensors[23] Such fabrication of course, demands for more usage of the TCE as well as for additional attributes in a TCE such as flexibility.

Transparent conductive oxide, indium tin oxide (ITO) is an obvious choice for both top and bottom electrode for semi-transparent OSCs. The incorporation of ITO as a top transparent conducting electrodes has shown encouraging results with power conversion efficiency of 71.4% to that of standard reference device.[24] The recent efforts involve use of new generation transparent electrodes such as PEDOT:PSS,[25-27] graphene[28, 29] and metal nanowires[30-32] that have proved to be very promising as bottom electrode for OSCs as discussed in Part-IIA section IIA.1. The deposition of top electrode directly above the photoactive layer is challenging because of chemical, physical and mechanical compatibility issues with the solvent, processing steps and softness of the organic layer.[33] The soft lamination of top electrode might also result in printing defects, interfacial resistance and poor contacts.[34] Graphene electrodes are laid on top of active electrode by PMMA assisted transfer[35] while CNTs and metal nanowire electrodes are prepared directly by drop coating or spray coating based solution processes

resulting in a 2-D percolating network.[36] The carbon nanotubes have not been much successful as top electrode for solar cells due to bundles formation, junction resistance, non-crossed nanotubes and roughness that can cause significant shunting and shorting with the bottom electrode.[37] The Ag nanowires faces similar problems most of which are addressed by external means as discussed in chapter-IIIA section IIIA.1.

IIIB.2.2 Scope of the present investigation

There have been successful attempts in the literature to employ Ag NWs as cathode to realize transparent solar cell to avoid any risks of shorting the device.[13] Although, they need either mechanically, thermally or electrically inducing welding of nanowires or by turning these into composite structure. All these endeavors have proven that metal mesh or gratings is the most efficient approach for constructing a top electrode for organic solar cells.[38] Not only the conventional lithography methods for sub-micron patterning are tedious and expensive, the resulting periodic features in form of mesh and gratings can result in increased diffraction effects. The aesthetically transparent solar cells require clear- view through visibly transparent electrodes with lower haze. The TCEs fabricated with less roughness and low haze has great importance.

The metal wire network fabricated through crackle lithography is ideal to use as a top top-illuminated electrodes for OSCs. These electrodes have already been demonstrated (Part-IIIB.1) to work well as transparent electrodes under bottom illumination with efficiencies around 2%. The utilization of these networks for top-illuminated electrodes is an altogether different play. Their fabrication directly on top of inverted OSCs assembly without any damage to the organic layers beneath is a challenging task. For this purpose, the integration of metal wire network and PEDOT:PSS hybrid electrodes in OSCs fabrication have been attempted. The

PEDOT:PSS was chosen as a composite material for metal wire network, which serves as a barrier layer and interconnects the void space in between the network. Further, this study is focused on exploitation of these TCEs in the fabrication of transparent capacitor. Such transparent capacitors find applications in the integration of transparent solar cells for window panels.[16] Few efforts have been made to fabricate transparent and flexible capacitor with polymer ion gel dielectric.

IIIB.2.3 Experimental Section

Fabrication of Au Mesh Network/PEDOT hybrid electrode: Glass substrates were washed and ultrasonicated in water, acetone and IPA, respectively. The substrates were dried with N_2 gun before use. In the second step, commercially available acrylic resin nanoparticle dispersion (Ming Ni Cosmetics Co., Guangzhou, China) was diluted to achieve a well dispersed solution of 0.6 g/mL concentration using commercially available diluter (Ming Ni Cosmetics Co., Guangzhou, China). The diluted dispersion was spin coated on PEDOT:PSS coated glass substrate at 1000 rpm for 120 s. In the next step, Au metal was deposited using a thermal evaporator (BOC Edwards, Auto 306, FL 400 and Hind High Vacuum Co., India). In the final step, the crack template is removed by dissolving in either chloroform or acetone or ethyl acetate (see Figure IIIB.2.1). As fabricated transparent conducting electrodes, were further characterized using several tools. The fabrication of OSCs was carried out as discussed in Part-IIIB section IIIB.1.3.

Fabrication of transparent capacitor: Capacitor devices were fabricated by spin coating the electrolyte gel onto two identical Au wire network electrodes, each of 3 X 1 cm^2 area. An electrolyte gel comprising of PMMA and 1-ethyl-2-methylimidazolium bis (trifluoromethanesulfonyl)imide was spin coated at 1000 rpm onto both electrodes. The two

electrodes were placed on top of each other and the devices were encapsulated using pressure sensitive adhesive (3M 467MP). The C-V measurements were performed using Keithley 4200 semiconductor parameter analyzer for all frequencies. The voltage was scanned from -2 to 2 V.

IIIB.2.4 Results and discussion:

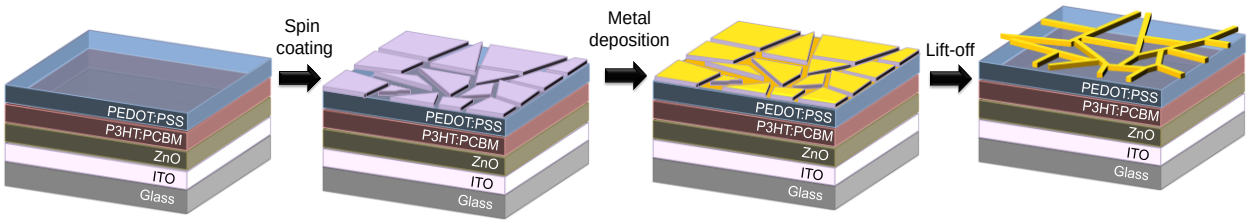

Figure IIIB.2.1 Schematic illustrating the fabrication of organic solar cell.

A transparent solar cell requires both the bottom and top electrode to be visibly transparent along with the active organic layer. Since P3HT:PCBM active layer absorbs in the visible region ~ around 550 nm, it can result in a semitransparent organic solar cell. ZnO and P3HT:PCBM layers were laid on ITO as bottom transparent electrode, in the standard configuration of organic solar cells. The top electrode i.e Au mesh network/PEDOT:PSS hybrid electrode is fabricated directly on top of the solar cell active layer (P3HT:PCBM) (see Figure IIIB.2.1). The metal wire network mesh is basically made up of seamless junctions and the issues related to roughness arising from standing of the wires are completely avoided. The integration of hybrid electrode with the solar cell is shown schematically in Figure IIIB.2.1. The entire fabrication for the hybrid electrodes was done directly on solar cell assembly. The solar cell assembly consists of ITO, ZnO and P3HT:PCBM layers above which PEDOT:PSS and Au wire network derived hybrid electrode is fabricated by spin coating of crack template, metal deposition, followed by lift-off. The solvent used for dissolving crackle template is acetone which does not have any impact on the P3HT:PCBM layer as it is masked by the underlying PEDOT layer.

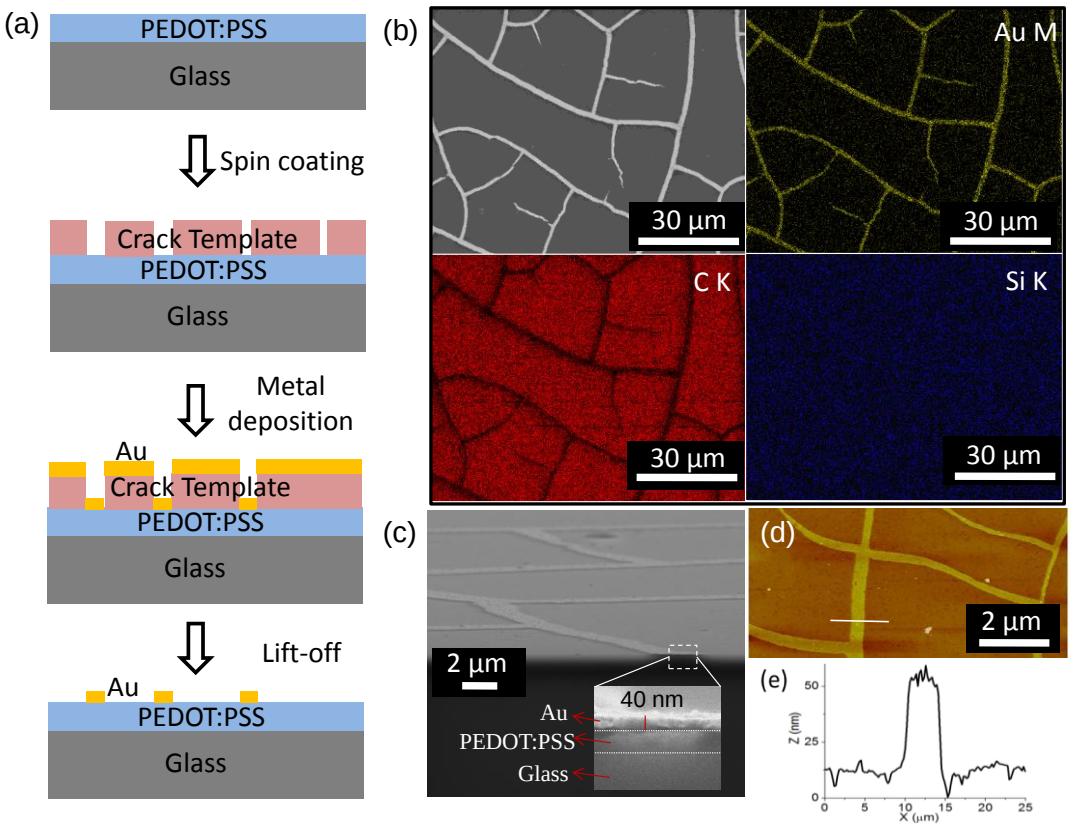

Figure IIIB.2.2 Schematic illustration (a) PEDOT: PSS coated glass substrate, following spin coating of crack template, Au deposition and removal of crack template by lift-off. (b) SEM image and corresponding EDS maps of Au K, C K and Si K. (c) SEM image showing the Cross-sectional view and (d), (e) AFM image along with height profile of Au mesh network/ PEDOT:PSS.

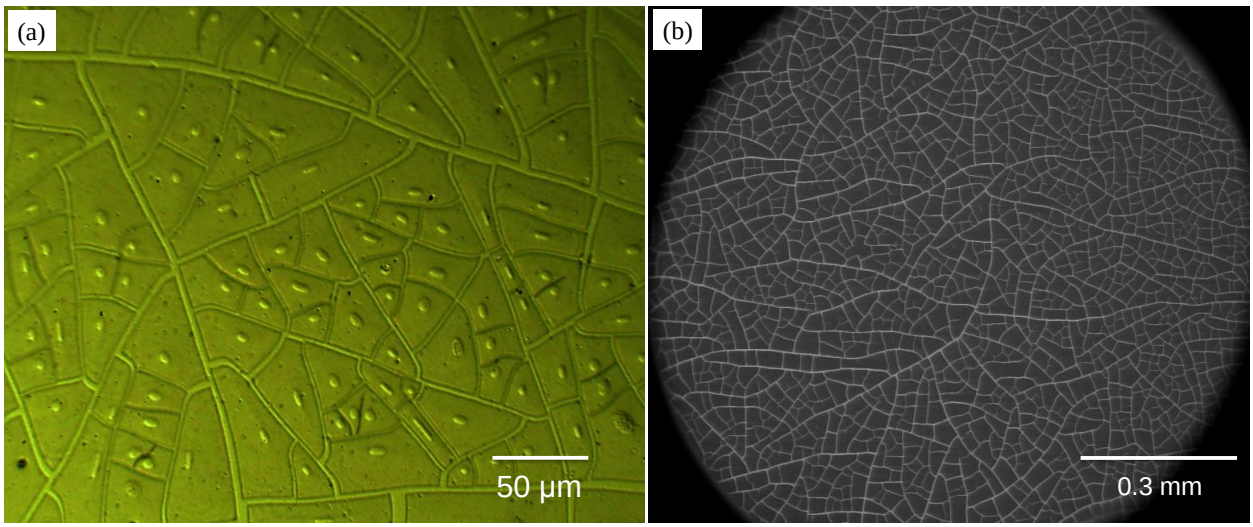

Figure IIIB.2.3 (a) Optical micrograph of crackle patterns formed on PEDOT:PSS layer. (b) SEM image of Au mesh network/PEDOT:PSS over 1 mm^2 area.

The basic fabrication process flow for hybrid electrodes is schematically shown in IIIB.2.2a. Instead of usual approach of laying PEDOT:PSS film on metal network,[9] metal wire network was laid on top of PEDOT:PSS (50 nm). Following, the crackle precursor was spin coated on the PEDOT:PSS surface resulting in spontaneous formation of cracks (see Figure IIIB.2.3a, optical micrograph image of crack template on PESOT:PSS). Interestingly, irrespective of the surface property, the crackle precursor is able to crack without any external aid. Moreover, crackle grooves run down to the PEDOT:PSS surface which is filled in with Au (40 nm) by slow thermal evaporation (~2 Å/s) in vacuum. The crackle layer is easily dissolved away by dipping in chloroform without affecting the PEDOT layer beneath. Several samples of different Au thicknesses were ranging between 20-60 nm were prepared following same procedure as discussed in Section IIIB.2.3. A typical electrode, Au (40 nm) mesh network/PEDOT hybrid was thoroughly characterized by host of characterization techniques as shown in Figure IIIB.2.2. SEM images and its corresponding EDS maps of Au wire network fabricated on top of the PEDOT:PSS are shown in Figure IIIB.2.2b. From SEM image, it is seen that the wires at the junctions are well connected without any defects (see Figure IIIB.2.2b). The Au mesh wire widths varied from several hundreds of nm up to 2 μm while the average distance between the wires (cell size) is ~30 μm resulting in metal fill factor of ~ 12%, similar to the networks fabricated on glass/PET sheet. The Au mesh network is continuous over large areas on PEDOT:PSS layer (see Figure IIIB.2.3b, SEM image of Au mesh network/PESOT:PSS). The Au M, C K and Si K signals in the EDS map reveals the presence of Au, C and Si respectively. Since Au is fabricated directly on top of PEDOT:PSS, the signal from Au wires is clearly visible while the C K signal is negative of Au K. This is due to the thickness of Au being more than the penetration depth of secondary electrons, mask the PEDOT:PSS below it. The signal from C K

(red) arising from PEDOT:PSS is stronger in intensity than Si K (blue) arising from glass substrate, as expected to be the case. Moreover, the uniform distribution of C K signal in the void regions of the network shows that PEDOT:PSS is defect free even upon development of crack template (see Figure IIIB.2.2c). The Si K signal is much weaker, due to the presence of ~50 nm PEDOT:PSS layer as seen from the cross-sectional image in Figure IIIB.2.2d. The good interfacial contact between Au metal and PEDOT:PSS layer is crucial for efficient charge collection in OSCs. The AFM image and the corresponding height profile (Figure IIIB.2.2e) over the hybrid electrode shows smooth surface of PEDOT:PSS beneath the Au wire. As seen from the AFM analysis in 2 × 2 μm^2 region (marked as 1), the average roughness (R_a) is ~ 5 nm. The average R_a of the Au wire network/PEDOT:PSS hybrid electrodes over entire 10 × 10 μm^2 area is 9 nm, while the peak to valley roughness is 47 nm. Since the metal fill factor per unit area is considerably low (~12%), the overall roughness R_a is significantly reduced.

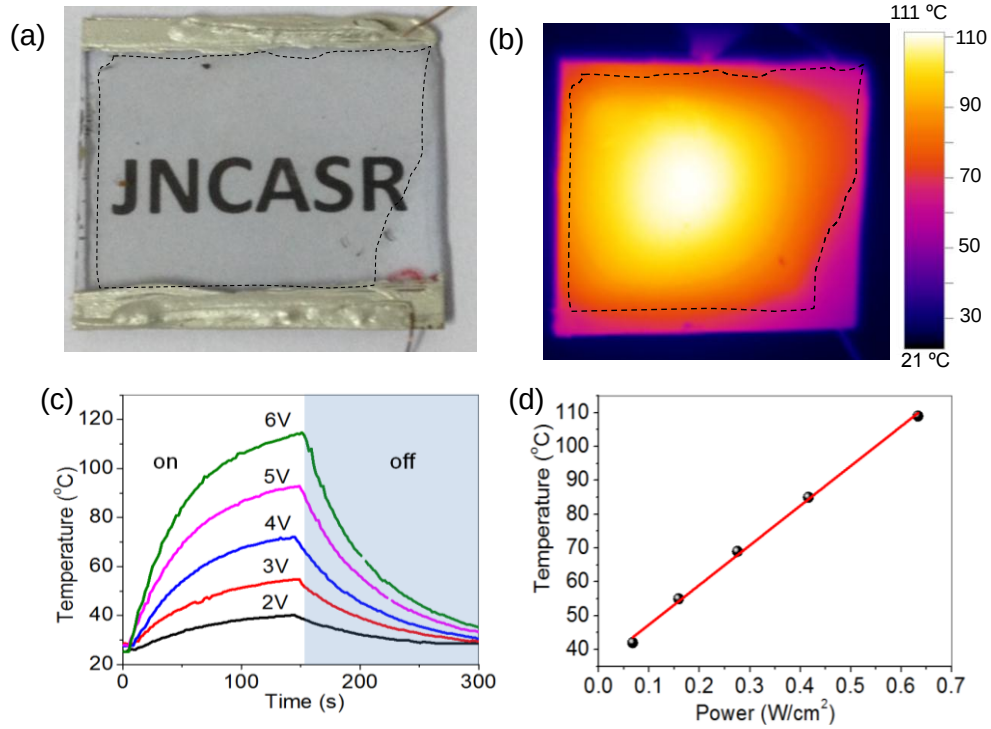

Figure IIIB.2.4 (a) Digital photograph (b) thermal image (at 6 V DC bias) of Au mesh/PEDOT hybrid electrode (see the dashed line region). (c) Temperature profiles as a function of time for a different applied voltages. (d) The maximum temperature achieved as a function of input power.

The electrodes fabricated in this way appear to be highly transparent as seen in Figure IIIB.2.4a**.** The letters behind the electrode indicates high optical transmission. The electrode exhibit a sheet resistance of ~ 3 Ω/sq which is significantly lowered by 3 orders of magnitude as compared to the PEDOT:PSS that has resistance of ~ 1.5 kΩ/sq. The uniformity in resistance is clearly seen by the homogeneous temperature distribution across the thermal image when the electrode is subjected to a DC bias of 6V (see Figure IIIB.2.4b). A noticeable temperature gradient is observed in IR image of Figure IIIB.2.4b. This is due to the shape of the transparent conducting electrode, marked with dotted line in the Figure IIIB.2.4a and b. Electrothermal joule heating behavior through the transparent electrode is shown in Figure IIIB.2.4c. With increase in the input voltage the maximum temperature achieved was increased, as soon as voltage was turned off substrate came back to room temperature. The maximum temperature of the hybrid TCE is linearly proportional to the input power as shown in Figure IIIB.2.4d. Thus, the Au mesh/PEDOT hybrid electrode showed a uniform heating via joule heating, which can be employed in various optoelectronic devices.

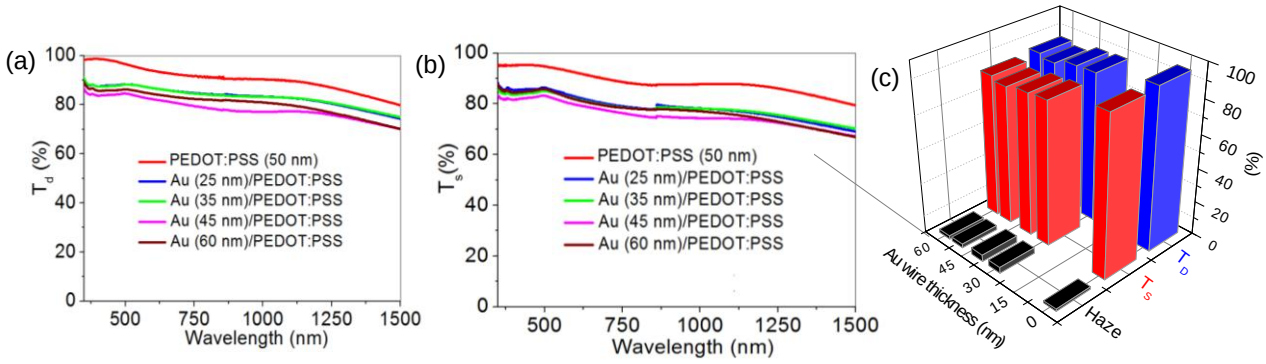

Figure IIIB.2.5 (a) Diffusive and (b) specular transmittance spectra (350 to 1500 nm) (c) Variation in T_S, T_D and Haze with Au wire thickness on top of PEDOT:PSS layer.

The study of optoelectronic properties for other electrodes with varying Au wire thickness was carried out in detail. Figure IIIB.2.5a shows the optical transmission spectra over a broad spectral range corresponding to diffusive transmittance (T_D) with average transmittance

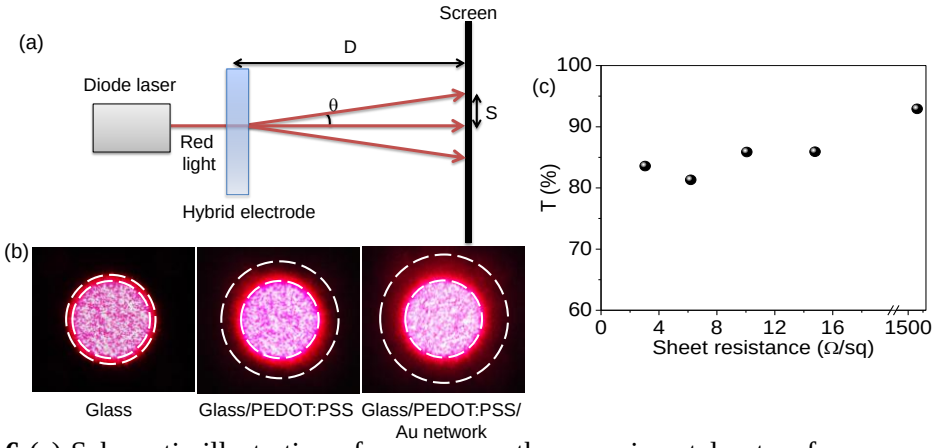

Figure IIIB.2.6 (a) Schematic illustration of the experimental setup for measuring angular distribution of diffusely scattered light. (b) The photographs of Angular distributed laser light after scattered light from glass, glass/PEDOT:PSS and glass/ PEDOT:PSS/Au network hybrid electrodes. (c) Transmittance versus sheet resistance for Au mesh network/PEDOT:PSS hybrid TCE with varying Au wire thickness.

between 70 - 85% similar to that of specular transmittance (T_S). The transmittance of hybrid electrodes is lowered by ~10-15% with respect to PEDOT:PSS thin film indicating that the network is highly transparent owing to low metal fill factor. Using average values of Ts and T_D as plotted in Figure IIIB.2.5c, the haze of the electrodes is calculated using relation, Haze (%)= (T_D-T_S/T_D). It refers to the percentage of light diffusely scattered through a transparent surface with respect to the total light transmitted. Haze is an important parameter to determine optical visibility especially those applications where transparency is concerned. Interestingly, the electrodes exhibit ultralow haze of ~ 5% for metal thicknesses up to 60 nm. The angular distribution of diffusely scattered light is determined using a simple optical set up with a laser pointer illuminating the hybrid electrode surface (see Figure IIIB.2.6a). The scattered light is directed towards the screen and captured with a camera. The radial spread of the laser light spot is calculated using the following equation, $\tan\theta = S/D$

The angular distribution of the diffused light is seen in the photographs of Figure IIIB.2.6b. The narrow distribution of the spot shows that specular transmission dominates over diffusive component with an angular spread for PEDOT:PSS layer and Au mesh network/PEDOT:PSS

hybrid electrode ~ 0.3° and 0.5°, respectively (see Figure IIIB.2.6b). These angular spread values can be less as compared to that of Ag nanowire derived TCEs.[39] The ultralow haze values for these electrodes are attributed to low fill factor and reduced surface roughness. Figure IIIB.2.6c shows the overall relation between transmittance and sheet resistance variation for the various electrodes prepared for this study. The overall resistance remains significantly low with increase in transmittance essentially overcoming the tradeoff between the two counteracting properties.

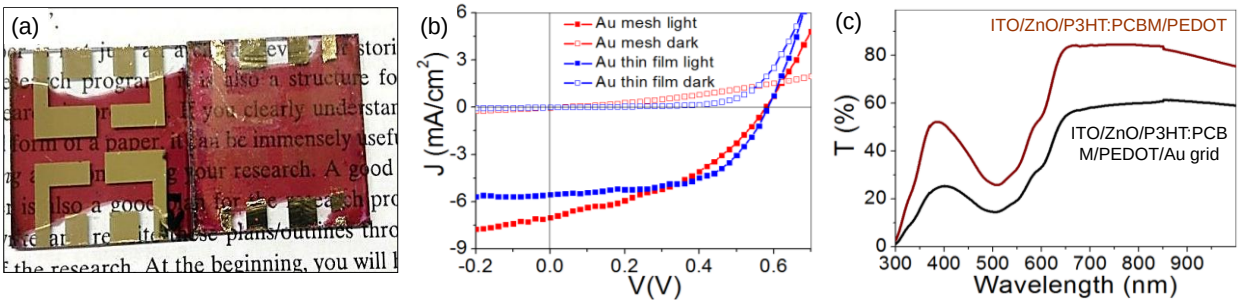

Figure IIIB.2.7 (a) Photograph of the organic solar cells fabricated with Au mesh network/ PEDOT:PSS transparent conducting electrode and with PEDOT:PSS/Au thin film. (b) J-V characteristics and (c) transmittance of the solar cell with and without Au top grid electrode.

The high performance of hybrid electrodes makes them highly suitable for solar cells application as discussed in Part-IIIB.1. The performance of Au wire hybrid electrodes were compared with a reference solar cell fabricated with a continuous Au thin film, under similar conditions of fabrication (Figure IIIB.2.7a). The J-V characteristics of the polymer solar cell with Au thin film and with Au wire network is shown in the Figure IIIB.2.7b. Au wire network derived solar cell has shown more dark current as compared with Au thin film reference solar cell. There is a low and steady slope in dark current of Au wire networked solar cell, which may be due to low shun resistance and high series resistance. The fill factor of Au wire network is less(light current) as compared to reference cell, may be due to the pin holes and defects caused during the lift-off of the crackle template. The devices made with Au mesh electrodes does not require any voltage shock for burning shunts which is reported by several groups as an important step for measuring organic solar cells.[9] As seen from the J-V characteristics in Figure

IIIB.2.7b, the efficiency of the polymer solar cell with hybrid TCE (1.64%) is very close to that of Au thin film (1.85%). All the devices fabricated in this study are tested in an ambient environment except active layer annealing which is probably the reason for moderate efficiency values. As seen in Table IIIB.2.1, the present Au mesh network derived P3HT:PCBM based organic solar cells performance is compared with literature results.

Additionally, the solar cell fabricated with hybrid TCE is quite transparent as shown in the photograph of the Figure IIIB.2.7a. It is clear from the photograph that the letters behind the transparent solar cell are visible, while the solar cell made with continuous Au thin film is opaque (see Figure IIIB.2.7a). The transmittance spectra of the solar cell with and without Au wire network are shown Figure IIIB.2.7a. The transmittance of solar cell is ~55% at 650 nm wavelength. There is a 15-24% decrease in the transmittance due to the Au wire network. The transmittance of the solar cells also depends on the thickness of the active layer apart from the top electrode. The further optimization of P3HT layer thickness may be required to improve transmittance without sacrificing much on performance. Further, use of new active materials that absorb in NIR while transmitting in visible may result in completely transparent solar cells. This is first hand proof of concept for the top electrode that is directly integrated over active layer for the fabrication of semi-transparent solar cell.

Table IIIB.2.1: Tabulation of photo-conversion efficiency for transparent top illuminated inverted organic solar cells with that of a standard reference solar cell with metal top electrode.

Ref No.	Top Electrode	$T_{device,\ 650\ nm}$ (%)	$\eta_{Semitrans}$ (%)	$\eta_{ref,metal}$ (%)	$100 - \left(\frac{\eta_{ref} - \eta_{semitrans}}{\eta_{ref}}\right)$(%)
40	3 layer Graphene	65	0.69	3.30	29
	10 layer Graphene	-	2.5	3.3	76
41	Ag NWs-TiO_2 composite	58	3.82	6.03	63.35
42	Ag NWs		2.2	3.5	62.6
43	AgNWs		2.1	2.6	80.77
44	Ag NWs	55	2.0	2.9	69
Present work	Au Mesh- PEDOT composite	57	1.64	1.85	88.6

Transparent capacitor:

Transparent and flexible capacitor is an important device for realization of new generation transparent and bendable circuitry in displays and in energy storage, particularly in combination with solar cells. This study is focused on fabricating transparent capacitors using the Au wire network based TCEs as parallel plate electrodes with a transparent dielectric in between. The Au wire network is fabricated on PET sheet as described in Part-IIA section IIA.3. Thus produced wire network is very well connected across the area without any defects as revealed by the optical profilometry image (Figure IIIB.2.8a). The sheet resistance (R_S) of the TCE was ~ 4.2 Ω/sq. A line profile in Figure IIIB.2.8a shows Au wire width to be ~ 2 µm and thickness ~ 70 nm, the latter being also the peak-to-valley roughness of the mesh. The estimated surface

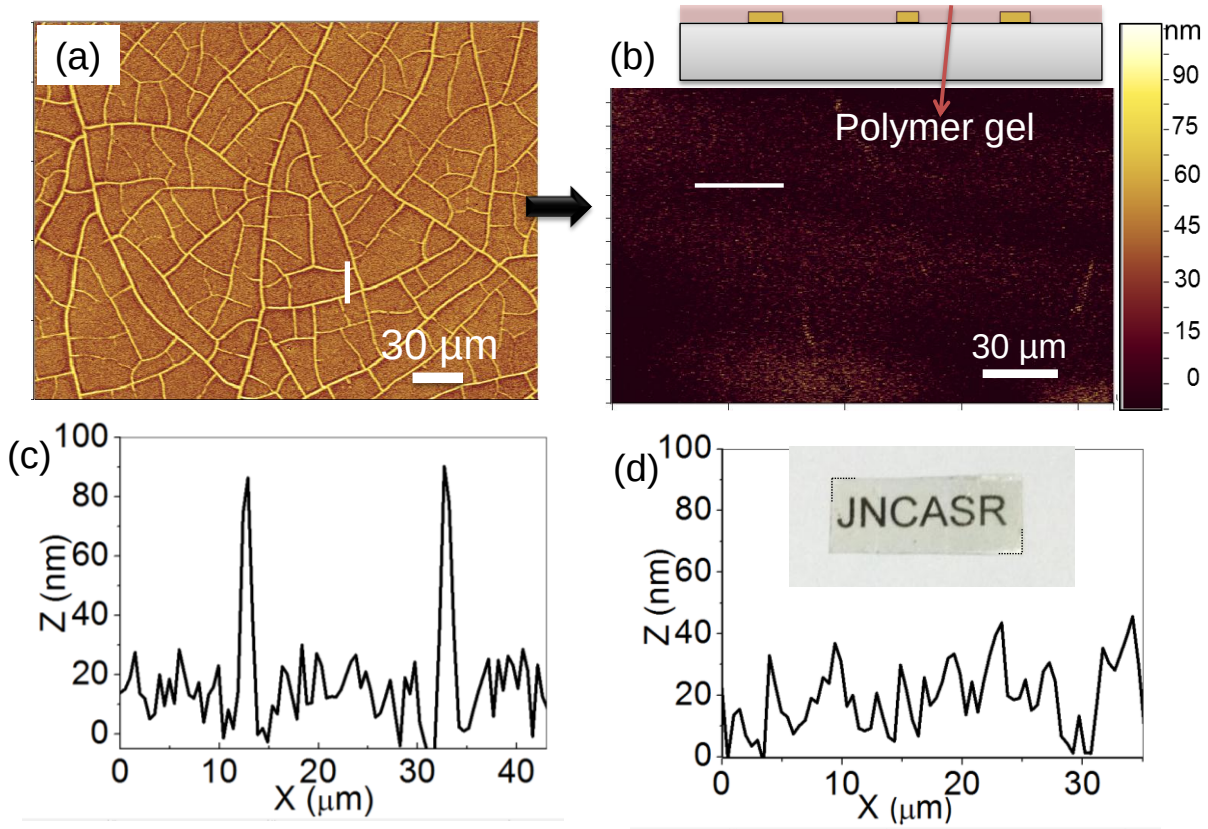

Figure IIIB.2.8 Optical profilometry image Au wire network (a) before and (b) after polymer-gel coating, (c) and (d) are corresponding height profiles along the lines marked in 'a' and 'b', inset in 'd' is the photograph of the Au wire network coated with the polymer-gel.

roughness of the wire mesh was of ~ 20 nm, which may arise due to residual precursor along with some contribution from the inherent roughness of the PET substrate. As shown in Figure IIIB.2.8b, the polymer-gel was spin coated to a thickness of ~20 µm when the surface became smooth (~ 10 nm roughness). The line profiles taken before and after coating the polymer-gel clearly demonstrate that the metal network got buried (compare Figures IIIB.2.8c and 8d). The electrode coated with the polymer-gel appeared quite transparent as shown in photograph in the inset of Figure IIIB.2.8d.

A parallel electrode capacitor was fabricated using two similar Au wire mesh TCEs coated with the polymer ion gel and assembled as shown in Figure IIIB.2.9a. The optical microscope images collected focusing on top and bottom TCEs show the two wire networks, one

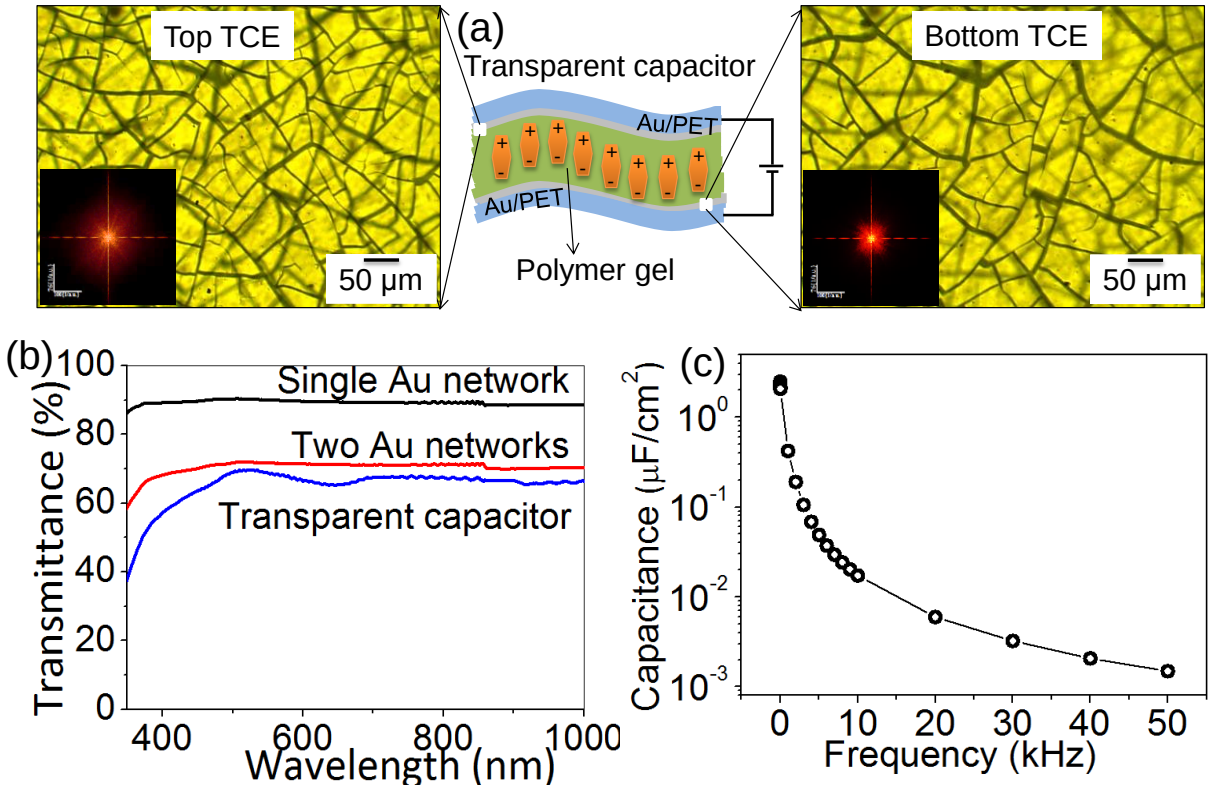

Figure IIIB.2.9 (a) Schematic illustration (middle) and optical micrographs of the fabricated transparent capacitor, with top (left) or bottom (right) TCE is held in focus. Corresponding FFT patterns are shown in the insets. (b) Diffusive transmittance spectrum of an encapsulated transparent capacitor along with those of Au wire mesh based TCEs, single and two together. (c) Capacitance as a function of frequency from 1 Hz to 50 kHz.

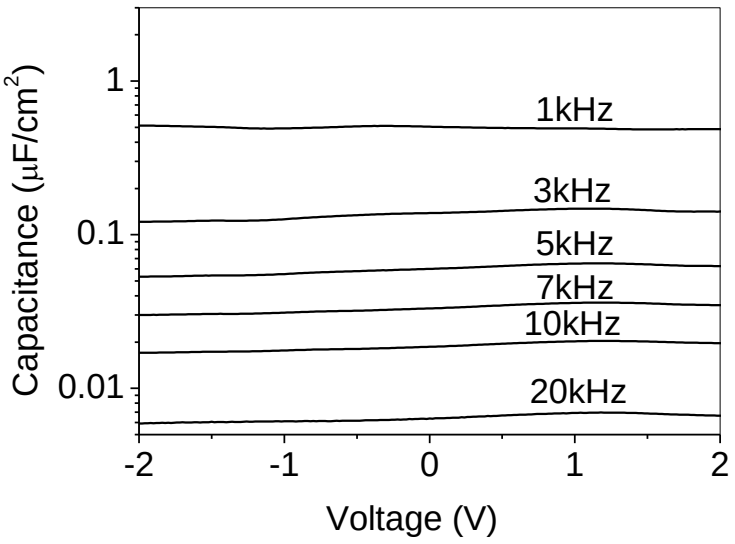

Figure IIIB.2.10 C-V curves of the transparent capacitor at different frequencies from 1-20 kHz.

in focus and the other out-of-focus (see either sides of schematic in Figure IIIB.2.9a). Since each TCE is a random network of wires, stacking two of them did not produce any shadowed regions. The corresponding FFTs shown in the insets are free of any Moire diffraction patterns, which are considered in general detrimental to display. Figure IIIB.2.9b clearly shows that the transmittance of a single TCE is ~ 89% which gets reduced to 69% for the integrated capacitor device. This value is only slightly less compared to that from the stack of two TCEs, the difference being due to the polymer gel and the encapsulant. The active area of the transparent capacitor was 1 cm^2 though the metal occupied only 15% of the total area (metal fill factor). Therefore, the effective capacitor area is just 0.15 cm^2, which is contributing for the total capacitance of the device. The obtained C-V curves are shown in Figure IIIB.2.10. As shown in Figure IIIB.2.9c capacitance decreases with frequency, from 2 $\mu F/cm^2$ at 1 Hz to 0.001 $\mu F/cm^2$ at 50 kHz, due to the limited polarization of ions at higher frequencies. The other two devices fabricated in a similar way, exhibited 2 and 20 $\mu F/cm^2$ at 1 Hz, respectively. The metal electrode wall width and fill factor variations can bring in such changes in capacitance which has not been studied in this study. It may be noted that the capacitance values mentioned here refer to the total

area and not just the metal filled area. Moreover, as a polymer ion gel electrolyte was used, it is essentially an electric double layer capacitor.[45] The present transparent capacitor has exhibited similar capacitance values as compared to normal (opaque) capacitors in the literature.[46,47] The transparent capacitor may be compared with literature results (see Table IIIB.2.2). The high capacitance values obtained in this study owe much to the ion gel dielectric.

Table IIIB.2.2: Literature table comparison with other transparent capacitors

S.No.	Dielectric	Dielectric thickness (μm)	Transparent electrode	Capacitance	Transmittance (%)	Flexible	Reference
1	Polyvinyl acetate	45-75	Single walled carbon nanotubes	0.1 nF/cm^2	74	yes	48
2	$Bi_2Mg_{2/3}Nb_{4/3}O_7$	0.2	Graphene	2.2 nF/cm^2 @ 1 kHz	70	yes	49
3	$Bi_2Mg_{2/3}Nb_{4/3}O_7$	0.2	$Al_{0.016}In_{0.003}Zn_{0.981}O$	3.1 nF/cm^2 @ 0.1 kHz	80	Perhaps	50
4	SU8 /Epoxy resin	45	Graphene	0.1 pF/cm^2 @ 320 Hz	NA	yes	51
5	Ecoflex silicone elastomer	300	Single walled carbon nanotubes	0.8 μF/cm^2	NA	Perhaps	52
6	Ion-gel	~20	Au wire network	2 μF/cm^2 @ 1 Hz	68	yes	Present work

The capacitance of a parallel plate capacitor can be defined as

$$\mathbf{C = \varepsilon A/d}$$

Where

C = Capacitance

$\varepsilon = \varepsilon_r \varepsilon_o$ = dielectric constant

ε_r = relative permitivity

ε_o = vacuum permittivity

A = area of the capacitor = L × W × FF

L = length of the electrodes

W = width of the electrodes

FF = Fill factor of the metal network

d = Spacing between the electrodes

The ability of a substance/material to store electrical energy in an electric field is called permitivty. This constant is equal to approximately 8.85 x 10^{-12} (F/m) in free space (vacuum). In the present case capacitance is directly propotional to the FF of the metal network. On the other hand transmittance is inversly prapotional to FF. The FF of TCE used in the capacitor fabrication is ~ 12%, which is a good compromise between the capacitance and transmittance.

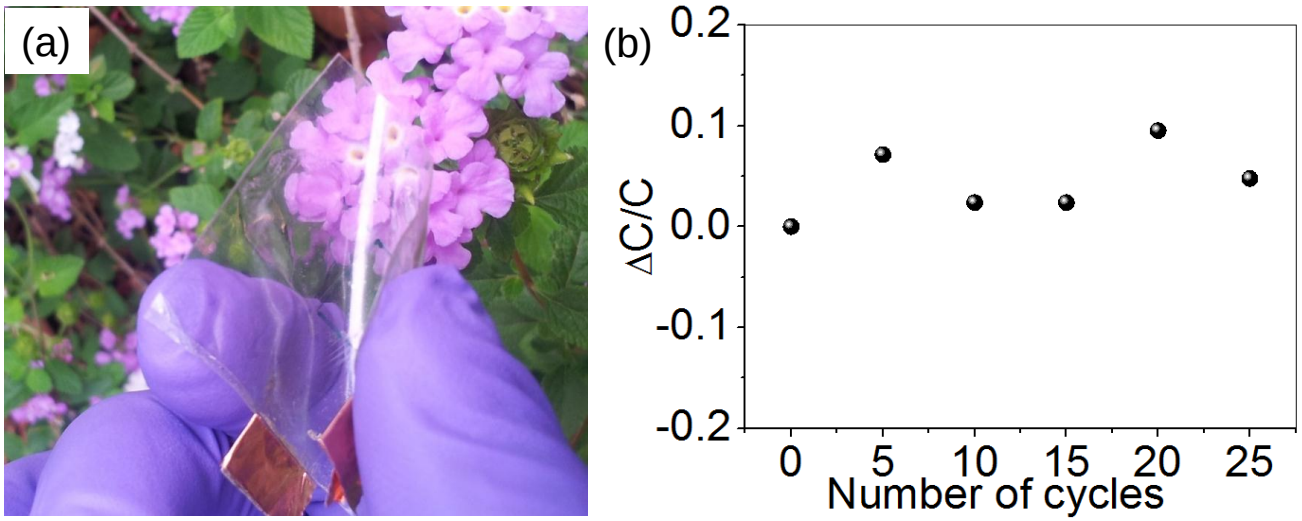

Figure IIIB.2.11 (a) Photograph of the transparent capacitor when it is bent. (b) Relative change in the capacitance as a function of bending cycles. Every fifth cycle, the capacitance was measured.

In order to determine the flexibility, the transparent capacitor is bent as shown in the Figure IIIB.2.11a. Since the PET substrate and the polymer dielectric, both are flexible in nature, the resulting capacitor is also flexible (Figure IIIB.2.11a). The capacitance was monitored under flexing cycles and it was found to be almost unaffected even after several bending cycles (Figure IIIB.2.11b). The capacitor was stable ever after 30 days without any degradation in the performance. Thus, the fabricated capacitor with metal wire network is not only transparent but also flexible. Such transparent capacitors find applications in the integration of solar cells for window panels.[53]

IIIB.2.5 Conclusions

This study demonstrated that such hybrid electrodes can readily be formed right on top of the active layers of polymer solar cell, rather than fabricating the hybrid electrode separately and integrating with solar cell. Thus, the fabricated solar cells are semi-transparent. The fabricated electrodes are intended for more efficient charge collection in optoelectronic devices such as solar cells, light emitting diodes etc. These electrodes are different from the fabricated Ag nanowire/PEDOT:PSS hybrid electrodes, where PEDOT:PSS coating was done over Ag nanowire network. The hybrid electrodes fabricated in this method are useful as top electrode for the integration semi-transparent solar cells. These hybrid electrodes are chemically, physically, mechanically and thermally robust as compared to Al or even Ag.

The study has even dealt with the fabrication of a transparent capacitor using Au wire network based transparent conductors as electrodes. Here, capacitor as a device was chosen as an example to demonstrate the capability of the wire electrodes. The devices showed capacitance in the range of 2-20 $\mu F/cm^2$ at 1 Hz frequency and were highly flexible. It is envisaged that transparent energy storage devices such as one shown above may find niche applications in combination with semi-transparent solar cells.[53] The demonstration of a working transparent capacitor and a semi-transparent solar cell provides evidence that the electrodes can be easily adapted in successful integration of devices.

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IIIB.3 Curved and flexible transparent heaters

Summary

Transparent conducting electrodes (TCEs) have been made on flat, flexible and curved surfaces following a crack template method in which a desired surface was uniformly spray coated with a crackle precursor and metal (Ag) was deposited by vacuum evaporation. An acrylic resin (CP1) and a SiO_2 nanoparticle based dispersion (CP2) derived from commercial products, served as crackle precursors to produce U-shaped cracks in highly interconnected networks as in the case of drop coating or spin coating. The crack width and the density could be controlled by varying the spray conditions resulting in varying template thicknesses. By depositing Ag in the crack regions of the templates, Ag wire network TCEs were produced on flat-flexible PET sheets, cylindrical glass tube and convex lens surface with transmittance up to 86%, sheet resistance below 11 Ω/sq for electrothermal application. When used as a transparent heater by joule heating of the Ag network, AgCP1 and AgCP2 on PET showed high thermal resistance values of 515 and 409 °C.cm^2/W respectively, with fast response (< 20 s) requiring only low voltages (< 5 V) to achieve uniform temperatures of ~ 100 °C across large areas. Similar was the performance of the transparent heater on curved glass surfaces. Spray coating in the context of crack template is a powerful method for producing transparent heaters over large area. AgCP1 with invisible wire network is suited for use in proximity while AgCP2 wire network is ideal for use in ultra-large area displays viewed from a distance. Both exhibited excellent defrosting performance even at cryogenic temperatures.

IIIB.3.1 Introduction

Large area transparent heaters are of utmost importance in applications such as display panels,[1]touch screens,[2] roof top solar panels,[3] camera lenses, windows and mirrors that require visual transmittance in cold and moist environmental conditions.[4] Transparent heaters are inevitable where anti-fogging[5] and de-icing[6] is required for the operational stability of the devices. Indium tin oxide (ITO) has long served as an ideal material for transparent heaters since it has high transmittance of ~ 90%, low sheet resistance of ~10 Ω/sq along with good environmental stability.[7,8] Due to the brittleness associated with ITO, its practical use in flexible devices is challenging.[9] Moreover, its current carrying ability and thermal stability are also limited.[8] With such drawbacks associated with ITO, new materials such as graphene films,[1,10,11] carbon nanotube network films,[12-14] Ag nanowire networks and grids[15-18] have been developed which can be potential candidates for ITO replacement. Indeed, many ITO-free devices have been reported in recent years based on the new materials, though mainly in the context of transparent conductors. Only in few cases, successful fabrication of transparent heaters has been realized.[4,19-23]

Low sheet resistance and high transmittance do not guarantee that a given electrode can be used for transparent heater application. The uniformity of sheet resistance is essential for homogeneous temperature distribution over large areas.[21] Small surface defects such as pinholes, scratches and dirt causes non-uniformity in the coating leading to locally high resistance[24] which can become hotspots and result in failure of the heater. The Ag nanowire networks usually suffer from high resistance at crossbar junctions which during joule heating, tend to behave as hot spots leading to local melting.[25] Kim et. al showed that the stability of the Ag nanowire network based transparent heater can be improved noticeably by avoiding the

formation of nanowire aggregates in the network during fabrication.[23] By comparison, transparent graphene conductors seem to do better,[4] though they exhibit relatively high sheet resistance requiring high operating voltages. Thus, low sheet resistance and excellent uniformity over large area are important criteria for a transparent heater. What one desires is a simple and inexpensive method of producing metal wire network based conductors, uniform over large area with minimal contact and junction resistances.

IIIB.3.2 Scope of the present investigation

In earlier sections, spin coating, drop coating and rod coating techniques for producing crackle have been employed for fabricating TCEs. This study explores the possibility of making a crackle template using spray deposition, especially on curved surfaces where common methods such as spin coating may be inconceivable and drop coating may not work well. Spray deposition technique is an attractive tool as it is one of the most suitable and efficient techniques for low-cost industrial-scale processes.[26] It is already well established for industrial use and in-line deposition processes. Several TCEs have been fabricated by direct spray coating of Ag nanowires,[27, 28] PEDOT:PSS[29] and graphene oxide dispersion[31] over large areas. Most of these TCEs are however, limited to flat surfaces.[27-31] The biggest advantage of using spray coating over other techniques is ensuring uniform coating on complex 3D curvilinear objects with varying topography.[32] However, there has been little effort in the literature of using spray technique for the fabrication of TCE directly on curved surfaces.[33] Puetz et al. showed the fabrication of transparent oxide electrode by spray coating of antimony doped tin oxide sol–gel (ATO) on glass tube.[33] In this work efforts have been made to fabricate metal network based transparent conducting electrodes directly on curved objects by beginning with spray coating of a crackle precursor. The spray coating was tried even on flat surfaces such as glass and PET sheets

over large areas. The metal wire networks are tested for joule heating and defrosting near cryogenic temperatures.

IIIB.3.3 Experimental Section

The crackle precursors (CPs) were chosen for the purpose such that the crack width could be obtained in a large range. A commercially available crackle nail polish (CP1) consisting of acrylic resin colloidal dispersion (Ming Ni Cosmetics Co., Guangzhou, China) and crackle paint (CP2) consisting of colloidal SiO_2 nanoparticles purchased from Premium Coatings & Chemicals (India) were the two cracking precursors for spray coating. CP1 was diluted to 0.2 - 0.6 g/mL with the diluter (Ming Ni Cosmetics Co., Guangzhou, China) while CP2 was added with the commercially available diluter and ethyl acetate in 3:1 volume ratio resulting in a concentration of 0.2 g/mL. The crackle precursors were spray deposited using a 135A Airbrush (United Traders, Bangalore) with 0.2 mm nozzle held at a fixed distance of ~ 3 cm above the surface at a nitrogen pressure of ~ 10 PSI. The spray coating was done under constant ambient conditions (25 °C and RH of 45%). Ag metal deposition was carried out on curved objects uniformly inside a physical vapor deposition system (Hindvac, India). A 55 V AC bias was applied to a tungsten basket containing ~ 150 mg of Ag ingot at a base pressure of 10^{-6} Torr to vacuum evaporate Ag metal. The substrates were held at a distance using a custom designed automated rotating holder (2 rotations per second). The deposition is done for 10 min to result in a film thickness of ~ 80 nm. In-situ thermal images of the TCEs while applying voltage was captured using a thermal imager (Testo 885-2, USA) with 640×480 pixels, thermal sensitivity of 0.03 °C, 30° field of view covering long wavelength infrared spectral range of 8-14 µm. The imager also provides relative surface humidity maps based on the ambient temperature, humidity and surface temperature values. The thermal images were acquired from the back side of the electrodes.

IIIB.3.4 Results and discussion:

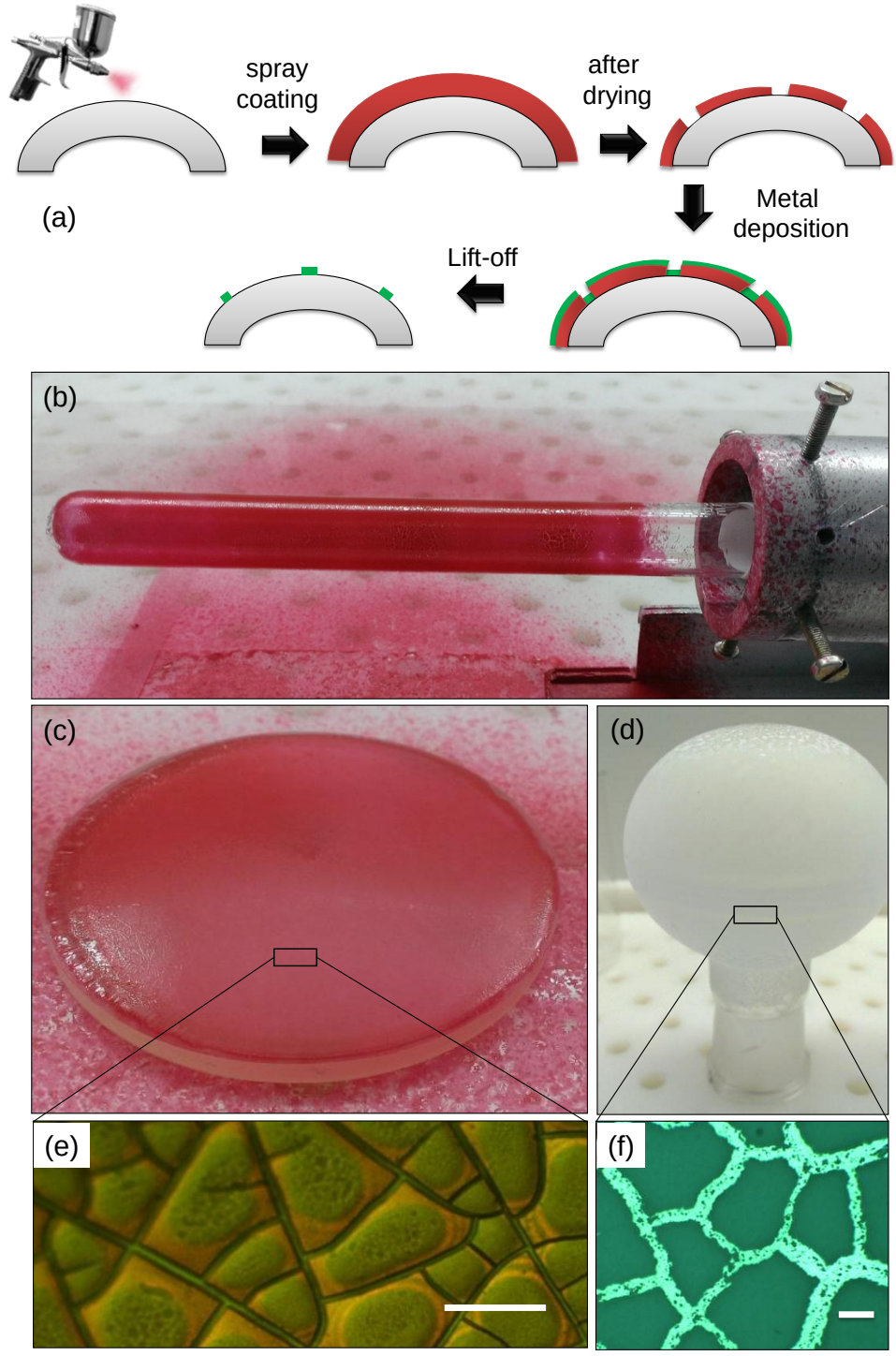

Figure IIIB.3.1 (a) Schematic illustration of the fabrication of crack template on curved surface by spray coating and metal network fabrication. Photograph demonstrating spray coating of crackle precursor CP1 on (b) glass tube and (c) convex lens while CP2 on (d) round bottom flask. Optical microscope images of crack template formed on (e) lens surface (scale bar, 50 µm) and (f) flask surface (scale bar, 100 µm).

In the spray deposition process, there are many controllable variables such as solvent, solution viscosity, spray pressure, the spray distance from sample, spray time and number of spray coats and all can influence the coating.[34] The ink formulation and the solvent properties such as vapor pressure, nozzle flow rate, viscosity and surface tension, also play an important role in deciding the overall quality of coating.[35] The crackle precursors were diluted suitably (see experimental section IIIB.3.3) such that clogging of airbrush is avoided. The fabrication of crack template on curved surface is schematically shown in Figure IIIB.3.1a. The curved objects were coated with crackle precursor, CP1 using custom designed spray coating set up as shown in Figure IIIB.3.1b mounted on a holder. The tube is uniformly coated with cracks all around its diameter. Similarly, a curved convex lens coated with CP1 at a single spray pass and air pressure of 10 PSI, is shown in Figure IIIB.3.1c. The self-drying of the spray coated film in ambient condition resulted in a crack network as shown in Figure IIIB.3.1d. Similarly, CP2 was also coated on curved objects such as a round bottom flask (Figure IIIB.3.1d) where an (CP1) was drop coated on 2.5 cm^2 area glass substrate placed inside a weighing balance. As solvent evaporated, the mass of the crackle precursor layer gradually decreased. The mass change was

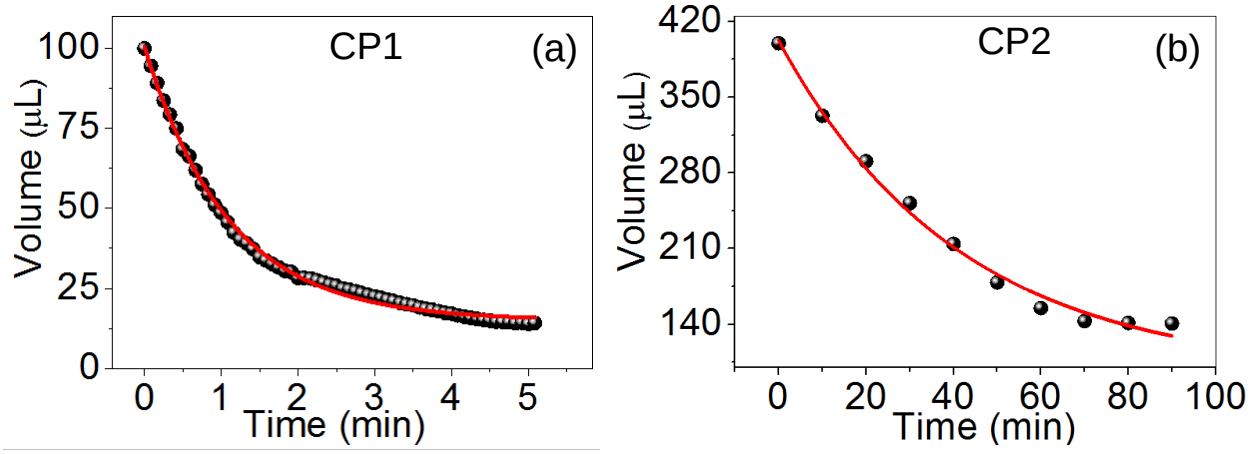

Figure IIIB.3.2 Change in the volume of the crackle precursor during drying, (a) CP1 and (b) CP2. Solid circles are the experimental data and red lines are the exponential fits.

converted into interconnected crack network formed upon slow drying as shown in Figure IIIB.3.1e. It may be noted that CP2 precursor took longer time for complete drying compared to CP1 that dried off quickly and the cracks in CP1 are much finer in contrast to those from CP2. In order to examine the volume change during drying of the colloidal dispersions, a 100 µL the crackle precursor volume change using the known density of the solvent (0.92 g/mL) and the initial volume. As shown in Figure IIIB.3.2a, the decrease in the volume of the crackle precursor is exponential with a decay constant of ~ 1 min. After ~ 5 min, CP1 dried completely and the final volume was 14.15 µL. In similar way, complete drying of CP2 took place in 90 min with an exponential decay constant of 41 min (see Figure IIIB.3.2b).

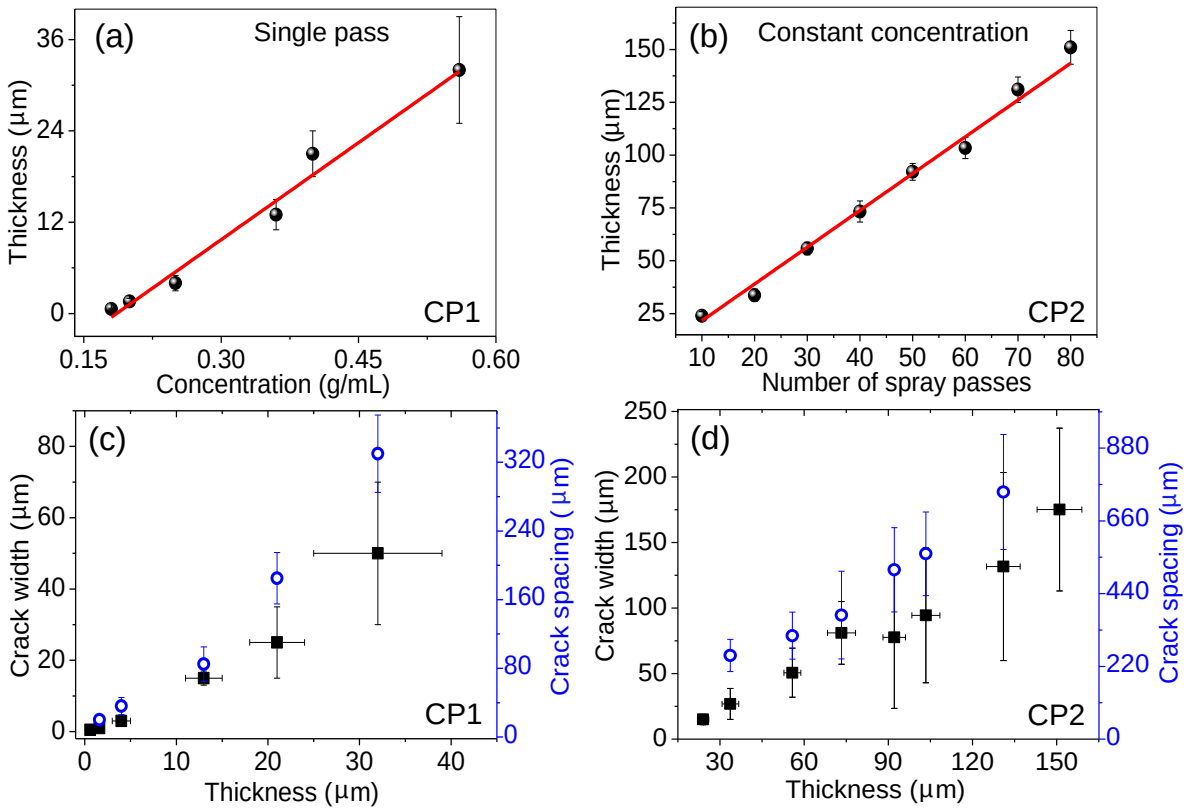

Figure IIIB.3.3 Thickness variation in dried crack layer obtained by spray coating for (a) different concentrations of CP1 in a single spray pass and (b) varying number of spray passes for a fixed concentration (0.2 g/mL) in case of CP2. Variations in crackle features with respect to crack thickness for (c) CP1 and (d) CP2.

After having realized the possibility of obtaining crack networks on curved objects by spray coating, the optimization of crackle template formation was carried out on flat PET substrate, by tuning the solution concentration and number of spray passes for CP1 and CP2 crackle precursors respectively. As CP1 is fast evaporating, single pass spray coating was chosen and achieved the desired thickness by varying its concentration (0.2 - 0.6 g/mL), however, without causing any clogging of the airbrush. The thickness of the dried film varied linearly between 0.5 – 30 μm for the range of dilution employed (see Figure IIIB.3.3a). The CP2 crackle precursor is relatively viscous even at low concentrations and thus required several spray passes for building up the layer beyond the critical thickness. Nearly 10 passes of spray over the same region resulted in a thickness of ~24±2 μm but it did not crack properly. The number of spray passes was increased gradually to 80 resulting in a dried crack template thickness of 150±5 μm (Figure IIIB.3.3b). From Figure IIIB.3.3a and 3b, it is clear that spray coating method of forming the crack template provides a good control over the layer thickness. However, the latter is not easily applicable to curved surfaces. The drop coating technique could be adapted to curved surfaces, but uniformity in coating over large area cannot assured (as discussed in Part-IIA).

For both crackle precursors, there is a critical thickness below which cracking does not occur. The threshold thickness of CP1 was found to be ~ 800 nm while for CP2, ~ 30 μm. The difference in the critical thickness for cracking depends on the nature of crackle dispersion, particle type, size, solvent etc.[36] Since the nature of cracking is different for the two precursors, provided a wider range of crack patterns, which is advantageous in different contexts (*vide infra*). The CP1 precursor contains soft acrylic particles (~ 50 nm) that may partially release the stress developed during drying by deforming, while the remaining stress is being released via crack formation as discussed in Part-IIA. Thus, CP1 results in the formation of much

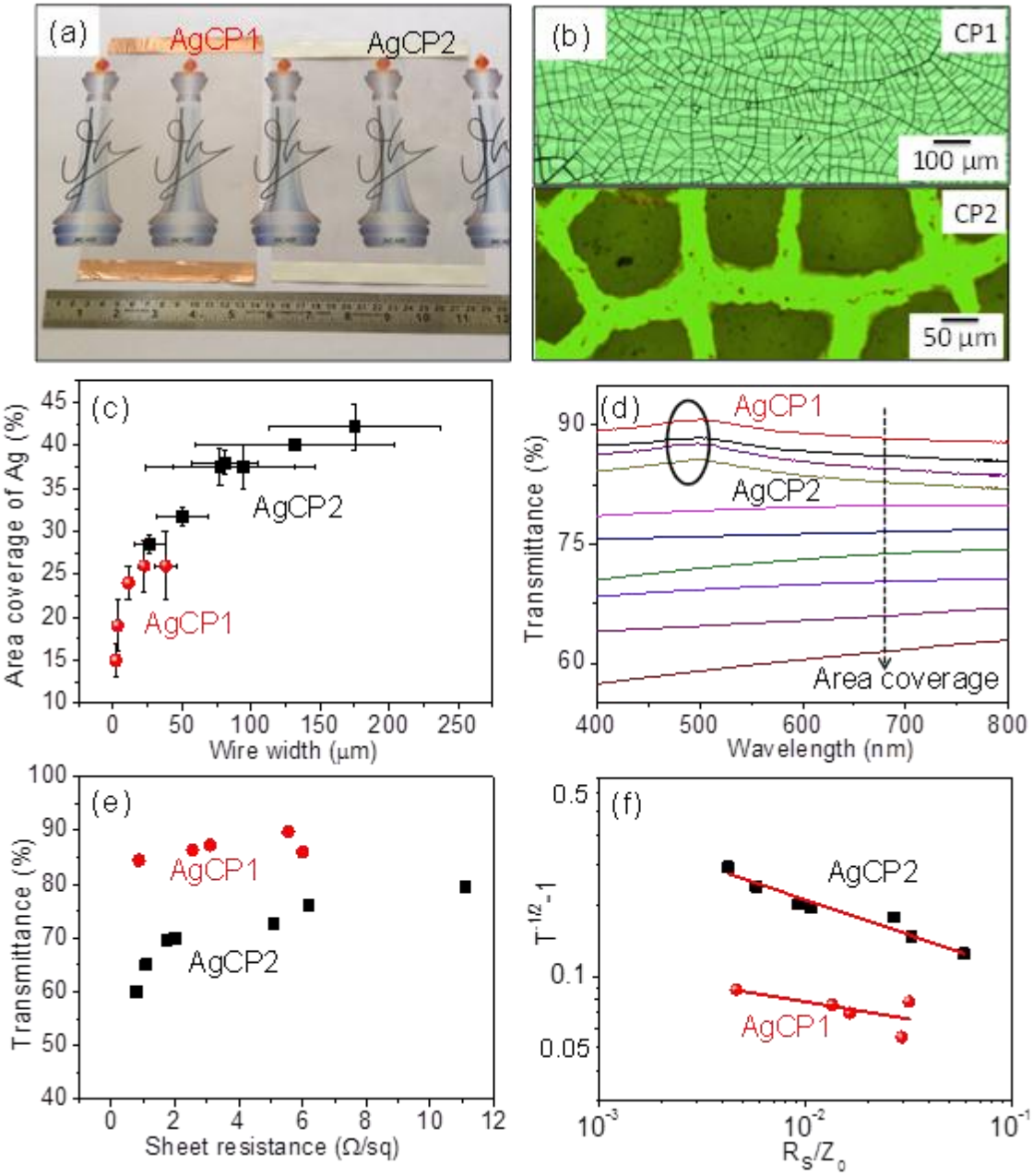

Figure IIIB.3.4 (a) Photograph of TCEs with Ag wire networks, AgCP1 and AgCP2. (b) Optical micrographs of the Ag wire networks, (c) Area coverage of Ag wire networks for various wire widths obtained in AgCP1 and AgCP2. (d) Transmittance spectra and (e) transmittance versus sheet resistance for AgCP1 and AgCP2 respectively. (f) $T^{-1/2}$-1 versus R_s/Z_0 plot for the data in e. Here, the red circles represent AgCP1 and the black squares, AgCP2.

finer cracks ranging between 2 - 40 µm (see Figure IIIB.3.3c) with low layer thicknesses. As CP2 precursor consists of hard silica particles (< 20 nm), particle deformation in this case may be negligible and therefore, all the stress developed in the layer during drying is released only via

crack formation. Thus much wider cracks (30 -250 μm) get formed at higher film thicknesses as seen in Figure IIIB.3.3d. For both the precursors CP1 and CP2, the crack width and spacing bears a direct relation with the thickness of the crack template, which is well known in crack physics.[37]

The crack templates were deposited with Ag metal of ~ 80 nm thickness and the templates were then removed by lift-off. The Ag wire networks formed using CP1 and CP2 templates are termed as AgCP1 and AgCP2, respectively. The photographs of AgCP1 (12 × 18 cm^2) and AgCP2 (14 × 18 cm^2) patterned PET are shown in Figure IIIB.3.4a. The optical micrographs reveal the connectivity of Ag wire network for AgCP1 and AgCP2 (see Figure IIIB.3.4b). The metal fill factors (percentage metal area coverage) in Figure IIIB.3.4b are 24% and 42%, respectively for AgCP1 and AgCP2 which varied with respect to the wire width. As seen in Figure IIIB.3.4c, the fill factor of AgCP1 is less (15 to 25%) compared to that of AgCP2 (28 to 42%), as wires are narrower in the former case. A low metal coverage is important in electrodes requiring high transmittance while high metal coverage ensures good conductivity across the electrode. Thus, the spray coated templates developed in this study not only provide a choice of wire widths in a broad range (2-250 μm), but also enable TCE fabrication over large areas. The transmittance spectra have been measured in specular mode for both types of Ag electrodes (Figure IIIB.3.4d). The AgCP1 electrodes exhibit high transmittance up to 88%. The diffuse transmittance including the contribution of scattered light was found to be more than the specular transmittance resulting in haze of ~5%. The transmission at 550 nm for Ag electrodes with different area coverage is plotted as a function of sheet resistance in Figure IIIB.3.4e. The sheet resistance values are quite low (< 11 Ω/sq) for all the electrodes, while the transmittance was above 80% for AgCP1 and around 60-78% for AgCP2 electrodes. The low sheet resistance

is a result of seamless wire junctions, which have been discussed in detail in Part-IIA. A TCE is quantitatively accessed usually by the figure of merit (FoM). There are several ways of defining FoM,[24] the most popular one is σ_{OP}/σ_{DC} (ratio of DC and optical conductivities) that relate T with R_s for conducting thin films using the equation (1):

Table IIIB.3.1: A brief literature comparison of FoM values for metal networks/meshes.

Material	Sheet resistance (ohm/sq)	Transmittance (%)	Figure of merit (FoM)	Reference
Ag network	4.2	82	300 to 700	38
Ag nanowires	100	92	500	15
Ag network	6.4	82	282	39
Cu nanowires	51	93	100	40
	7.7	68.4	117	
	1.4	14	80	
Cu nanotrough Au nanotrough Ag nanotrough	2 8 10	90 90 90	1742 436 348	41
Ag nanowires	6.5	91	160	42
AgCP1	0.9	84	2445	Present study
	6	86	401	
AgCP2	0.8	60	809	
	2	70	482	

$$T = \left[1 + \left(\frac{z_o.\sigma_{OP}}{2R_S.\sigma_{DC}}\right)\right]^{-2} \qquad (1)$$

The σ_{OP}/σ_{DC} values fall in the range of 400 to 2445 for AgCP1 and 482 to 809 in the case of AgCP2. The values obtained here are commendable and probably the highest reported in the literature (see Table IIIB.3.1). Recently, Han et al. claimed high values of σ_{OP}/σ_{DC} in the range of 300-700 for Ag wire networks.[38] With the present metal networks has much higher values probably due to lower metal fill factor and lesser haze (~5%). In order to understand the conduction behavior of these networks, the following equation (2) given by Sorel *et al*.[43] was used to fit the data in Figure IIIB.3.4e.

$$T = \left[1 + \frac{1}{\Pi}\left(\frac{z_o}{R_S}\right)^{1/(n+1)}\right]^{-2} \qquad (2)$$

where Π is percolative figure of merit and *n*, percolative exponent. From the fits in Figure IIIB.3.4f, the fitting parameters for AgCP1 are Π = 25.6, *n* = 5.8 and for AgCP2, Π = 18.4 and *n* = 2.3. These values stand above the threshold requirement of industry standards.[44]

The exceptional optoelectronic properties of the spray produced electrodes have been further explored by fabricating transparent heaters, initially on PET before embarking on rigid curved surfaces. The electrodes were initially examined for stability against atmospheric oxidation by externally heating at different temperatures as well as by monitoring the change in resistance at a given temperature and confirmed the thermal stability. The electrodes were then joule heated by applying DC bias. A typical thermal image obtained for the AgCP2 network over 4 × 2 cm^2 area is shown in Figure IIIB.3.5a. The area marked in the photograph has a mean temperature of

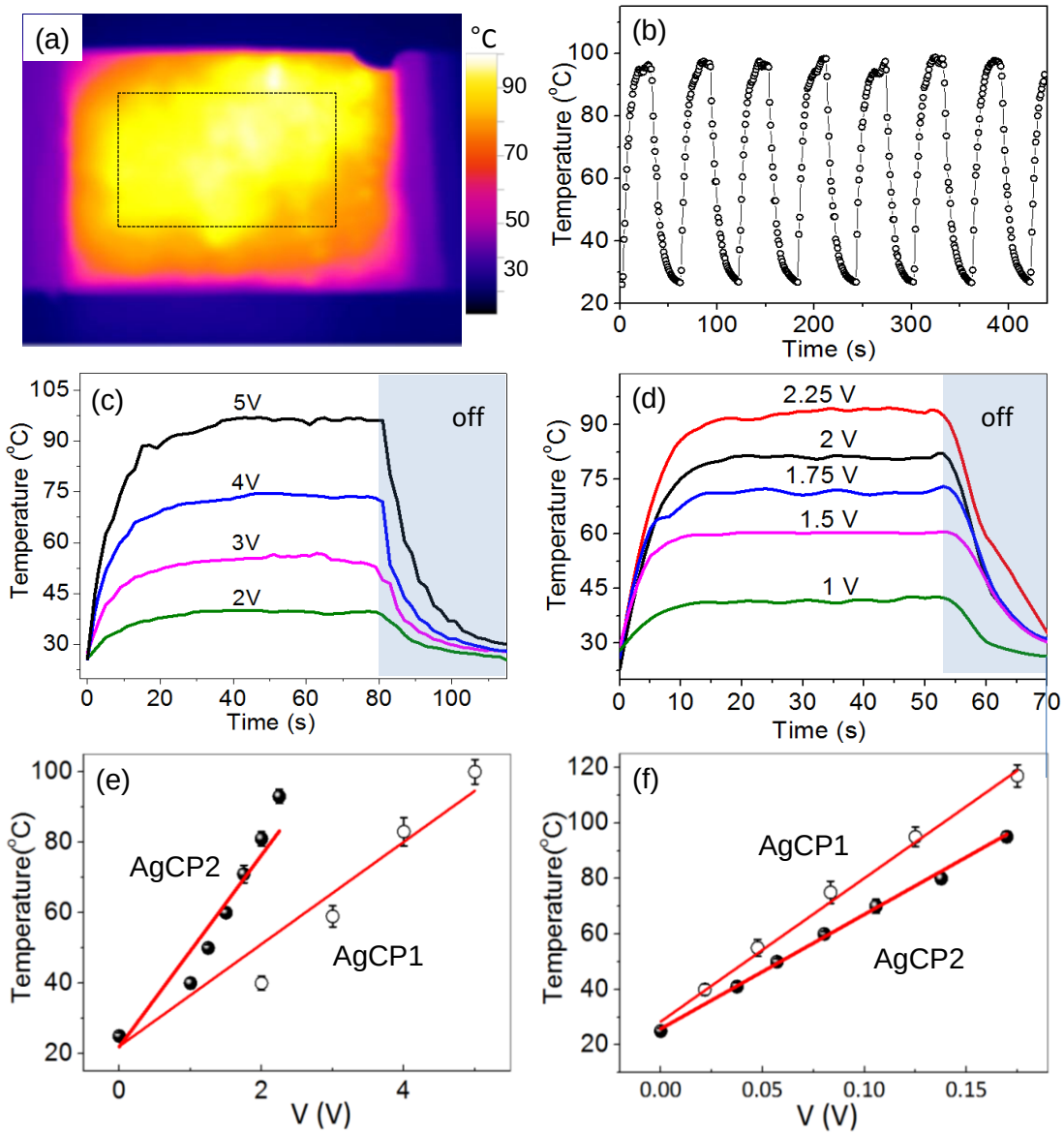

Figure IIIB.3.5 (a) Thermal image of AgCP2 based heater. The temperature distribution in the marked region is uniform. (b) Heating cycles at an operating voltage of 2.25 V. Temperature rise curves at different applied voltages as a function of time for (c) AgCP1 and (d) AgCP2. Maximum temperature attained as a function of (e) applied voltage (f) input power for both type of electrodes.

93.4±3.2 °C. The uniform temperature distribution clearly indicates high quality of these electrodes. A voltage of 2.25 V was applied to raise the temperature to 95 °C and after 30 s, it was reduced to zero and this was repeated for several cycles. Accordingly, the temperature switched between the ambient (27 °C) and 95 °C as shown in Figure IIIB.3.5b. The temperature rise and fall curve were obtained at different voltages for AgCP1 and AgCP2 (Figure IIIB.3.5c

and 5d). Since the resistance of AgCP2 is lesser because of the higher metal area coverage, the temperature up to 100 °C could be attained at much lower voltages (below 3 V) compared to AgCP1. The temperature is found to be quite stable under an applied voltage and falls down immediately as soon as the voltage is reduced to zero. The response time is very low (20 and 15 s respectively for AgCP1 and AgCP2) as compared to the literature results (see Table IIIB.3.2), which may be attributed to less scattering as the wire junctions are seamless. The power dissipated in the network, given by V^2/R, indicates that the power is inversely related to resistance at a constant voltage. Since the resistance of AgCP2 is lower than AgCP1, higher temperatures are attained at a much lower voltage as seen from Figure IIIB.3.5e. For large area heating application, AgCP2 is preferred as the network parameters- wire width and cell size, are much bigger than those in AgCP1 electrode. This in turn reflects in the low input voltage ($\Delta T/\Delta V$) requirement. The response is also slightly better in the former (see Table IIIB.3.3). For smaller areas that require complete visible transparency, AgCP1 is better even though it requires somewhat higher response time and voltage input; it may be noted that these values are however much smaller than those reported in the literature (Table IIIB.3.2). The choice of CP1 or CP2 for patterning depends upon the specific application under consideration. The thermal resistance calculated from the slopes of temperature versus power plots[45] (Figure IIIB.3.5f) is found to be 515 °C.cm^2/W and 409 °C.cm^2/W for AgCP1 and AgCP2 respectively. These values are much higher compared to literature results on Ag nanowire and CNT based TCEs, which is understandable since the present TCEs do not suffer from loss at junctions. Indeed, the values are comparable to that obtained with graphene based transparent heaters (Table IIIB.3.2).

The flexibility of transparent heater was tested by bending it at different curvatures (see Figure IIIB.3.6). The IR images in Figure IIIB.3.6 reveal the uniform temperature distribution even in

the bent position. Thus, flexibility of the transparent heater has been demonstrated without any degradation in the performance.

Table IIIB.3.2: Literature comparison of transparent heaters.

Reference number	Material used	R_s (Ω sq^{-1})	V (V)	T (°C)	Response time (s)	Rate (°C/s)	Thermal resistance (°C.cm^2/W)
6	Graphene	43	12	100	75	1.3	409
4	Graphene	66	12	100	300	3	660
46	Graphene	641	60	180	120	1.5	163
47	MWNT	172	40	140	30	4.6	---
48	MWNT	349	15	75	---	---	---
49	SWNT	139	60	160	---	---	---
45	SWNT	2600	60	47	60	0.78	140
50	SWNT	250	60	200	~70	2.8	54
51	Ga doped ZnO	---	42	90	30	3	---
52	Ga doped ZnO	---	20	160	50	3.2	---
53	ITO		50	180	25	7.2	---
54	ITO	633	20	160	110	1.4	---
55	Ag NW / SWNTs	---	15	100	30	3.3	---
56	Ag NW	33	7	55	500	0.11	~ 85
23	Ag NW	10	7	100	75	1.3	---
Present study	AgCP1/PET	6	5	95	20	4.7	515
	AgCP2/PET	2	2.25	97	14	7	409

Table IIIB.3.3: Optoelectronic and thermal properties of TCEs derived from crackle precursors, CP1 and CP2.

Pattern type	width (µm)	Cell size (~ µm)	T (%)	R_s (Ω/sq)	Area (cm^2)	Thermal resistance (°C.cm^2/W)	Response time (s)	ΔT/ΔV °C/V
AgCP1	2-5	50	86	6	4 × 3	515	20	18
AgCP2	100 -150	500	70	2	4 × 2	409	14	42

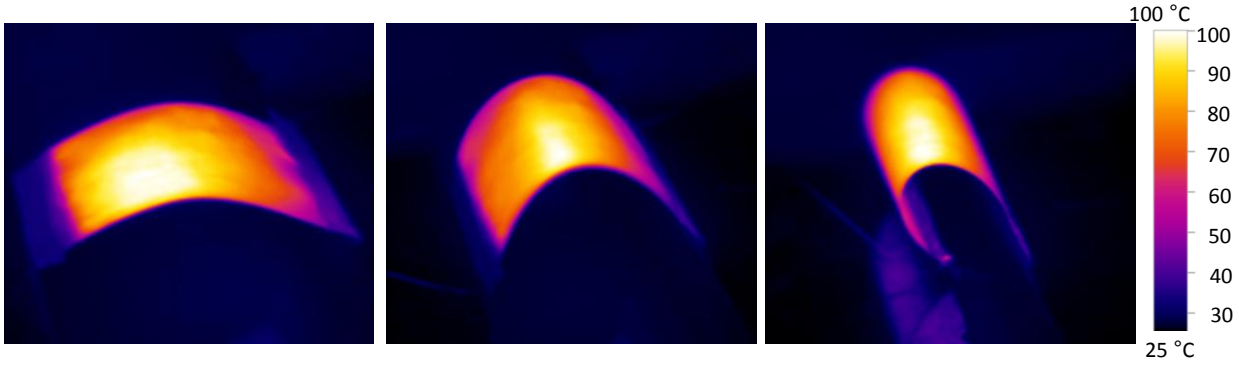

Figure IIIB.3.6 IR images of AgCP1 transparent heater (3.5 × 2.5 cm^2) while it is bent to different curvatures.

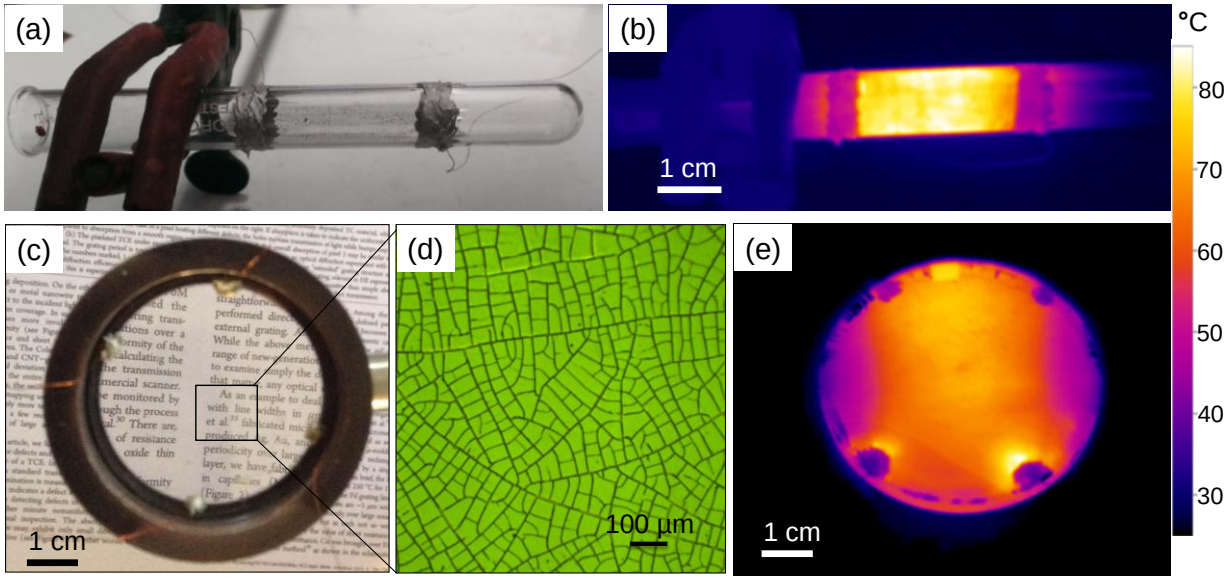

Figure IIIB.3.7 (a) Photograph and (b) thermal image of a glass tube covered with AgCP1 at 8 V. (c) A photograph showing the zoom-in text seen clearly through a AgCP1 derived TCE on convex lens along with its (d) optical micrograph and (e) thermal image taken at 9 V.

The transparent heaters find high practical utility when fabricated on substrates of any curvature. Although ITO coating on curved surfaces is well known,[57] this issue is not well

addressed in the literature, particularly in the context of new generation TCEs. The crackle precursor spray coated directly on curved objects was developed after depositing metal (thickness, ~ 80 nm) with the help of a custom designed set up for rotating the object inside the chamber during deposition (see Figure IIIB.3.1b). Figures IIIB.3.7a and 7c show the AgCP1 metal networks fabricated on a glass tube and a convex lens, respectively. By applying 8 V to

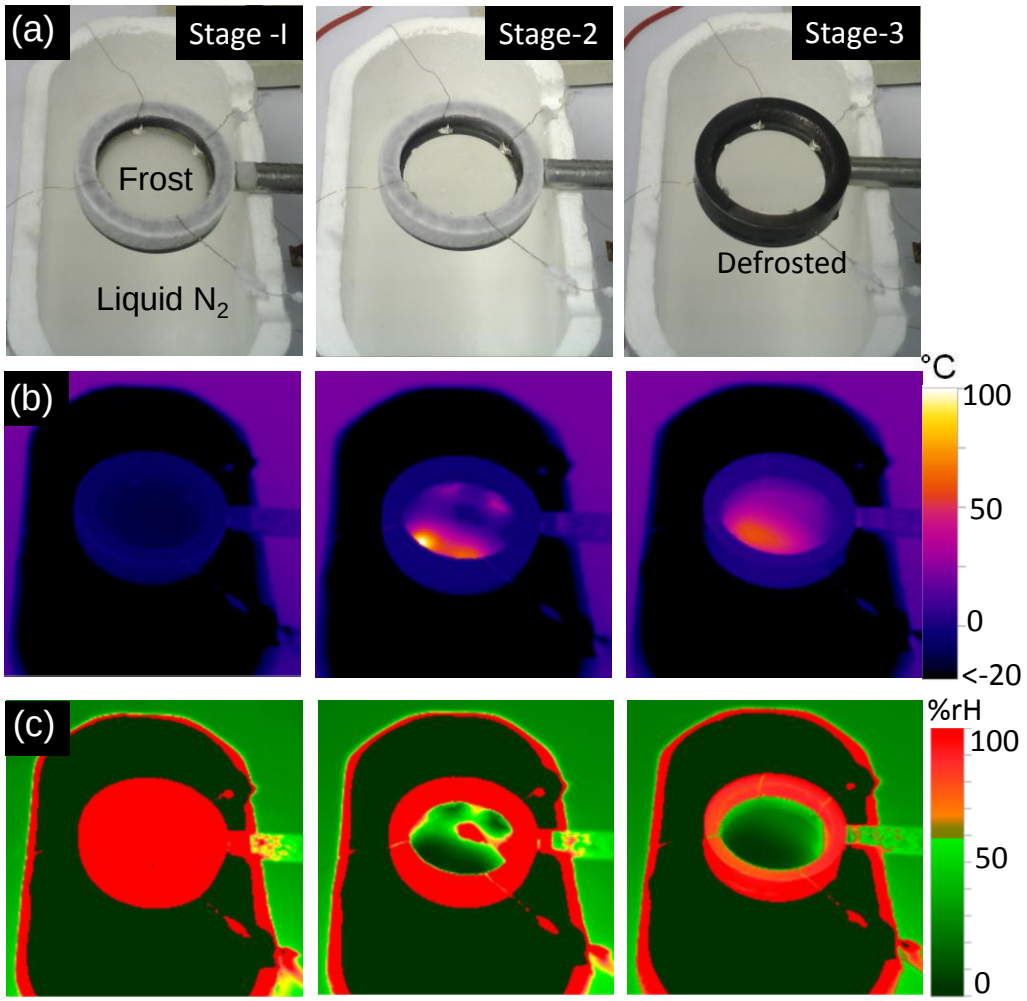

Figure IIIB.3.8 (a) Photographs (b) thermal images and (c) humidity images of the AgCP1 coated lens showing the sequential defrosting stages. Initially in stage 1, frost was made to form by exposing the TCE(lens) to liquid nitrogen vapor which on applying 6 V, got partially removed within few seconds (stage 2) and after 2 min (stage 3), complete removal of frost took place.

ring electrodes, the tube could be made to attain a temperature of ~ 85 °C uniformly all around its curvature (see Figure IIIB.3.7b). Such transparent heaters may find applications in culturing

of cells, bio-monitoring and chemical reactions, where uniform heating is required at a constant temperature. The AgCP1 coated on a convex lens presents another example, where these patterns are invisible to the naked eyes. The text letters below the lens are clearly seen magnified through the lens (Figure IIIB.3.7c) despite the surface being patterned with wire network as seen in the optical microscope image in Figure IIIB.3.7d. The lens was joule heated by taking contacts from the four corners such that the uniform temperature distribution is achieved (see Figure IIIB.3.7e). Thus, spray coating technique is able to produce uniform wire networks on curved objects as well.

The heating performance of the AgCP1 coated lens was utilized for defrosting as shown in Figure IIIB.3.8a. The frost formed by freezing over liquid nitrogen disappeared quickly on applying voltage (6 V) in situ for 2 min as indicated by stages 1, 2 and 3. The thermal images in Figure IIIB.3.8b show the corresponding temperature changes on the defrosted lens surface. The temperature above the liquid nitrogen bath was less than -20°C while the lens surface showed a temperature of 0 °C (stage 1). As the voltage was turned on in stage 2, the temperature started rising as seen more clearly at the contacts. After complete defrosting (stage 3), the temperature reached a value higher than the surrounding as clearly seen in the defrosted image. To examine further, relative surface humidity maps were obtained from the thermal imager as shown in Figure IIIB.3.8c. The ambient humidity was around 48% while above liquid nitrogen bath, it was nearly 0%, as nitrogen filled the local atmosphere. The frosted lens surface appears red with 100% RH (left) due to frost formation, which upon heating, turned to ambient RH due to defrosting (see middle and right images). This shows the capability of transparent heater to work even at sub-zero operating temperatures.

Thus, spray coating of crack template is a viable and efficient route to TCE fabrication particularly on curved surfaces. By the spray coating method, the desired template thickness can be easily achieved even on highly curved surfaces, and it is the thickness alone which ultimately decides the nature of the crack network and in turn the nature of the wire network on the curved TCE. This clearly is the merit of the present method. On the other hand, spray coating of nanowire dispersions to produce TCEs is indeed possible but is limited to flat substrates.[27,28] Else, it is shown that a prefabricated TCE on a flat substrate can be transferred onto a curved object using a polymer support.[41, 58] However, transferability over large area involving complex surfaces can prove difficult. A flexible sheet cannot be laminated perfectly on a curved surface without cuts and folds. Further, lamination on curved objects will not produce a continuous network but rather artificially connected TCE fragments. This may also introduce extra electrical junctions and relatively less transparent regions between the TCE fragments. The transfer substrate (a polymer usually) adds additional thermal mass with poor thermal conductivity. Thus, the power required to heat up the curved surface will be much more due to an additional heat sink. The lamination may require adhesive in between whose optical and thermal properties may interfere with defrosting action and bring down the performance. Such shortcomings are completely avoided in the present method. Where the TCE is directly fabricated on the curved tube surface, for example by ATO coating, the sheet resistance is comparatively higher (R_s of 3-5 kΩ/sq) which may not result in an ideal heater.[32] In this method, the metal wire network is produced directly on the curved surface and is seamless with low sheet resistance. The fabricated transparent heater exhibited high performance in terms of uniformity of heating, operating voltages and stability. The temperature rise and fall take place typically in less than a minute during heating and cooling, which is an important characteristic

for a heater. These features of a transparent heater may not be easily achievable using other materials and methods (see Table IIIB.3.2).

IIIB.3.5 Conclusions

This study developed a method of spray coating of crackle precursor for fabricating crack template on flat and curved surfaces to obtain crackle networks which serve as sacrificial templates for depositing metal wire networks. In essence, crackle lithography is extended to curved surfaces involving spray coating. Two types of crackle precursors, acrylic resin based (CP1) and SiO_2 particles based (CP2), were chosen such that the crack widths spanning from 2 to 250 μm were made with fill factors in the range of, 15-42%, the lower values pertaining to AgCP1 and the higher values to AgCP2. The crack template was obtained on curved objects such as tube, lens, and flask as well as on flat and flexible substrates. The obtained metal wire networks simply mimic the crack networks; those resulting from AgCP1 were invisible even from small viewing distances while those from AgCP2 were unnoticeable only from a distance. Importantly, both showed excellent optoelectronic properties such as low sheet resistance and high transmittance (6 Ω/sq at 86% for AgCP1; 2 Ω/sq at 70% for AgCP2). Using AgCP1 and AgCP2, transparent heaters have been fabricated on flat-flexible PET as well as on curved glass objects resulting in uniform heating all across, irrespective of the substrate type and its curvature. Thus made transparent heaters were high performing includes low response times (< 20 s), low input voltages (< 5 V) and high thermal resistances i.e 515 °C.cm^2/W. Upon application of a nominal voltage of 6 V, a temperature of 60 ºC was achieved on the lens held under sub-zero celsius condition.

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IIIB.4 High temperature transparent heaters

Summary

A transparent conductor which can generate high temperatures finds important applications in optoelectronics. In this study, a wire network made of Au on quartz is shown to serve as an effective high temperature transparent heater. The highly interconnected Au wire network thus formed exhibited transmittance of ~ 87% in a wide spectral range with sheet resistance of 5.4 Ω/sq. By passing current through the network, it could be joule heated to ~ 600 °Cwithin few seconds. The extraordinary thermal performance and stability owe much to the seamless junctions present in the wire network. Further, the wire network gets self-annealed through joule heating as seen from its increased crystallinity. Interestingly, both transmittance and sheet resistance improved following annealing to 92% and 3.2 Ω/sq, respectively.

IIIB.4.1 Introduction

Transparent conducting electrodes (TCEs) are essential components of any optoelectronic device be it a polymer solar cell,[1] dye-sensitized solar cells (DSSC),[2] light emitting diode,[3] touchscreen or a display.[4] The main requirements of a TCE, besides the long-term stability, are high transmittance (~ 90%) in the visible range of wavelengths and low sheet resistance (~ 10 Ω/sq) and both should be uniform over the electrode area. Other useful attributes are the flexibility, ease of processing and importantly, the cost of fabrication. While applications such as touchscreen may compromise with many of the above technical requirements, those involving active semiconductor or electrolyte layer interface, would demand in addition, high thermal stability of the TCE.[2] Often, the as-deposited active layer may lack crystallinity, which needs

annealing at elevated temperature during processing.[5] Such a treatment is also used for enhancing the coupling between the active layer and the electrode.[3] If only a TCE can sustain the desired annealing temperature, which may be several hundred degrees depending on the nature of the active layer, the device performance can be maximized.[6] For example, during the fabrication of DSSC, the TCE (fluorine doped tin oxide, FTO), deposited with TiO_2 layer is typically annealed at ~ 600 °C.[5] CdTe based solar cells not only require high thermal stability but also demand chemical stability of the TCE at elevated temperatures.[7] GaN based light emitting diodes require annealing at elevated temperature (300 to 600 °C) in air to achieve ohmic conduction between TCE and active material, leading to higher performance.[3,6]

Annealing temperatures are usually decided based on the TCE, what it can withstand. Indium tin oxide (ITO) is widely used as TCE due to its excellent optoelectronic properties, albeit the scarcity of In and high cost of fabrication.[8] Its thermal properties are just ordinary; it exhibits a slow thermal response and a poor thermal stability.[9] It degenerates into an oxygen deficient species when heated above 400 °C.[10] FTO, though similarly expensive, is preferred over ITO due to its higher temperature stability.[11] In the recent years, substantial work has been carried out to overcome these issues using nanomaterials. Ag nanowire[9,12,13] or CNT network,[14-16] Ag grids[17] based TCEs has been discussed in Part-IIA section IIA.1. As these are metallic/CNTs and hence conduct high current densities (~ 10^5 A cm^{-2}), instead of joule heating external heating is possible; joule heating is advantageous in that no external heat source would be required and heat need not transmit across the thickness of the substrate, the latter usually is a moderate thermal conductor. Further, external heat may induce other effects such as dewetting of the active layer.[18] Indeed, in the recent past, transparent heaters have attracted much attention particularly in the context of applications such as defogging and defrosting

windows, where TCEs joule heated to around 70-150 °C would suffice.[9,12-16] The issue being addressed in this study refers to a more stringent requirement of being able to anneal active layers at higher temperatures by joule heating the TCE.

IIIB.4.2 Scope of the present investigation

There have been few studies in the literature evaluating the performance of TCEs as joule heated transparent heaters. For instance, Ag nanowire networks have shown high performance flexible transparent heaters.[9,12,13] It is shown that Ag nanowires may get damaged beyond 200 ºC when heated externally in air.[19] With joule heating, maximum temperature achieved was only 100 ºC.[9] The CNT based TCEs,[14,15] although exhibit good performance, suffers from moderate to low sheet resistance values. The sheet resistance value of a SWNT based TCE was seen to increase upon exposing to air, which practically limits its use.[16] Moreover, such nanowire network based TCEs formed by *brute force* contain innumerable crossbar junctions[20, 21] and therefore suffer from inherent junction resistance; the junctions tend to act as hot spots for oxidation increasing the overall resistance. Another promising nanomaterial is graphene; several graphene based TCEs have been reported in the literature in the last few years.[4, 22, 23] Although transmittance can be very high, the sheet resistance values are only moderate.[4] A graphene based transparent heater was made to reach 180 °C by applying 60 V. However, the high sheet resistance and buoyant mass of the graphene are the constraints for joule heating to elevated temperatures.[24]

In short, any workable solution to the fabrication of a high temperature TCE (HT-TCE) should therefore address the above issues and achieve low sheet resistance, high current density and resistance towards oxidation at elevated temperatures in various media. For high thermal stability in air, Au is the best option among metals. However, synthesis of Au nanowires has

been confined to smaller lengths,[25] although there are a few reports in the literature on polycrystalline Au nanowire networks as TCE.[26,27] These networks also suffer from similar issues (junction resistance) as do Ag nanowire networks, in addition to lack of crystallinity.[9] Thus, it is very important to fabricate Au metal network derived high temperature TCE (HT-TCE) with the junction resistance and crystallinity duly addressed. In this study Au wire network fabricated through crackle lithography has been tried as a high temperature transparent heater. It is mainly focused on fabricating TCEs with high thermal stability even at elevated temperatures.

IIIB.4.3 Experimental Section

Au wire network was fabricated on quartz substrate as described in Part-IIA section IIA.3. As fabricated TCEs were well characterised and Ag epoxy contacts were taken with copper wire connections. In-situ thermal images of the TCEs while applying voltage was captured using a thermal imager (Testo 885-2, USA) with 640×480 pixels, thermal sensitivity of 0.03 °C, 30° field of view covering long wavelength infrared spectral range of 8-14 μm. The thermal images were acquired from the back side of the electrodes. The data points for temperature profile were obtained from the clip recorded during the measurement.

IIIB.4.4 Results and discussion

Au wire network with 60 or 220 nm thickness was fabricated through crackle lithography as described in Part-IIA section IIA.3. Figure IIIB.4.1a shows SEM image of the uniformly spread Au wire network (60 nm thick) and the magnified view shows the natural junction of the network (see Figure IIIB.4.1b). EDS maps in Figure IIIB.4.2 reveal the presence of Au on the quartz substrate. The wire width is typically ~ 2 μm (Figure IIIB.4.1b) but in some wire segments, the width is < 500 nm (see Figure IIIB.4.3) implying that this is a micro/nanowire network. Importantly, the junctions in the network are seamless (Figure IIIB.4.1b). This is because these

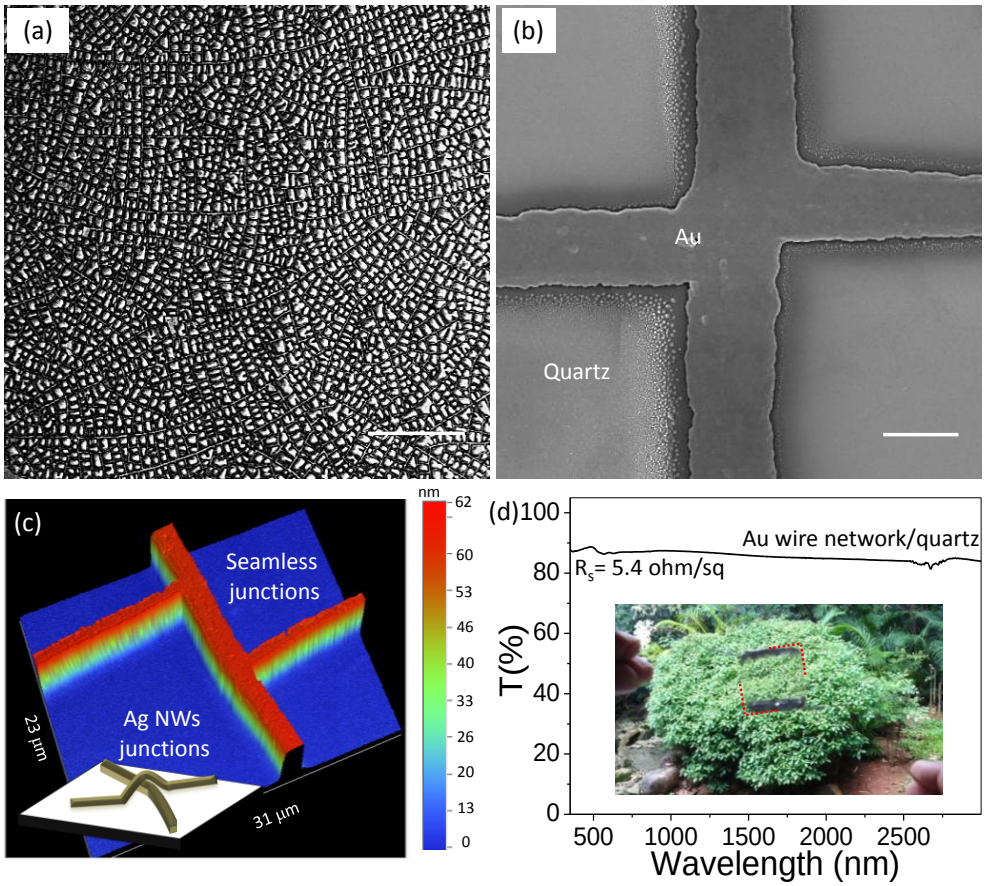

Figure IIIB.4.1 (a) SEM image of Au wire network on a quartz substrate (scale bar 250 µm), (b) High magnification image of the network showing a smooth junction (scale bar 2 µm). Blurring in both images is due to local charging of the substrate under e-beam. (c) Optical profilometry image of the network showing high degree of smoothness of the wire. Schematic of a nanowire crossbar junction representing typical literature example, is shown in the inset to contrast with the seamless junction. (d) Transmittance of Au wire network/quartz (Au thickness = 60 nm) in a wide spectral range. Inset shows a photograph of a Au wire network/quartz TCE, held by stretching the connecting wires. A bush is seen in the background.

junctions are not formed by depositing wires made *a priori* in a solution; rather, they get formed in predefined locations along with the junction regions. Single Au wire network TCE, unlike the Ag nanowire crossbar junctions (see inset of Figure IIIB.4.1c). The substrate being quartz, the TCE can transmit UV, visible as well as IR wavelengths, the average transmittance in the visible range being ~ 87% (Figure IIIB.4.1b). The sheet resistance as measured using a four probe was ~ 5.4 Ω/sq. Another TCE with Au wire thickness of 220 nm has been fabricated with 87%

transmittance and 3.1 Ω/sq sheet resistance. However, this study is focused on Au based transparent heaters to highlight the performance achievable with seamless junctions.

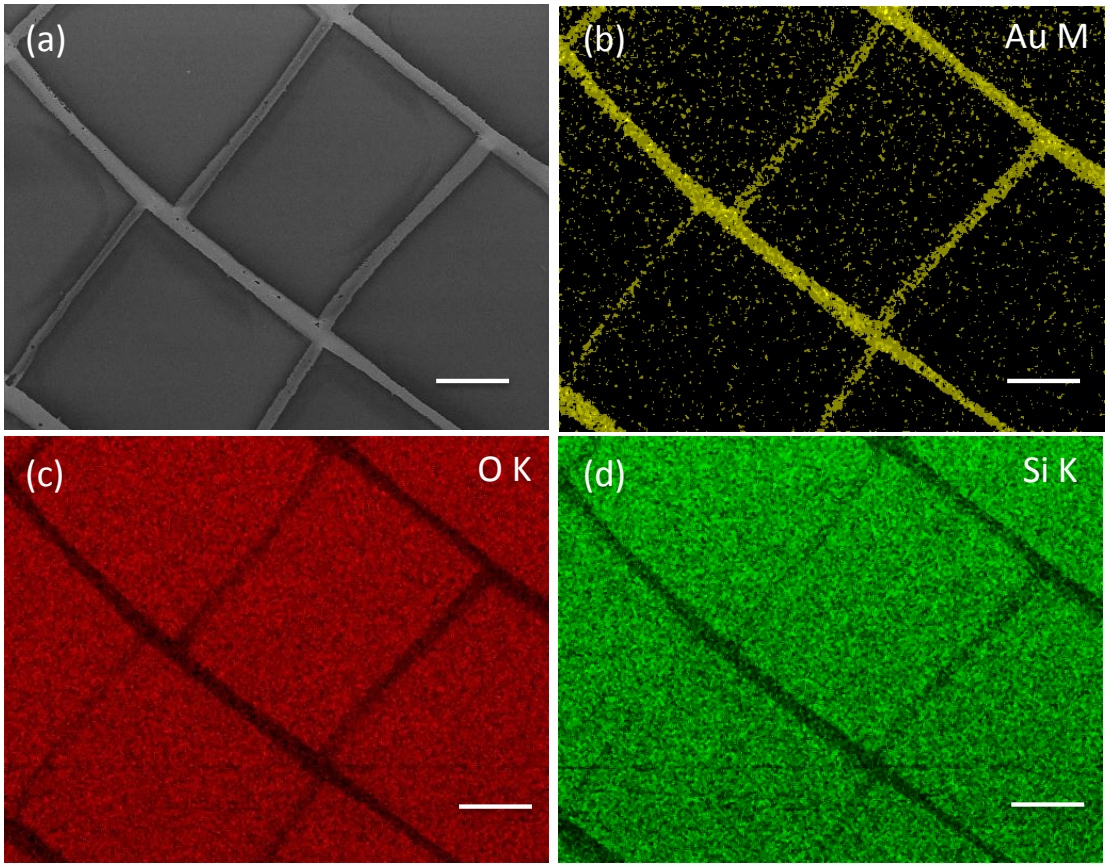

Figure IIIB.4.2 (a) SEM of image of Au network on quartz substrate, EDS maps of the same region corresponding to (b) Au M, (c) O K and (d) Si K, respectively (scale bar 10 μm).

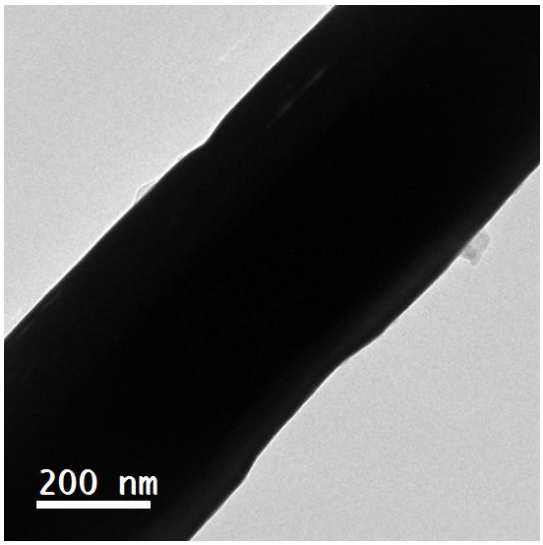

Figure IIIB.4.3 Bright field TEM image of Au nanowire with width ~ 500 nm.

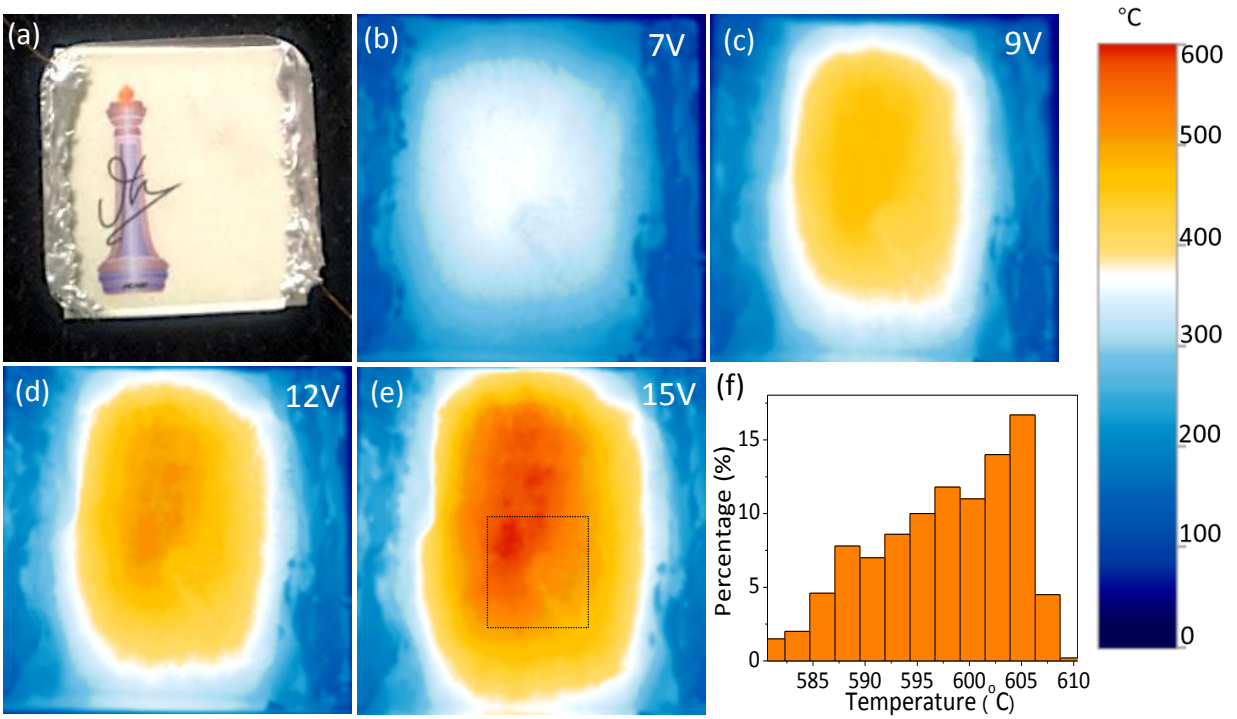

Figure IIIB.4.4 (a) Photograph of a Au wire network/quartz TCE placed over a card on a black background. Its boundary is discernible. The institutional logo on the card is clearly seen through the TCE. For joule heating the TCE, Ag epoxy was used for making contact. Cu wires drawn as contacts for voltage application can be seen in the photograph in a and TCE was held hanging in air (b) to (e) IR images of Au wire network/quartz (Au thickness = 220 nm) at 7, 9, 12 and 15 V, showing temperatures 310, 380, 510 and 600 °C, respectively. (f) Histogram of the temperature distribution in the marked area in e, temperature distribution is within ~ 30 °C.

The Au wire network/quartz TCE was tested for its ability as a resistive transparent heater. One such electrode is shown in Figure IIIB.4.4a with Ag epoxy electrodes laid out on either side. The wire network was joule heated with different applied voltages up to 15 V and at each voltage, IR images were collected. As seen in the IR images in Figure IIIB.4.4b to 4e, the temperature of the substrate increases with the applied voltage, maximum temperature achieved being ~ 600 °C. The histogram in Figure IIIB.4.4f reveals the uniformity of temperature over the TCE; in the marked region of 1 x 1.5 cm^2 (total area, 2.5 x 2.5 cm^2), the temperature is varied in a narrow range of 585 °C to 610 °C. This temperature, outside of the marked region is slightly less due to additional heat loss at the edges.[24] Silver paint contacts also add to extra thermal mass. Clearly, this amounts to a high thermal stability of the TCE made possible by the low sheet

resistance (3.2 Ω/sq) and high current carrying ability (5 $\times 10^5$ A cm^{-2}) of the Au wire network. Interestingly, all the experiment was carried out in the ambient, as Au and quartz both could withstand 600 °C. In vacuum, the TCE should be able to reach even high temperatures. For Ag epoxy, this is almost the limiting temperature, beyond which Ag oxidizes and becomes insulating.

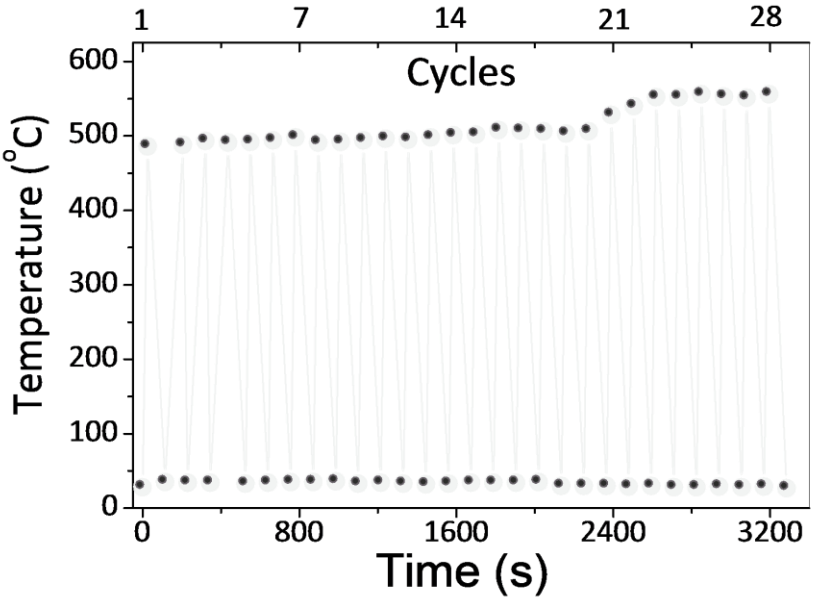

Figure IIIB.4.5 Temperature switching cycles for the HT-TCE with 0 and 12 V applied voltage.

The thermal stability of the transparent heater was further tested by switching the applied voltage from 0 to 12 V for 28 cycles (see Figure IIIB.4.5). As seen from the plot, application of 12 V increased the TCE temperature to around 500 °C in every cycle up to 20 cycles, beyond which the temperature attained was somewhat higher. This may be due to lowering of the sheet resistance caused by joule-annealing of the wire network (*vide infra*). After 29 cycles, it reached the limiting temperature of the device (~ 600 ºC), however the device stopped conducting due to melting and breaking of Au wires (see Figure IIIB.4.6). While performing the temperature switching cycles the resistance of the Au wire network decreased beyond 18 cycles. As a result there is a slight increase in the temperature as seen in IIIB.4.5 with same input voltage (12 V).

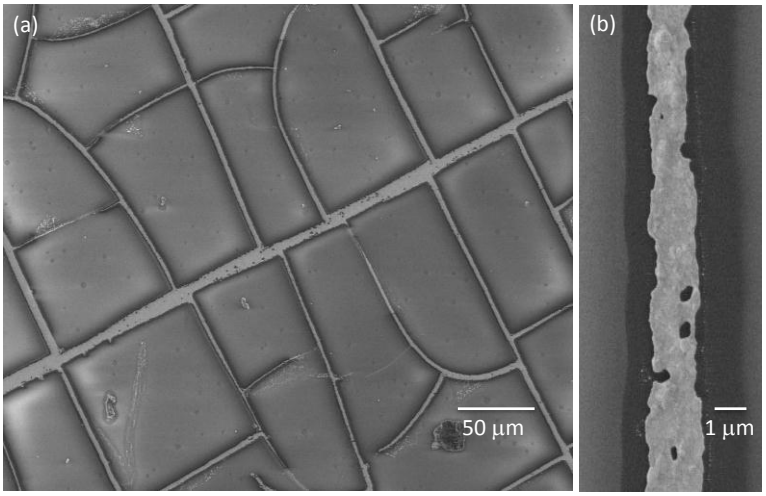

Figure IIIB.4.6 (a) SEM image of damaged Au wire network after self-annealing 650 °C, (b) A magnified view showing pinholes.

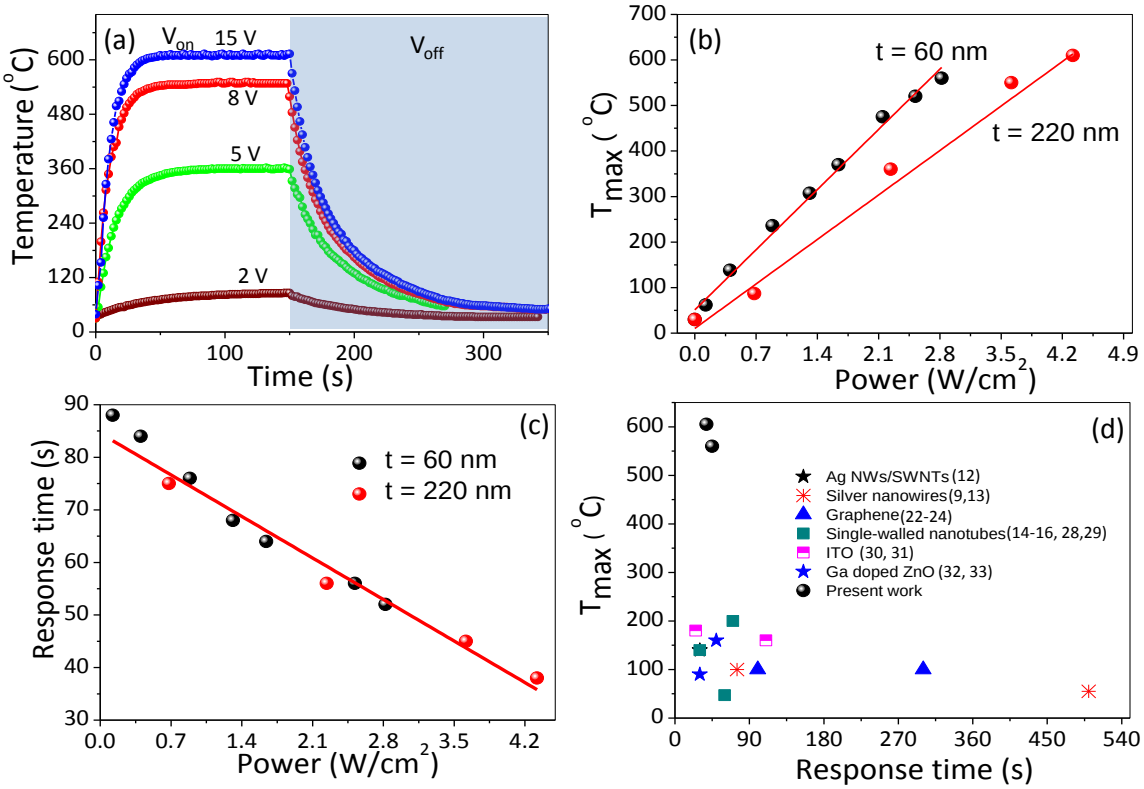

Figure IIIB.4.7 Temperature profiles of Au wire network/quartz as a function of time at different applied voltages recorded using an IR camera. (b) Maximum temperature reached as a function of input power per cm2 area and (c) response time as a function of input power per cm2 area, red lines are linear fits for the experimental data (black and red circles represent 60 and 220 nm thickness of Au wire network). (d) Maximum temperature achieved as a function of the response time compared with the literature examples. The numbers in parenthesis indicate the cited references.

After 28 cycles the device went to a maximum temperature of 600 ºC and small pin holes, broken wires were observed as shown in Figure IIIB.4.6.

The above results deserve some mention in relation to the literature on transparent heaters made with metal NWs, CNT network and graphene. For this purpose, a comprehensive survey of transparent heaters from the literature which is shown in Table IIIB.4.1 along with the present results. As it is clear from the table, the maximum temperature attainable with the transparent heaters reported in the literature is less than 200 ºC, while the present heater could easily reach thrice this value. Such a performance owes much to the high degree of connectivity between the wires with seamless junctions spread uniformly over the substrate.

In order to understand the nature of joule heating in the HT-TCE, the IR image data was carefully analyzed (Figure IIIB.4.7). In Figure IIIB.4.7a are shown the temperature profiles achieved with the 220 nm Au wire network/quartz at different applied voltages. In each case, the temperature reached a plateau maximum in few seconds (response time). As the applied voltage (power) alone decided the ultimate temperature (without any feedback circuit), reaching higher substrate temperatures took lesser time. The maximum temperature was found to vary linearly with the power (see Figure IIIB.4.7b). The slope of the linear fit is defined as thermal resistance i.e. dT/dP, which showcases the performance of the transparent heater.[16] Higher the thermal resistance better is the performance of the transparent heater. The thermal resistances determined from the slopes in Figure IIIB.4.7b are 189 and 139 °C cm^2 W^{-1}, respectively for 60 and 220 nm thickness of the Au wire network. The heat performance of the Au wire network is high as compared to the SWNT network (137 °C cm^2 W^{-1}).[16] The response time of the heater is seen to decrease linearly with increase in the input power for both Au wire thicknesses (see Figure IIIB.4.7c). When a voltage is applied to the device, first the metal network reaches maximum

Table IIIB.4.1: TCEs as transparent heaters. ITO, thin film as well as nanowire/nanotube network based TCEs from the literature compared with Au wire network/quartz from this study

S.No	Material used	Applied Voltage (V)	Maximum temperature achieved (°C)	Response time (s)	R_s (Ω/sq)	Remarks	Ref
1	Ag NW	7	55	500	33	-------	34
2.	Ag NW	7	100	75	10	------	35
3.	Graphene	12	100	75	43	Doped with Au	36
4.	Graphene	12	100	300	66	Dope with Au	37
5.	MWNT	15	75	---	349	High sheet resistance	38
6.	SWNT	60	160	---	139	Thermal heating is required	39
7.	SWNT	60	47	60	2600	High sheet resistance	40
8.	SWNT	60	200	~70	250	T only 30 %	41
9.	ITO	50	180	25		Films are not flexible	42
10	ITO	20	160	110	633	Sintering at 400 °C is required	43
11.	Ga doped ZnO	42	90	30	---	thin films	44
12.	Ga doped ZnO	20	160	50	---	thin films	45
13.	Ag NW/ SWNTs	15	100	30	---	Hybrid structures	12
14.	MWNT	40	140	30	172	5 layers of MWNTs were used	46
15	Graphene	60	180	120	641	Annealing at higher temperatures	47
16.	Au wire network/quartz	23	550	45	5.4 &3.2	Au thickness = 60 nm	Present work
		12	600	40	2.44&3.3	Au thickness = 220 nm	

temperature instantaneously. In this case, the response time is the time taken by the substrate to reach equilibrium temperature. i.e time required to reach an equilibrium temperature in between Au wire network and substrate. As the input power increases the Au wire network reaches higher temperatures, thus requiring lesser time to reach equilibrium temperature i.e lower response time for higher powers. Importantly and uniquely, the TCE presented in this study is capable of Reaching annealing temperatures of over 600 °C within 38 seconds, uncommon among the known TCEs (see Figure IIIB.4.7d and Table IIIB.4.1).[9,12-16,22-24,28-33] Such a fast response owes much to the absence of the conventional junction resistance. In essence, it is a metallic ohmic heater. In contrast, ITO is quite sluggish; in one example, it took 110 s to reach a temperature of 160 °C by joule heating.[31] It has been found to be unstable beyond 350 °C.[11]

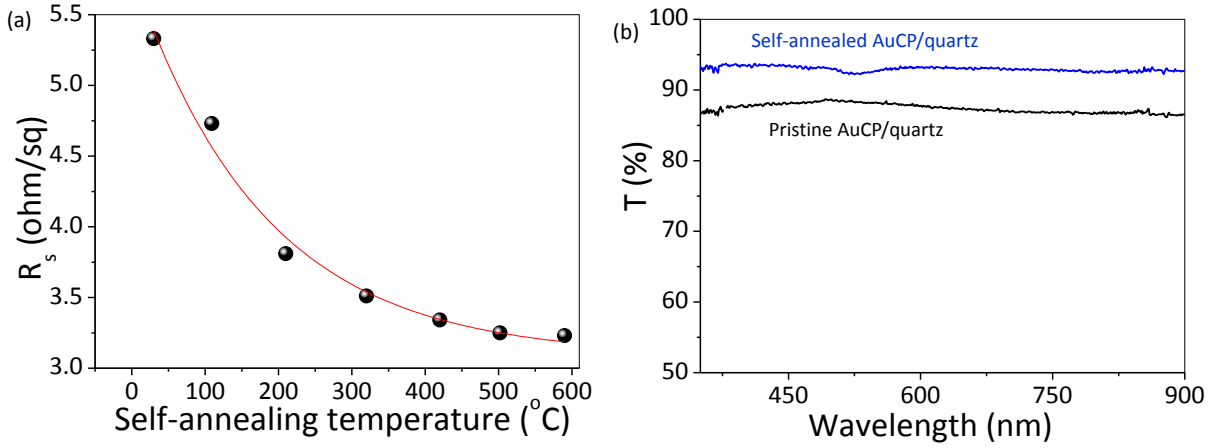

Figure IIIB.4.8 (a) A plot between the sheet resistance of Au wire network TCE and self-annealed for 12 min at each temperature (black circles), fitted with an exponential decay behavior (red curve). (b) Transmittance spectra of pristine and self-annealed (at 600 °C) TCE.

Joule heating has a self-annealing effect on the Au wire network. The sheet resistance of the TCE dropped exponentially from 5.4 to 3.2 Ω/sq (a 40% decrease) following annealing at elevated temperatures (Figure IIIB.4.8a). The inverse of the decay constant in the exponential decay fit indicates the temperature (178 °C) at which the sheet resistance decreased to half of its initial value. The decrease in the resistance is understood by the increased connectivity between

the nanoparticles after annealing.[48] Accordingly, the transmittance of the TCE improved from 87% to 92% (see Figure IIIB.4.8b) following self-annealing at 600 °C (see microscopy results below). The enhanced transmittance with increase is attributed to crystallinity. This situation may be similar to that observed in the case of thin films due to less edge scattering of light.[49] Higher annealing temperature caused local melting, breaking and formation of pinholes

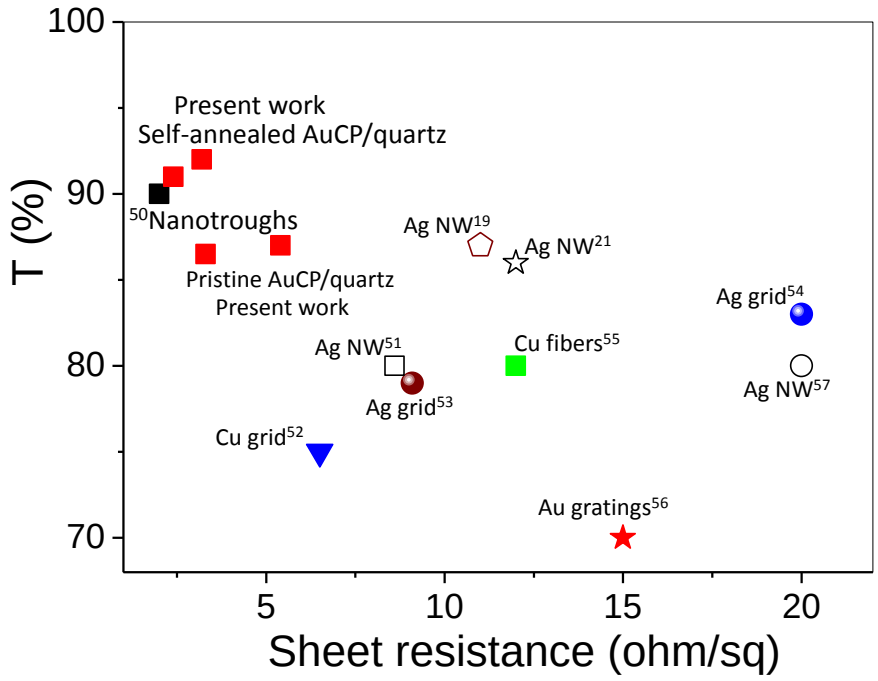

Figure IIIB.4.9 Transmittance versus sheet resistance of TCE compared with the literature (reference numbers indicated), which include TCEs fabricated with seamless contacts and attempts to make seamless contacts.

in the Au wire network (see Figure IIIB.4.6). With higher Au wire thickness employed in this HT-TCE (220 nm) and temperature achieved up to 600 °C. However, a higher wire thickness should be possible, as the crack groove template is typically ~ 1 μm deep. As shown in the Figure IIIB.4.9, the transmittance and sheet resistance values of Au wire network/quartz are compared with other TCEs in literature with seamless junctions[19,21,50-57] and attempts to make seamless junctions from Ag NWs by mechanical pressing and external heating.[19,21]

Moreover, any attempt to decrease the sheet resistance seems to lower the transmittance value, shown by various examples of Ag nanowire networks,[51] CNT networks,[15] graphene[4] and other hybrid structures.[12] In the case of single Au wire network presented here, the transmittance increased while the sheet resistance decreased (see Figure IIIB.4.8a and 8b). Interestingly, in the present case the joule heating favored the both contrasting properties (transmission and sheet resistance).

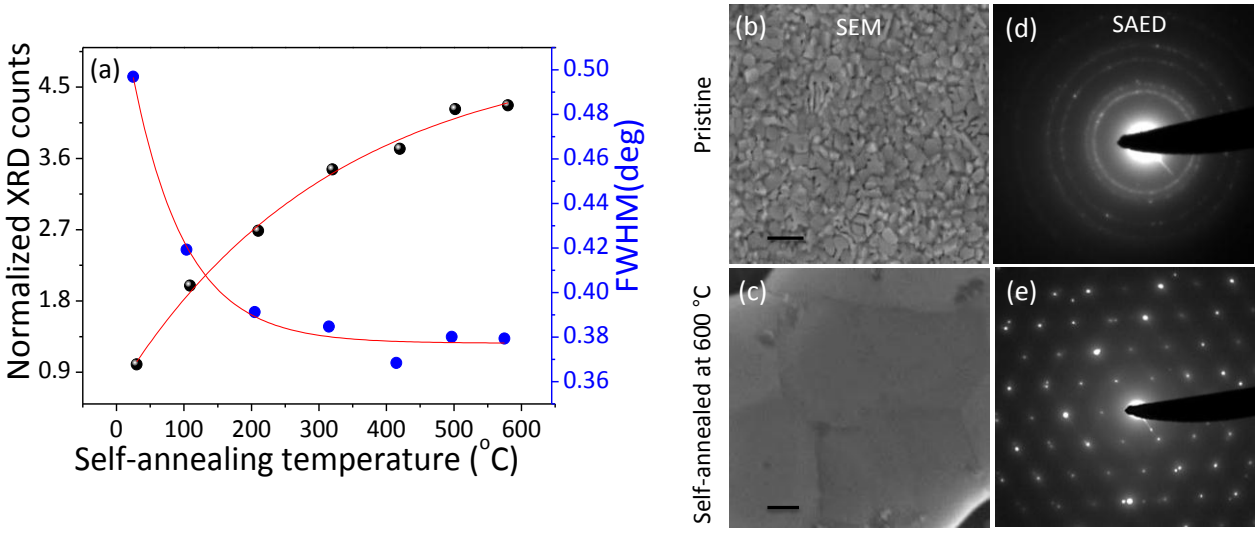

Figure IIIB.4.10 (a)Normalized XRD counts (black circles) and corresponding FWHM (blue circles) of Au wire network/quartz as a function of self-annealed for 12 min at each temperature, fitted with exponential growth and decay curves, respectively (red curves). SEM and SAED images of Au wire network (b), (d) before and (c), (e) after self-annealing at 600 °C (scale bar 200 nm).

In order to gain an insight into the self-annealing behavior, XRD, SEM and SAED measurements were carried out on the HT-TCE before and after joule heating (Figure IIIB.4.10). The (111) diffraction peak of Au grew in intensity and became narrower as the substrate annealing temperature increased. The normalized XRD data in Figure IIIB.4.10a shows that there was a few fold increases in the intensity while the FWHM of the peak decreased by ~ 24%. The nature of these variations is similar to the change in resistance shown in Figure IIIB.4.10a. The decrease in the sheet resistance is nearly linear with respect to the (111) peak intensity, which clearly indicates that the decrease in the sheet resistance owes much to the increased

crystallinity of Au wires. The SEM image in Figure IIIB.4.10b shows granular nature of the as-prepared Au wire, which upon annealing developed much larger and smoother grains (Figure IIIB.4.10c). The electron diffraction pattern from the as-prepared wire consisted of concentric rings typical of polycrystalline nature (Figure IIIB.4.10d), while that from self-annealed wire showed sharp spots (Figure IIIB.4.10e), a signature of the underlying high degree of crystallinity which corroborates the observations made above. An advantage of joule heating over external heating is that the latter is known to produce cracks and dewetting in the TCE.[19] In order to examine the thermal stability, Au wire networks were heated externally on a hot plate at 450 °C for 30 min. As shown in Figure IIIB.4.11 the wire network is broken and lost the interconnectivity, which is clearly prevented in joule heating.

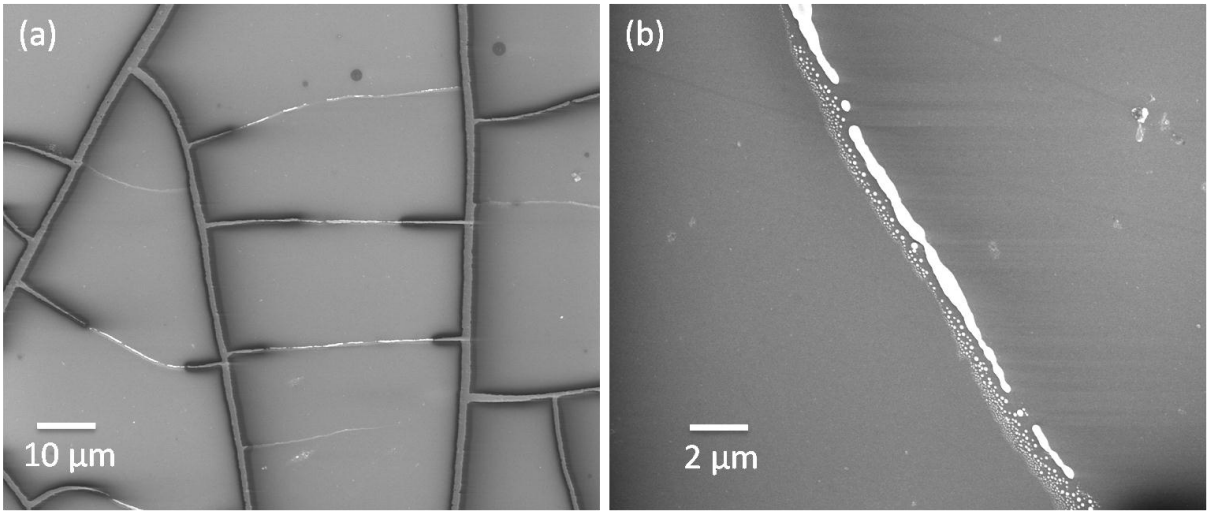

Figure IIIB.4.11 (a) SEM images of externally heated Au wire network (450 °C for 30 minutes), (b) magnified view, demonstrating dewetting.

The HT-TCE proposed in this study therefore finds significance in devices requiring annealing of the active or barrier layers. In order to show the practical usage, the Au wire HT-TCE has been used as joule heater to prepare ZnO film starting with Zn film, just as an example. A Zn thin film (thickness, ~ 60nm) was deposited on the Au wire HT- TCE. By applying a bias of 9 V, the HT-TCE was heated to 450 °C in air when Zn oxidation began. After 45 min, the

substrate was cooled. The XRD pattern (see Figure IIIB.4.12a) clearly demonstrates the formation of ZnO. The EDAX spectrum in Figure IIIB.4.12b) reveals the formation of ZnO on Au wire HT-TCE. The SEM images show (see Figure IIIB.4.12c and 12d) that the Au wires are buried beneath the ZnO thin film. The overall roughness of the Au wire TCE was found to be 60 nm for wire thickness of ~ 220 nm, which decreased to ~ 30 nm after ZnO film formation. The HT-TCE proposed in this study therefore finds significance in devices requiring annealing of the active or barrier layers. Such a step is often quite crucial during the fabrication of optoelectronic devices.

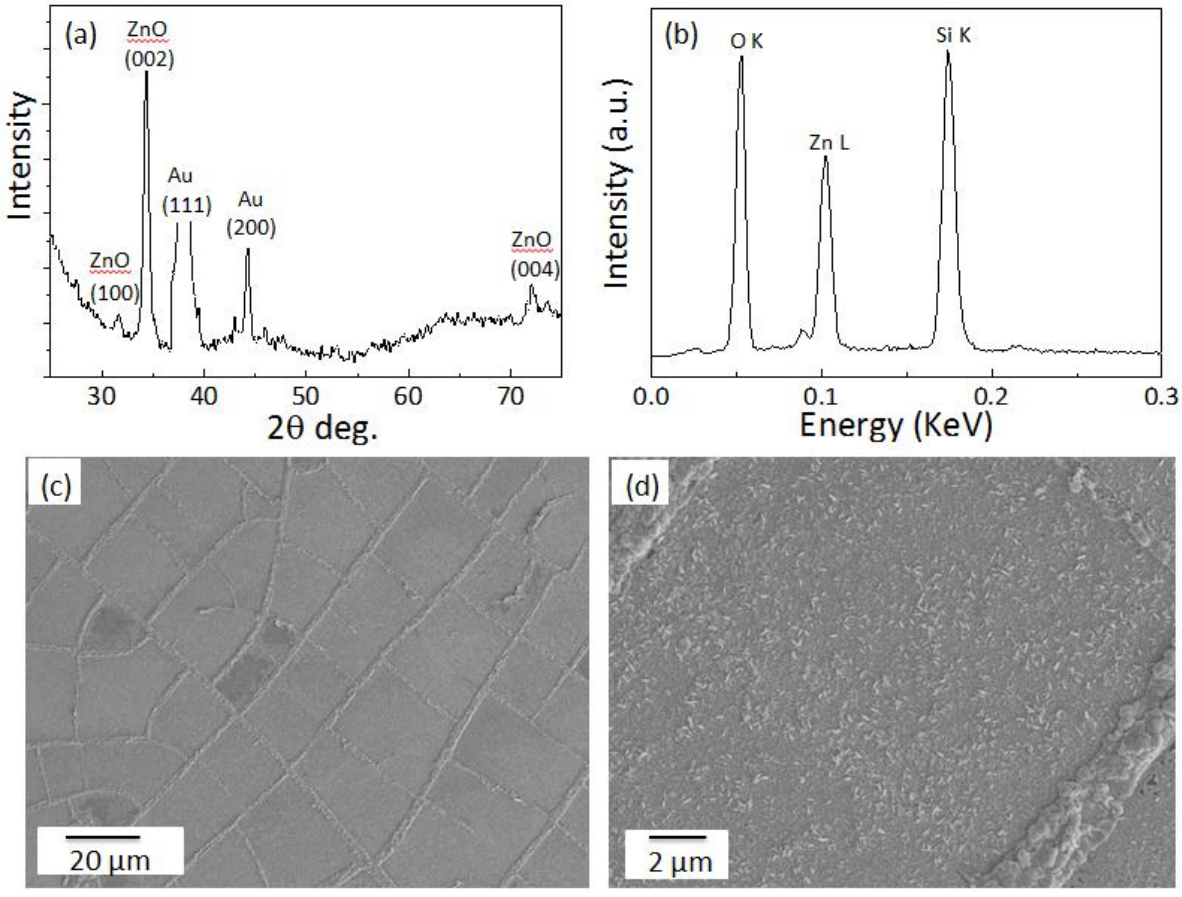

Figure IIIB.4.12 ZnO thin film on Au network (HT-TCE): (a) XRD pattern and (b) EDS spectrum of ZnO obtained by oxidizing Zn film in air by joule heating the Au wire HT-TCE to 450 °C for 45 min. (c) SEM image of ZnO thin film fabricated on Au network, (d) a magnified view.

IIIB.4.5 Conclusions

This study has dealt with pertinent issues related to using a transparent conducting electrode as a transparent heater (HT-TCE). While conventional electrodes made of ITO suffer from limited thermal stability, the new generation electrodes based on graphene, Ag nanowire or CNT networks though serve as HT-TCE, have shown limited performance due to crosswire junction resistance. In the method presented here, the Au wire micro/nanowire network is prepared by physically depositing the metal on a quartz substrate through crackle lithography. It is essentially a perforated thin film cast in the form of a wire network, devoid of crossbar junctions by design. It is not only a good transparent conductor (T, 87% and sheet resistance, 5.4 Ω/sq), but also a high temperature transparent heater. By applying a voltage of 15 V, it reached ~ 600 °C within 38 seconds with the current density of 5×10^5 A cm^{-2}. The temperature distribution was practically uniform across the substrate area. These findings make this HT-TCE quite unique among the literature examples. The joule heating also induced annealing of the metal grains in the wire network. Accordingly, the transmittance improved to 92% and the sheet resistance decreased to 3.2 Ω/sq, contrary to any conventional treatment. The study clearly demonstrates the possibility of making HT-TCEs capable of even higher temperatures by using, say, higher wire thickness or wires of refractory metals and alloys in place of Au.

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IIIB.5 Transparent strain sensor

Summary

This part deals with the development of transparent strain sensors using crackle lithography. A crackled template was made on a Si surface and Au metal was deposited in the cracks via electroless deposition by dipping the Si substrate in a plating solution. The Au wire network thus formed was transferred onto a PDMS layer, which partially embeds the wire network. The fabricated device showed a transmission of 85% with gauge factor of ~10^9 for strains up to 2.5%. These devices have been successfully employed to monitor human body part movements with degree of sensitivity.

IIIB.5.1 Introduction

The demand for flexible and wearable electronic devices[1-3] is growing in recent years due to their multi-functionalities and easy integration on human body.[4] Efforts have been devoted towards realization of highly sensitive and skin-mountable sensors.[1,5,6] For instance, they can be easily mounted on clothing or directly attached onto the body.[7] Various potential applications are in situations such as rehabilitation[8] and personal health monitoring, structural health monitoring, sports performance monitoring, human motion capturing for entertainment systems (e.g., motion capture for games and animation), and mass measurements.[9-10] In particular, highly stretchable and sensitive sensors are required in biomechanics, physiology, and kinesiology.[11]

Strain sensors measure local deformations by changing the electrical properties such as resistance or capacitance.[6,12,13] Strain sensors are mainly used for damage detection, characterization of structures and fatigue studies of materials.[14] The conventional strain

sensors fabricated with metal and semiconductor show poor stretchability and sensitivity i.e low gauge factors.[15] Most of them suffer due to lack of multi-directional strain sensing capabilities. Also, they have low resolution in nanoscale regime and cannot be embedded in structural materials. Nanomaterials such as nanoparticles,[16] nanotubes,[6] graphene[17] and nanowires[1] are alternative materials for strain sensing because of their exceptional mechanical and electrical properties. Strain sensors fabricated with zinc oxide nanowires,[18] carbon nanotubes (CNTs),[6] graphene[19] showed promising performance. Remarkably, nanomaterial can be embedded into structural materials and operate as both multidirectional and multifunctional sensors with high strain resolution even at the nanoscale.[20] The electromechanical properties of these strain sensors are far better than traditional sensors. However, in order to realize practical usage of the strain sensors, it demands high strain performance (i.e high gauge factors) in a broad strain range, along with fast response and high stability involving low fabrication cost. Importantly, the devices should prove an extra degree of freedom to integrate on any remote part of the body or skin. To reach such stringent requirements, novel nanomaterials, new fabrication methods and approaches have to be employed.

IIIB.5.2 Scope of the present investigation

The versatility of the crackle lithography could be exploited not only to realize metal networks in soft polymer matrices but also use them as flexible electrodes. In addition, there exists a possibility that a metal wire network under strain may show changes in resistance thus serving as strain sensor. Such transparent sensor may find applications in therapeutics.

PDMS may be chosen as a substrate for stretching experiment, because of its elastic properties. PDMS is known to serve as a substrate for transferring desired species; for example, it has been

used successfully to transfer graphene from catalyst surface. Given these possibilities, wire network may be realized on any substrate and transferred/embedded later. Once proven, this also opens up a route to solution processed metal deposition with a crackle template.

IIIB.5.3 Experimental Section

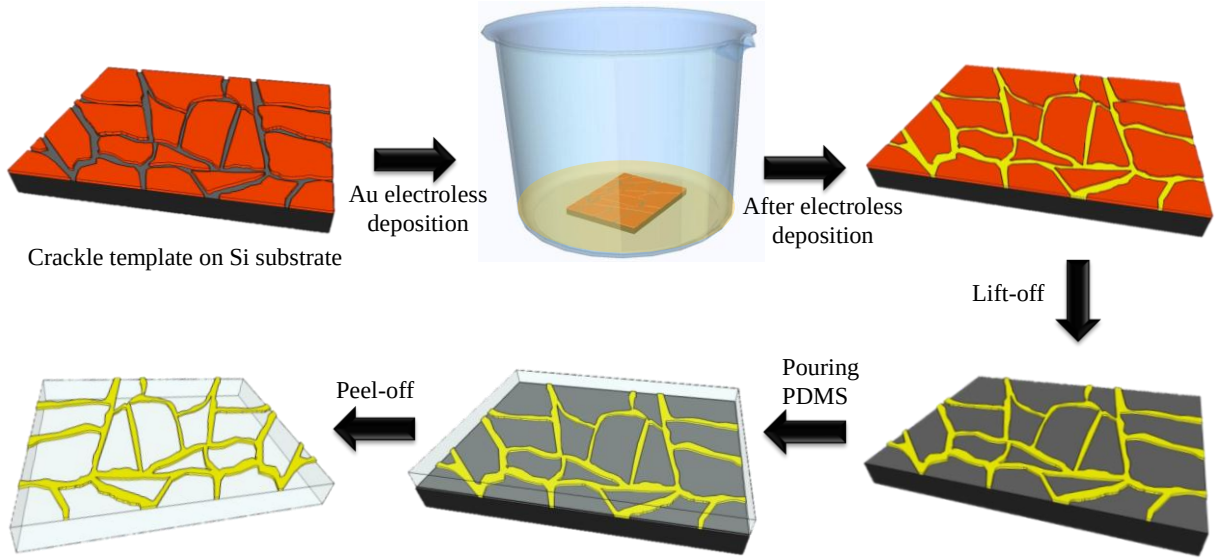

Figure IIIB.5.1 Schematic illustration of the fabrication of Au wire network on PDMS substrate through solution processed crackle lithography.

As shown in Figure IIIB.5.1a, crackle template was fabricated on Si substrate as described in Part-IIA, section IIA.3. After the formation of crackle template, the Si substrate was dipped in Au electroless plating solution. The plating solution was prepared with 25 mM $HAuCl_4$ in 5 M HF solution. The deposition was carried out for 3 minutes at room temperature. After 3 minutes, the Si substrate with crackle template was pulled out from the solution and cleaned with water (see Figure IIIB.5.1). Following the lift-off, a continuous Au wire network was formed on Si substrate. In the next step, PDMS (10:1 ratio elastomer to curing agent) was poured on the Au wire network/Si as shown in Figure IIIB.5.1. In order to cure PDMS, the substrate was heated in a hot air oven at 100 °C for 1 hr (thickness of PDMS ~ 2 mm). In the final step, the PDMS film was peeled off from the Si substrate; visibly, the Au wire network is seen completely transferred

onto PDMS without any breakage or discontinuity.

IIIB.5.4 Results and discussion

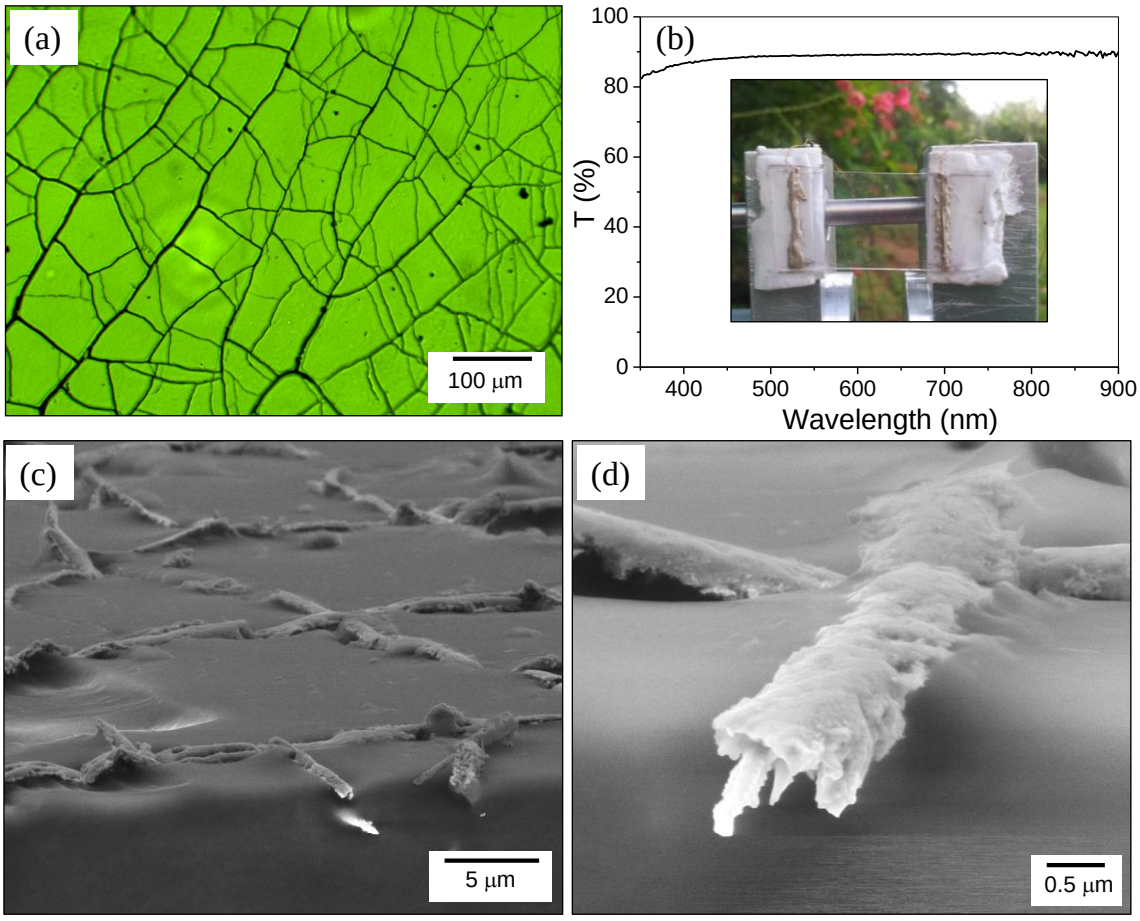

Figure IIIB.5.2 (a)Optical micrograph of Au wire network after transferring to PDMS substrate. (b) Transmittance spectrum of Au wire network/PDMS in the wavelength range 300-900 nm. Inset shows the photograph of the Au wire network/PDMS on screw gauge. (c) SEM image of Au wire network partially embedded in PDMS and (d) magnified view.

The optical micrograph In Figure IIIB.5.2a reveals the presence of Au wire network on PDMS, quite similar to vacuum deposited Au wire network shown in Part-IIA. The solution processed Au wire network is interconnected throughout the substrate without breakage even after transferring to PDMS substrate. The transmittance spectrum shown in the Figure IIIB.5.2b clearly demonstrates that the transmittance is around ~ 85%, which is also evident from the photograph in the inset of Figure IIIB.5.2b. In order to examine the stretchability of the Au wire

network, the device was glued to a screw gauge (see inset of Figure IIIB.5.2b) and the Ag epoxy contacts were taken from outside of the stretching area. Importantly, the sheet resistance was only 100 Ω/square. Interestingly, the Au wire networks are partially embedded in PDMS as shown in SEM image in Figure IIIB.5.2c, as expected. The magnified view of a single wire shows that at least 50% of the wire diameter is embedded in PDMS. The wire surface is rough and textured because of electroless deposition.[21]

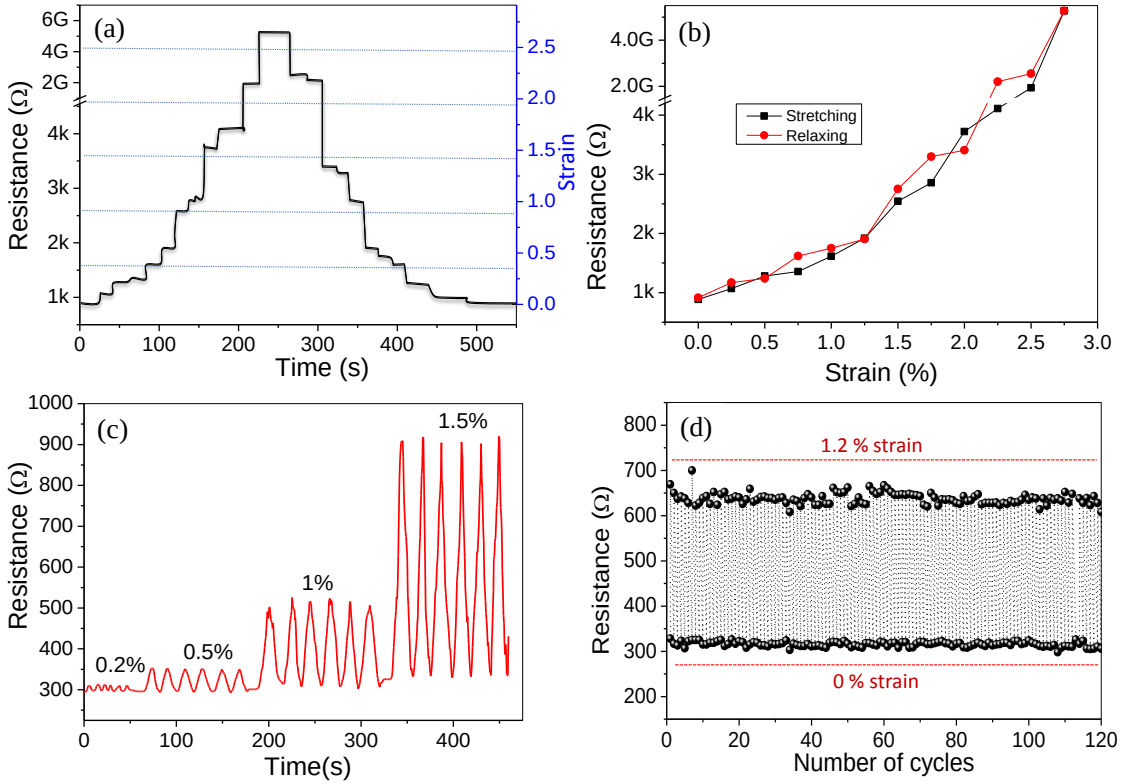

Figure IIIB.5.3 (a) Plot between the resistance of Au wire network/PDMS versus the applied strain as a function of time. (b) The resistance of Au wire network/PDMS for an applied strain during stretching and relaxing. (c) The resistance of the Au wire network/PDMS for 6 six stretching cycles at 0.2, 0.5, 1 and 1.5% strains and (d) the change in the resistance for a 120 stretching cycles between 0 and 1.2% strain.

The device resistance was monitored for each 50 μm stretching along its length using the screw gauge (least count, 10 μm). The strain was calculated using the following formula

$$\text{Strain} = \varepsilon = \Delta L/L \times 100\% \quad (1)$$

where ΔL is change in length and L is original length. As shown in Figure IIIB.5.3a, the device resistance was monitored as a function of time while stretching 50 μm in each step. With increase in the strain, jumps in resistance were observed, the jumps being quite discrete with respect to the strain. As shown in Figure IIIB.5.3a, the resistance increased from the initial 800 Ω to 4 kΩ at 1.7% strain. Beyond 1.7% strain device suddenly jumps to 2 GΩ, the device continued to respond to the applied strain and a maximum resistance of 5 GΩ was observed at 2.6% strain. Most strikingly, when the strain was gradually withdrawn, the resistance of the device retraced and reached its original value (see Figure IIIB.5.3a). The change in the resistance is shown in Figure IIIB.5.3b as a function of applied strain. The plot clearly depicts that the increase and decrease in the resistance is quite monotonous, without any observable hysteresis. Gauge factor is an important parameter to assess the performance of strain sensor. In this study, the gauge factors are calculated using the following equation.

$$\text{Gauge factor} = GF = (\Delta R/R)/\varepsilon \quad (2)$$

where ΔR is change in resistance, R is original resistance and ε is applied strain. For R = 850 Ω, $\Delta R = 5.2\times 10^{9}$ and ε = 0.0275. The estimated gauge factor for this device is 2.2×10^{8}, which is one of the best value reported in the literature.[1-4,6,9,10,12-14,16-19,22-24] The fabricated strain sensor is taken through a cycled strain at various strain values as shown in Figure IIIB.5.3c. In a single strain cycle, the strain was applied and then released to its rest position; likewise 6 cycles were performed on the device at various strains. As the strain increased, the change in the resistance also increased as shown in Figure IIIB.5.3c. Further, switching between strain values of 1.2% and 0%, 120 stretching cycles were performed on the same device. The device performance was consistent within 5%.

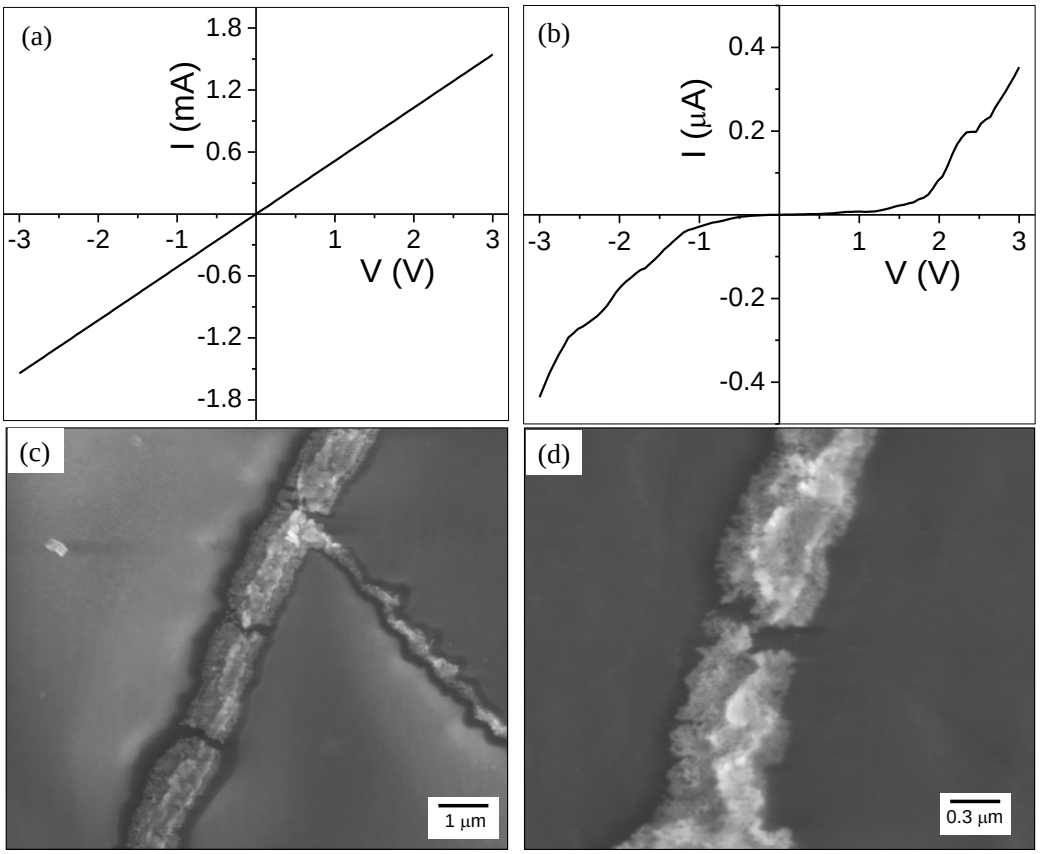

Figure IIIB.5.4 I-V characteristics of Au wire network/PDMS at (a) 0% and (b) 2.5% applied strain.(c) SEM image of Au wire network after applying 2.7% strain, and (d) magnified view.

In order to understand the mechanism of the strain sensing, microscopy and electrical characterization was done on the strained network. In the relaxed state (rest position) of the device, I-V characteristics were linear as shown in Figure IIIB.5.4a, indicating that the conduction is ohmic throughout the network. In this case, all Au wires must be well connected as shown in Figure IIIB.5.2a. However, with 2.7% applied strain, the I-V characteristics became non-linear as shown in Figure IIIB.5.4b. This may be attributed to the breakage and opening of gaps in the wire network. The device was examined carefully in SEM during in-situ application of 2.7% strain. The SEM image in Figure IIIB.5.4c clearly shows opening of the gaps in wire network. A magnified view in Figure IIIB.5.4c reveals that the gaps are around few nanometres to ~ 100 nm. The non-linear I-V characteristics therefore arise due to the tunnelling or

filamentary conduction in the wire network under high strain. Interestingly, all gaps get closed with release of strain giving again linear IV characteristics.

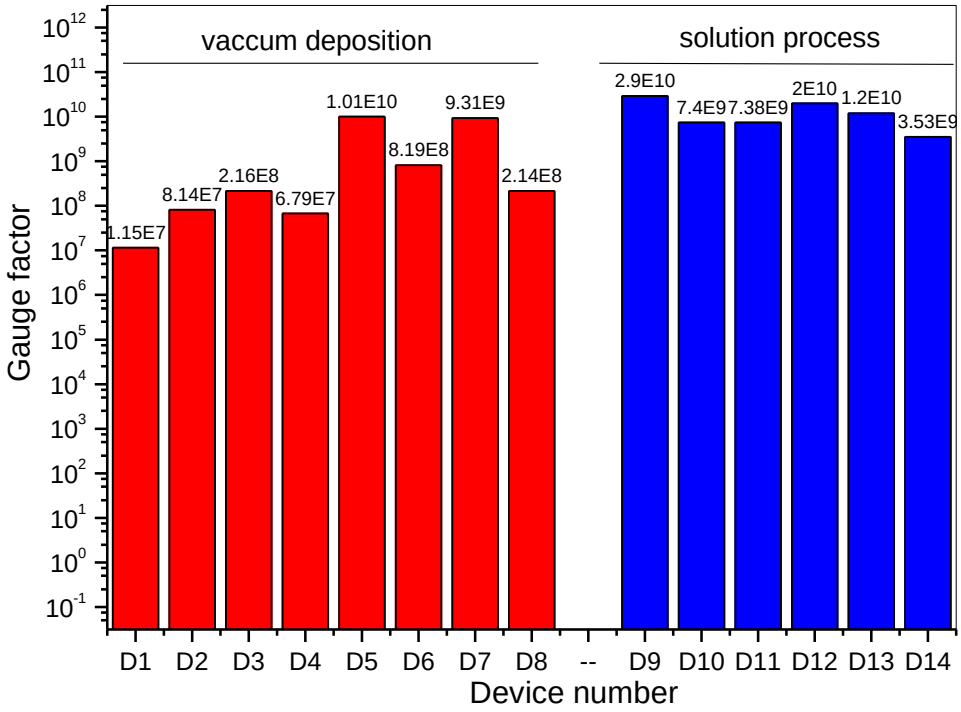

Figure IIIB.5.5 Gauge factor histograms of various devices fabricated through vacuum deposition and solution processed crackle lithography.

In order to examine reproducibility and reliability of the fabrication process, various devices were fabricated using vacuum deposition and solution processed deposition of the metal, while keeping rest of process unchanged. The gauge factors of all devices fabricated in study is shown in the form of a histogram (see Figure IIIB.5.5). From the histogram, it is clear that there is more variation in the gauge factors of sensors obtained from vacuum deposition (blue bars in Figure IIIB.5.5), whereas solution processed devices showed consistent and high gauge factors (red bars in Figure IIIB.5.5). Thus, the solution processed crackle lithography is a promising method to fabricate consistent and reliable strain sensors.

Transparency of the sensor is an additional attribute though it need not contribute functionally. However in the context of therapeutics it may add a great value, particularly in

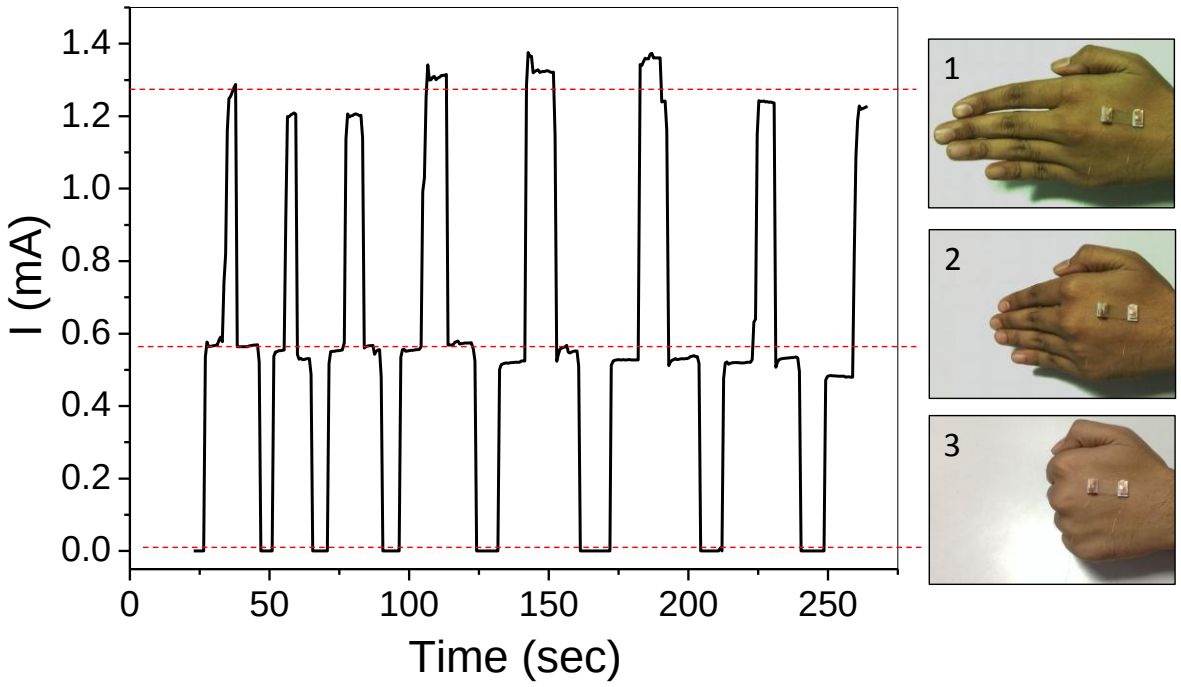

Figure IIIB.5.6 Current passing through the Au wire network/PDMS, while performing the three gestures of hand. Photographs were taken at three different gestures of the hand.

situations where the sensor is to be concealed while being attached to the outer parts of the body of an individual such as face or hand, not affecting the aesthetic appearance. Transparency of the sensor plays important role if the device should enable a physician to see through it for monitor the underlying skin/body part for possible swelling, injuries or for rashes. Here, the utility of transparent strain sensor was examined in two contexts. The sensor was placed on opisthenar area of a volunteer's hand as shown in the photographs in Figure IIIB.5.6. The current passing through the device was monitored as a function of hand gestures. The photographs show three hand gestures, where the hand was held momentarily at those positions during stretching and releasing of the hand grip. The device showed ~1.3 mA in gesture '1' i.e completely relaxed position and in '2' gesture i.e partially stretched position, the current was ~0.5 mA, whereas in '3' gesture i.e completely stretched position, the device showed ~2 nA indicating near complete

breakage of the wire network. In this way, 8 cycles were performed and the changes were reproducible as shown in Figure IIIB.5.6.

In second context, the device was placed on left temple area of a volunteers' head above the facial nerve as shown in the photograph in Figure IIIB.5.7a. The main focus of this experiment is to monitor the differential facial nerve movements while eating different food articles, as the concerned serve is directly linked to jaw movements. In the relaxed state, of the facial nerve, the device is in rest position and while eating food articles the facial nerve strained and stress translates to the device as shown in the schematic in Figure IIIB.5.7b. Thus, the strain, relaxation or compression in the facial nerve could be directly transferred to the strain sensor. Four food articles were consumed each bearing different properties such as potato chips (crispy), chocolate (soft), ground nut (hard, powdery) and chewing gum (soft and eleastic). In first example, potato chips were consumed while the device current was monitored as showed in Figure IIIB.5.7c. The prehension of potato chip increased the current sharply marked with red color curve in Figure IIIB.5.7c.

During mastication, the current showed spike-like features with minimum current even below the initial (rest) value, indicating that the sensor measured both signs of strain (tension and compression). A single mastication cycle was thus a compression-tension cycle in the facial nerve, which was clearly reflected in the current (see Figure IIIB.5.7c). At the end of mastication, the oscillations died down in amplitude corresponding to swallowing stage. In case of chocolate mastication, the decrease in the oscillation amplitude was less due to the soft nature of the food article (see Figure IIIB.5.7d). Conversely, during mastication of a ground nut, the oscillation amplitude decreased rapidly due to its powdery nature and came to relaxed state after 8-10 mastication cycles as shown in the Figure IIIB.5.7e. On the other hand, the oscillation

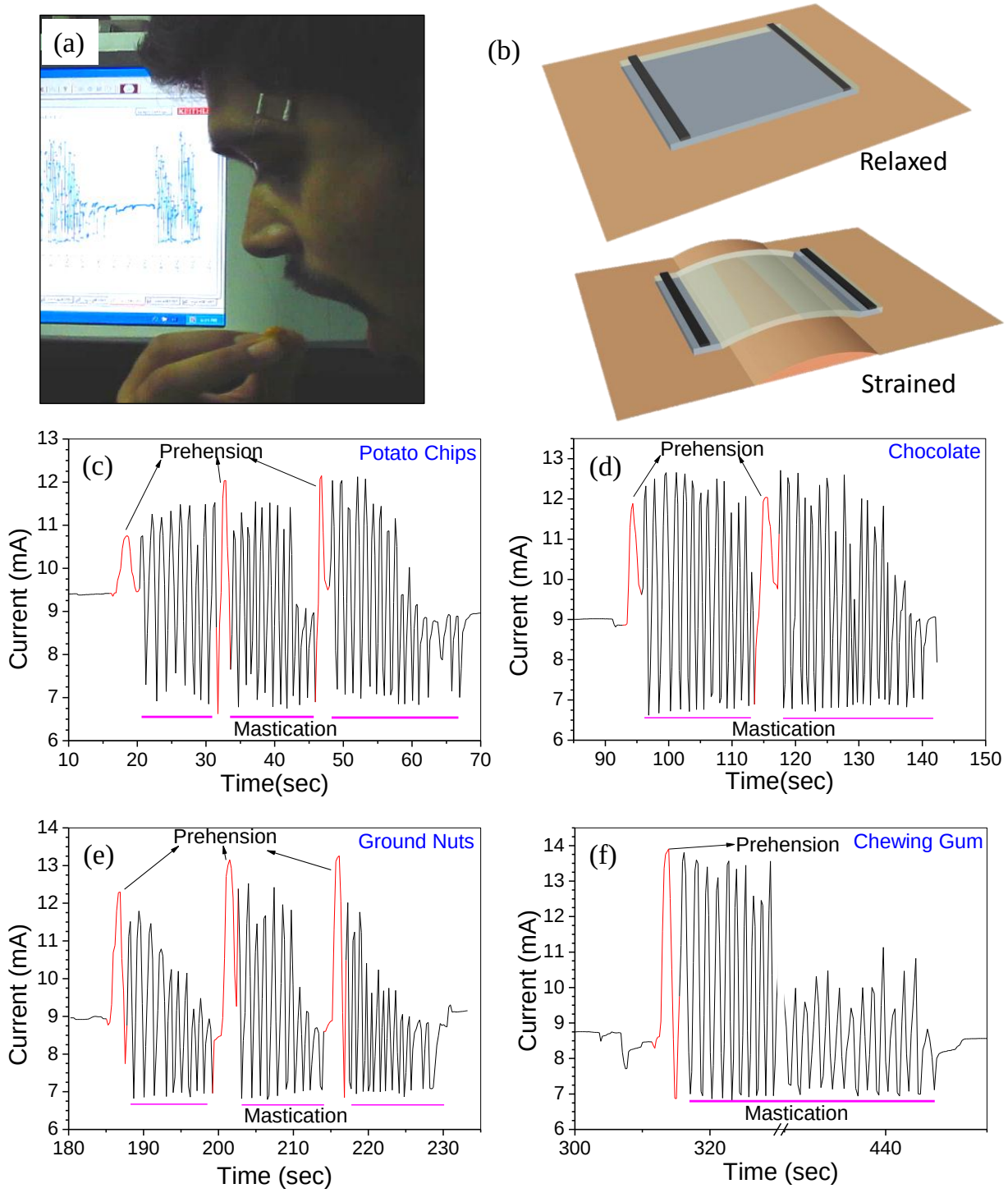

Figure IIIB.5.7 (a) Schematic illustration of the strain sensor at relaxed and strained positions. (b) Photograph of the volunteer, where the device was struck on top the facial nerve, during the intake of food. The current passing through the Au wire network/PDMS, while the volunteer eats (c) potato chips, (d) chocolate, (e) ground nut and (f) chewing gum, where red color indicates prehension of the food and black color mastication of the food.

frequency in the case of the chewing gum was relatively high and decrease in the amplitude was very slow. It did not come back to the relaxed state at all and the mastication was forcefully stopped (see Figure IIIB.5.7f). This is attributed to the soft and elastic nature of the chewing gum. Hence, the strain sensor fabrication in this method is able to sense eating of various food articles with well differentiated signals. Such a device can be easily integrated on any part of the body and highly local body movements can be monitored. This may be used in the automatic monitoring of the hand gestures or other parts of body as a patient recovers from an injury or fracture of bones.

IIIB.5.5 Conclusions

In this study, transparent strain sensors were fabricated through solution processed crackle lithography with 85% transmittance and 100 Ω/sq sheet resistance. The strain sensor was realized with Au wire network partially embedded in PDMS matrix. This is crucial for the strain sensing action, as the wire network held embedded in PDMS responds well to an applied strain, in terms of breaking and forming of the nanogaps. In the unstrained condition, ohmic type of conduction is seen through the network while tunneling or filamentary conduction appears during strain. The fabrication process is highly reproducible, with consistent gauge factors ~10^9. This transparent strain sensor has been employed in monitoring hand gestures and facial nerve movements while eating different food articles. In both cases, highly reliable responses have been obtained.

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Chapter IV

In-plane multi-level resistive switching in PdO thin films

Summary

Resistive random access memory (RRAM) is the most promising candidate for the next generation non-volatile memory. In this study for the first time, resistive switching in PdO thin film devices has been investigated. The PdO thin films were obtained by thermolyzing the Pd hexadecanethiolate in oxygen atmosphere. The devices showed multiple memory states (MMS) as many as five, under ambient conditions. Both continuous voltage sweeps and millisecond voltage pulses have been employed for memory state switching. The memory characteristics of the devices are found to be excellent. Memory retention was examined for 10^3 s while multistate endurance was studied for 25 cycles with no noticeable degradation by randomly switching the memory state. Unlike resistive switching devices reported in the literature which are generally non-ohmic, these states exhibited linear I-V characteristics below 1 V. The low temperature measurements have revealed variable rang hopping (VRH) type of conduction, the activation energy increasing with the number of the state. SEM, EDAX and Raman spectroscopy have also been performed and on the basis of these measurements, reversible oxidation/reduction of Pd/PdO is found to be responsible for resistive switching action. For the first time, an attempt has been made to quantify the efficiency of a MMS device by defining "multiplex number (M)". M, is defined as the sum of total number of memory states and the ratio between the number of switching events observed in a device and the total number of possible switching events. The present PdO MMS device exhibited M value of 5.7, which was compared to estimates done on literature examples, is significantly high. Such high performance MMS in PdO devices makes it a potential candidate RRAM and neuromorphic circuits.

IV.1 Introduction

Resistive random access memory is a promising candidate for the next generation non-volatile memory, due to simple fabrication, low drive power, high speed operation, excellent scalability and high storage density.[1, 2] A simple resistive memory device is a two terminal device which consist of metal-insulator-metal (MIM) structure. Resistive switching (RS) phenomenon has been observed in various metal oxides such as TiO_2, HfO_x, NiO and TaO_x etc, as well as with metal chalcogenides, carbon nanotubes and organic materials.[3-9] In general in the above examples, the devices have shown high performance with respect to two state resistive switching. In the recent past, multilevel resistive switching has gained much importance due to the possibility of high density memory storage, with little change in the bit dimension.[10-11] This explains the surge of activity in the recent literature reporting multiple memory states (MMS) devices made of a variety of materials. Most of the MMS devices using oxides such as Al_2O_3 and HfO_2, which showed 3 or 4 memory states.[10-34] There are few attempts in the literature to achieve 5 or more number of resistance states with active elements such as NiO-Pt, CuO_x, TiO_2, SiO_2 and HfO_x etc.[35-40] However, these devices suffer from poor reliability and unfavorable operating voltages.[41-42] The improvements in device fabrication and performance require a deep insight into RS mechanism. Various theoretical models have been proposed in this direction involving filamentary conduction, charge trapping as well as electro-migration.[3, 40, 43] In-situ TEM, SEM and Raman spectroscopy measurements have also been employed to understand the RS mechanism.[7, 37, 31, 44] Nevertheless, the progress in RS device fabrication is not hindered.

Memory devices are switched into different resistive states either by current induced[34] or voltage induced processes.[35] Although there are few examples in the literature employing

current induced MMS devices, often this process causes a distribution in the resistance state leading to poorer endurance.[34] On the other hand, MMS devices working with voltage pulses are more popular due to higher reliability.[35] In this case, switching to a memory state often requires resetting to the initial resistive state. Recently, Zhao et al. showed RS action with as many as eight states with voltage pulse, but switching in between the states is not considered.[45] Huang et al. showed 5 resistance states with increasing the number of voltage pulses; however all the switching events have not been realized.[35]

IV.2 Scope of the present investigation

The practical usage of the MMS device involves switching between all possible combinations of the resistance/memory states. So far MMS devices reported in the literature demonstrated switching ability between a lowest resistance state (LRS) and several high resistance states (HRS1, HRS2 etc.) or switching between the neighboring states. However, an aspect which is given less attention is randomly switching in-between any two resistance states, not necessarily neighboring states. The fabrication of such enabled MMS devices not only requires a complete understanding of the underlying switching mechanism but also a precise control over the oxidation/reduction of the active material or the motion of charge carriers in between the metal electrodes, as the case may be. Ideally, the MMS device should be driven with low input voltages and switching should happen under ambient conditions. Such stringent requirements invoke the development of novel active materials for resistive switching.

In this part, PdO thin film has been explored as active element for MMS RS devices. PdO was chosen as a novel active element for RS because of the possibility of reversible reduction and surface oxidation under ambient conditions.[46] In this study, additional effort has been made to examine switching in-between any combination of resistive states. For this purpose, in-plane

geometry of electrodes was considered more appropriate. The ability to switch freely was quantified using a new term, 'multiplex number' (M). Further, the switching mechanism has been examined with Raman spectroscopy and low temperature resistance measurements.

IV.3 Experimental Section

Mica/quartz substrates were subsequently cleaned and ultrasonicated in water, Acetone and IPA, dried with N_2 gas. A 100 μL of 50 mM Pd hexadecaylthiolate was drop-coated on the substrate at room temperature and then the substrate was thermolyzed at 250 °C for 2 hours in air and at 600 ºC for 3 hours in oxygen atmosphere. Thus formed PdO thin film was used for the device fabrication. A 50 nm thick ~ 7 μm wide Au gap electrodes were deposited using a thin carbon fiber as shadow mask by physical vapor deposition (Hind High Vacuum Co., India). As fabricated PdO device with Au electrodes and electrical characterization was done using a Keithley 4200/236, which served as the source and measurement unit. SEM was carried out using a Nova Nano SEM 600 instrument (FEI Co., The Netherlands). A Perkin−Elmer Lambda 900 UV/visible/near-IR spectrophotometer was used to do the absorption spectra. Raman maps were collected by stitching 2500 Raman spectra of PdO thin film.

IV.4 Results and discussion:

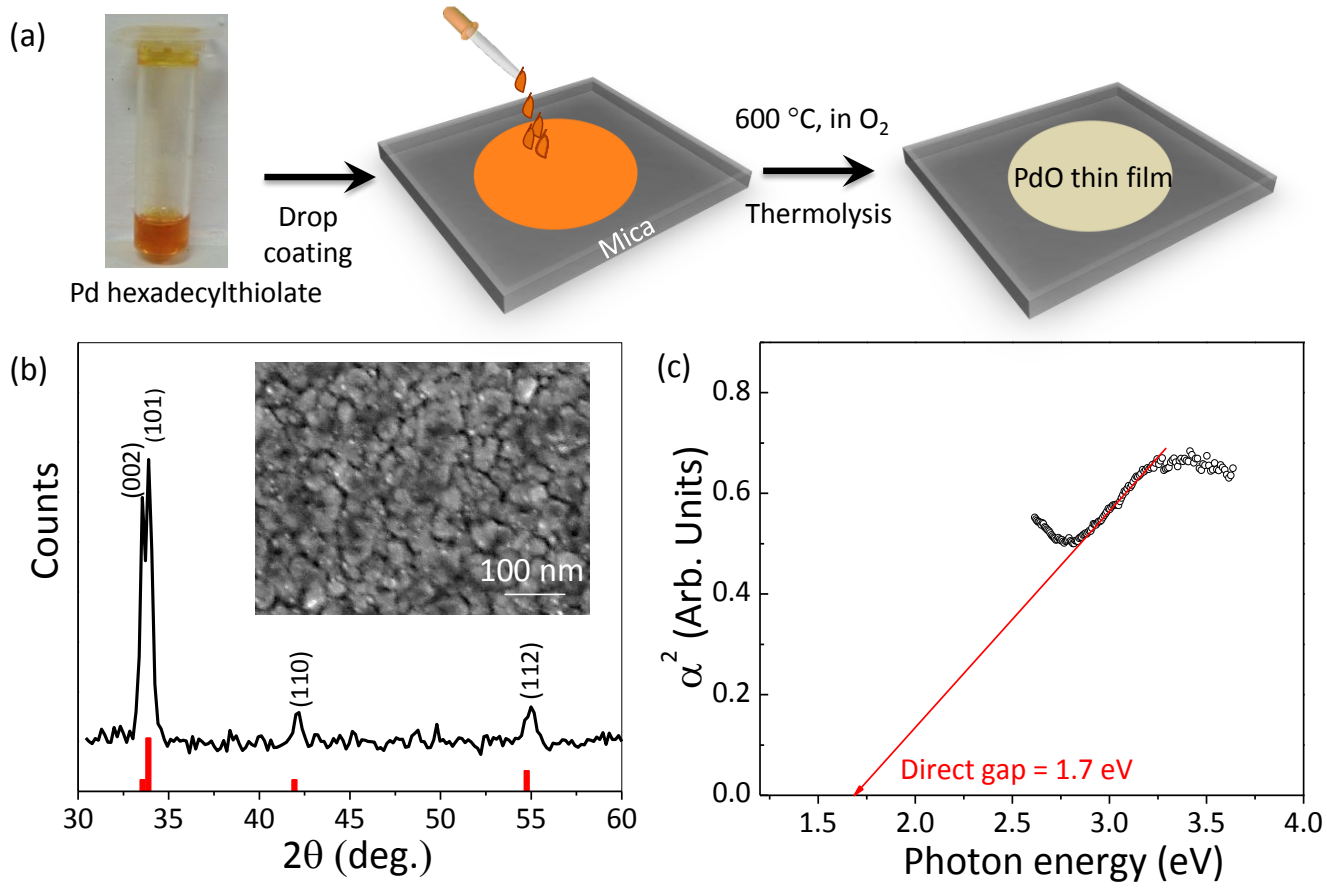

Figure IV.1 (a) Schematic illustration of the synthesis of PdO thin film. Characterization of PdO thin film, (b) XRD pattern indexed with JCPDS file number-431024, where standard peaks are marked in red. Inset shows a typical SEM image. (c) Variation in absorbance coefficient with photon energy.

The first few steps in device fabrication involve synthesis of PdO film on a mica substrate as shown in schematic in Figure IV.1a. Pd hexadecylthiolate was drop-coated on the substrate and was thermolyzed at 600 ºC in oxygen. As the organic components were removed, the film turned brownish black marking the formation of PdO. The XRD pattern in Figure IV.1b shows the presence of crystalline tetragonal phase of PdO which is indexed with JCPDS (no. 431024). The particle size was calculated by using the following Scherrer formula

$$D = {(0.9 \times \lambda)}/{(\beta \times cos\theta)} \quad (1)$$

where D is particle diameter, λ =1.54 Å is wave length of X-rays, β = 0.003 rad is full width half maximum (FWHM) and θ = 16.9° is Bragg angle. The estimated particle size using the equation (1) is ~ 48 nm. The SEM image in the inset of Figure IV.1b shows particles in the size range of 20 - 50 nm well packed into a continuous film of measured thickness ~ 50 nm. An optical band gap of ~ 1.7 eV was estimated from the UV-vis absorption data (Figure IV.1c), which may be compared with the literature value of ~ 2 eV for PdO.[47]

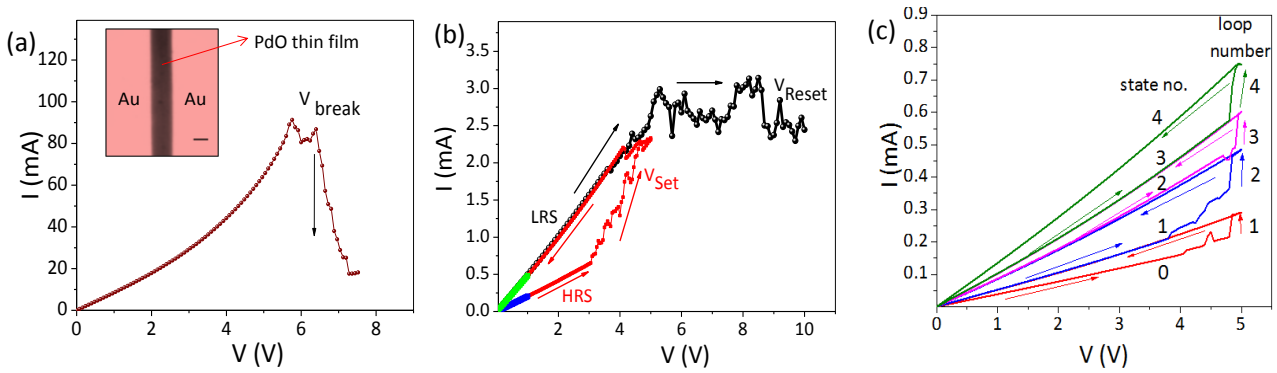

Figure IV.2 (a) I-V characteristics of the voltage-controlled forming process in device-8. Inset represents the optical micrograph of PdO thin film device along with in-plane Au electrodes (scale bar 5 μm). (b) Typical switching characteristics of device-3. LRS, the low resistance state and HRS, high resistance state are marked. Blue and green lines near origin refer to reading of the respective state. (c) Consecutive voltage cycling from 0 to 5 V (arrows indicate the direction of voltage sweeps). Voltage scan rate, 0.5 V/s in (a) and (b), and 3 V/s in (c).

An in-plane resistive switching device was fabricated by depositing Au metal electrodes on top of PdO film by shadow masking a gap of ~7 μm (see inset in Figure IV.2a) across the entire length (3 mm) of the film. To initiate resistive switching, the device was taken through a forming process (Figure IV.2a) by varying the applied voltage.[48] As the voltage was increased from 0 to 7 V, the current increased sub-linearly before showing a breakdown around 6 V. This is a forming behaviour in which a highly conducting pristine device (~ 100 Ω) is taken to a less conducting state (~ 2 kΩ) irreversibly. In the RESET process, a subsequent voltage sweep was

performed (see black curve in Figure IV.2b). The device showed a similar linear increase in current up to ~ 5 V beyond which, it became non-steady. The resistance of the device was measured by sweeping voltage from 0 to 1 V (blue line) and this value is assigned as a high resistance state (HRS). In order to revert back to LRS, a voltage cycle of 0 to 5 to 0 V was applied (red line). The curve trailed the HRS up to ~ 3.6 V, beyond which it became unsteady only to increase and settle in the LRS at ~ 5 V. This state of the device was again measured by sweep voltage from 0 to 1 V (green line). Thus, two resistance states namely LRS and HRS got defined for the fabricated PdO device with V_{reset} (LRS to HRS) and V_{set} (HRS to LRS) at ~ 10, 5 V respectively and with V_{read} of < 1 V. Likewise, several devices were activated (see Table IV.1).

Table IV.1: Summary of the resistive switching devices made in this study

Device no.	**Resistance (kΩ)**	
	Low resistance state (LRS)	**High resistance state (HRS)**
1	1.4	2.2
2	8.1	11.0
3	3.0	9.0
4	6.0	9.0
5	9.0	13.3
6	4.2	7.1
7	11.0	25.1
8	2.1	5.0
9	9.0	12.0
10	6.1	9.3
11	3.0	7.0

From these measurements, it is evident that PdO can potentially be used to define resistive memory states. In order to explore the existence of resistance states in between LRS and HRS, the SET process was performed with a faster scan rate of 3V/s (see Figure IV.2b) as compared 0.5V/s in Figure IV.2b. As shown in the Figure IV.2c, voltage of a given polarity is cycled several times to take the device sequentially from one resistive state to the next.[49] During the consecutive voltage sweeps (see Figure IV.2c), hysteresis in current with 0 to 5 to 0 V cycles is evident in the form of 'touching loops'; after the first cycle, the resistance of the device switched to second state at 4.8 V. Likewise, it was possible to switch to four increasingly lower resistance states and finally reached its initial LRS. In short, the PdO showed tuneable multiple memory states. Interestingly in the present case, the touching loops are linear unlike those in many literature examples.[49-51] What is interesting is that the device works in 'in-plane' (2D) configuration and that the RS curves are linear over the operating voltage range, requiring small readout voltages.

Remarkably, multilevel resistive switching in the PdO device can be achieved by applying different RESET voltage sweeps. As shown in Figure IV.3a, tuneable high resistance states were obtained with increasing RESET voltage sweeps up to 8, 10, 12 and 15 V, respectively. In RESET processes, the device was stable in LRS up to 5 V independent of applied voltage, beyond which four HRSs got defined. With increase in the RESET voltage, the HRS resistance increased, and beyond 15 V the device became unstable. Importantly, the device got retrieved back to the LRS (0 state) with a 0-5V cycle from all four HRSs (1 (red), 2 (green), 3 (blue) and 4 (brown) states). The PdO device showed stable and reversible multilevel resistive switching in ambient atmosphere. More interestingly, the PdO device can also be switched to

different HRSs by applying a voltage pulse. In this approach, a set of increasingly higher voltage pulses, 5 to 8, 10, 12, 15 V, were applied to the PdO device for 20 ms.

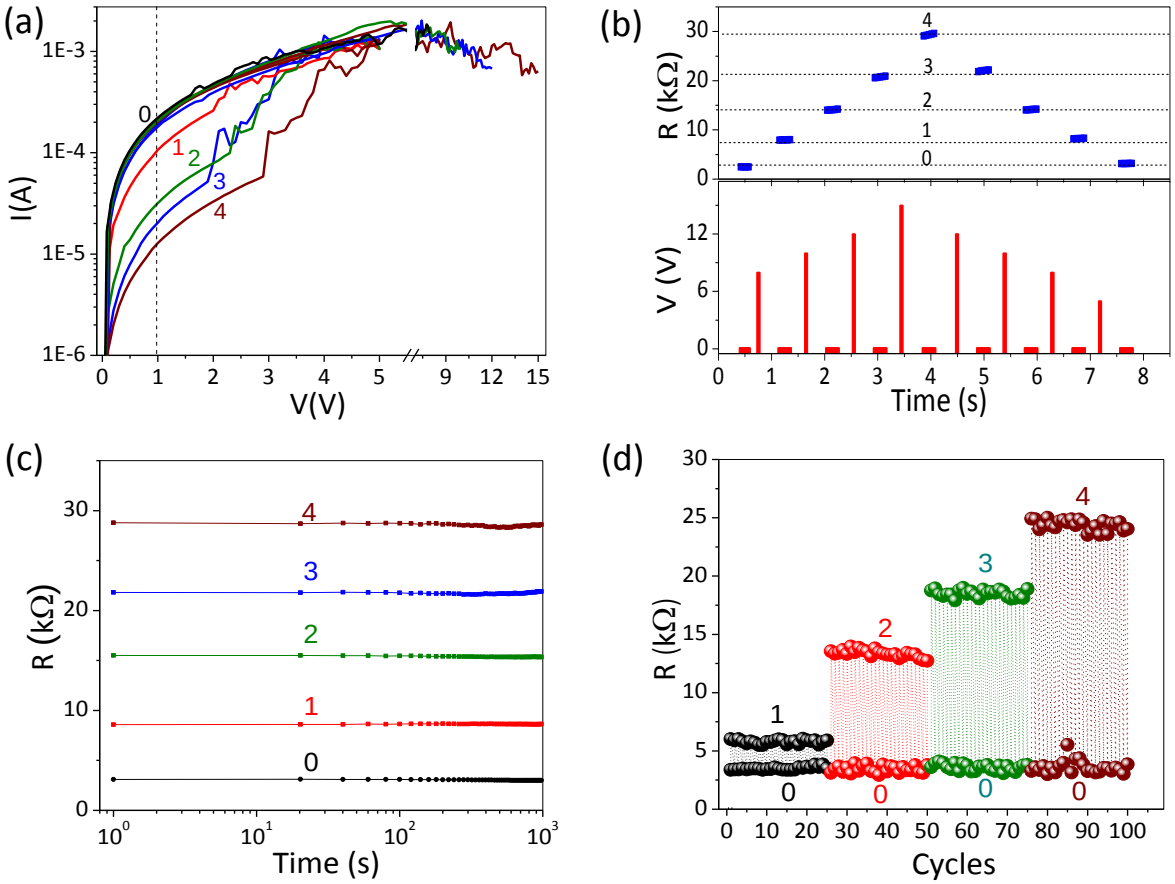

Figure IV.3 Electrical characteristics of the PdO device: (a) Consecutive RESET voltage sweeps 8V (red), 10V (green), 12V (blue) and 15V (brown) and each RESET process is followed by a SET process by applying a 0-5V cycle in device-17. (b) Top, resistance states achieved with different applied voltage pulses 5, 8, 10, 12, and 15 V (pulse duration 20 ms) and bottom, resistance read out using a reading voltage 10 mV (duration 0.5 s). The time scales in the bottom panel are magnified for better visibility in device-16. (c) Retention (device-16) and (d) endurance (device-13) of the MMS device.

Figure IV.3b shows the resistance values (top panel) corresponding to the different memory states obtained using programmable voltage pulses (bottom panel) while being readout by applying 10 mV. Thus, it was possible to switch steadily from the state '0' to state '4' and vice-versa, with the predetermined voltages. Interestingly, the resistance values obtained match well with those from the first approach using continuous voltage sweeps. Likewise, several

devices were initiated into MMS (see Figure IV.4), emphasising the versatile nature of PdO for memory device applications.

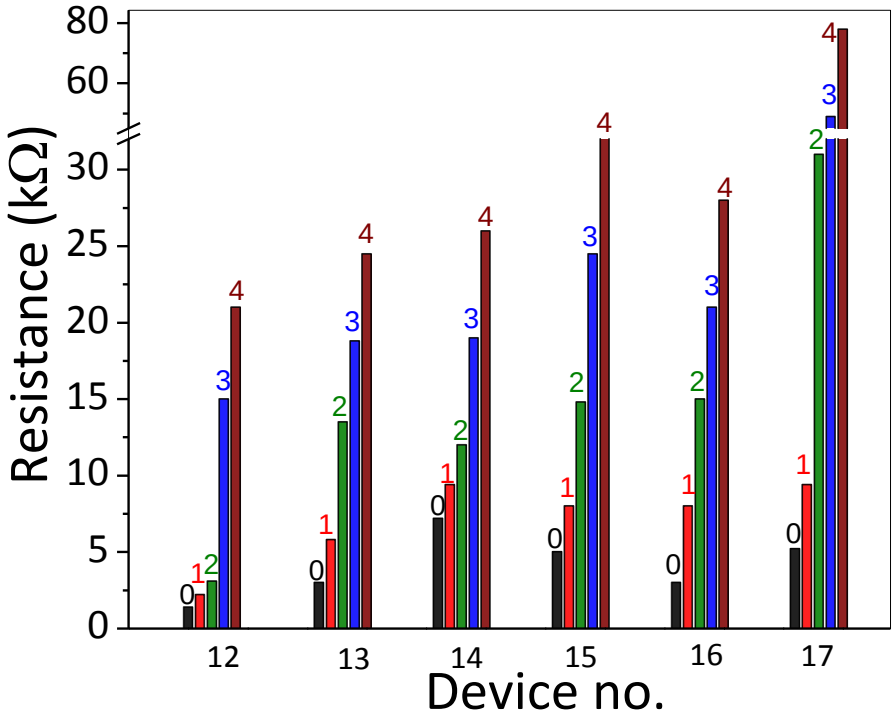

Figure IV.4 The resistances verses number of the devices for six representative PdO MMS devices.

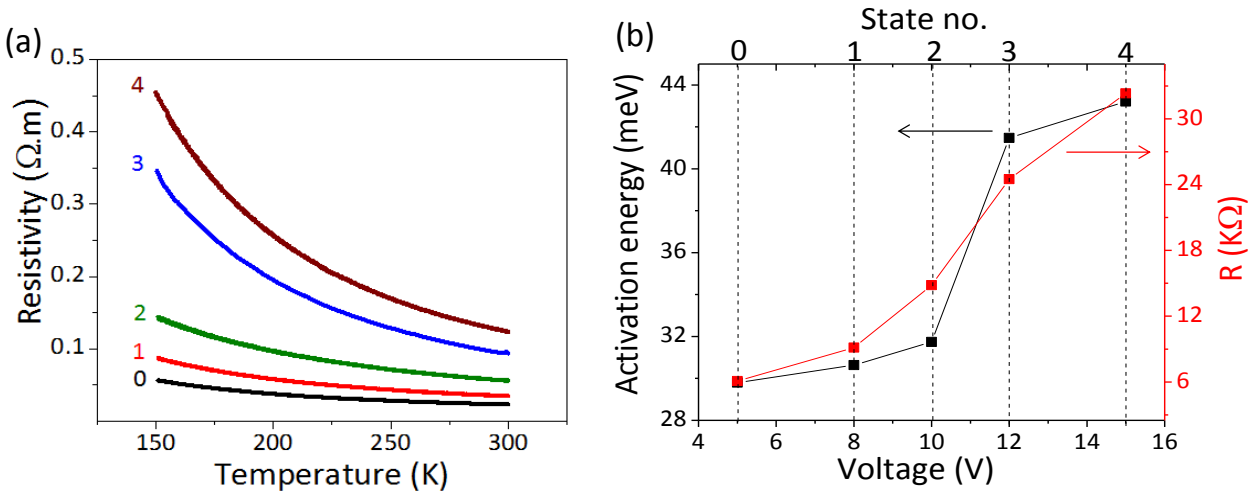

Figure IV.5 (a) Resistivity measurements of all five resistance memory states from 150 to 300 K. (b) Estimated activation energy from the VRH model, compared with room temperature resistance for each state in device-15.

The persistence of these MMS is studied in endurance study. Using 10 mV reading voltage, each state was monitored for 10^3 s as shown in Figure IV.3c. It can be noted that, even though the states are close, they remain well separated consistently over the long periods of time. The resistance variation was less than 3%, 0.5%, 0.9%, 1% and 1.7%, respectively for the 0-4 states, demonstrating high stability of the PdO MMS device. Further, its nifty performance in dynamically switching between the states interchangeably is also demonstrated (see Figure IV.3d). Thus, PdO MMS device showed a consistent, reliable and controllable multilevel resistive switching which can be used in MMS devices.

In order to understand the nature of electrical transport, temperature dependent resistance measurements were carried out while the device was made to stay in different memory states (Figure IV.5a). In each state, the resistivity was found to increase with decreasing temperature revealing the semiconducting nature. Generally, metallic conduction have been observed in many resistive state materials such as in Ta_2O_{5-x}[52] and NiO[53] with metallic species resulting from oxide reduction forming filamentous paths in the insulating matrix. The contact material may also play a role in deciding metallic or semiconducting nature of the filament.[54] The data obtained (Figure IV.5a) was fitted with variable range hopping (VRH) equation,[55]

$$R(T) = R_0 \exp[(T_o/T)^{\alpha}] \quad (2)$$

Where *R(T)* is temperature dependent resistance, R_0 is temperature independent pre-factor, T_o is characteristic temperature and α is exponent. The best fit for the low temperature data was obtained with α=1/3, indicating a 2D VRH type conduction in nanocrystalline Pd-PdO system.[55] The estimated activation energy values from the VRH model, the room temperature resistance and the corresponding V_{reset} values are shown in Figure IV.5b in the form of a plot

against the designated memory states. The activation energy is seen to increase with the state, indicating an increase in the barrier height for the charge carriers in between PdO nanoparticles.

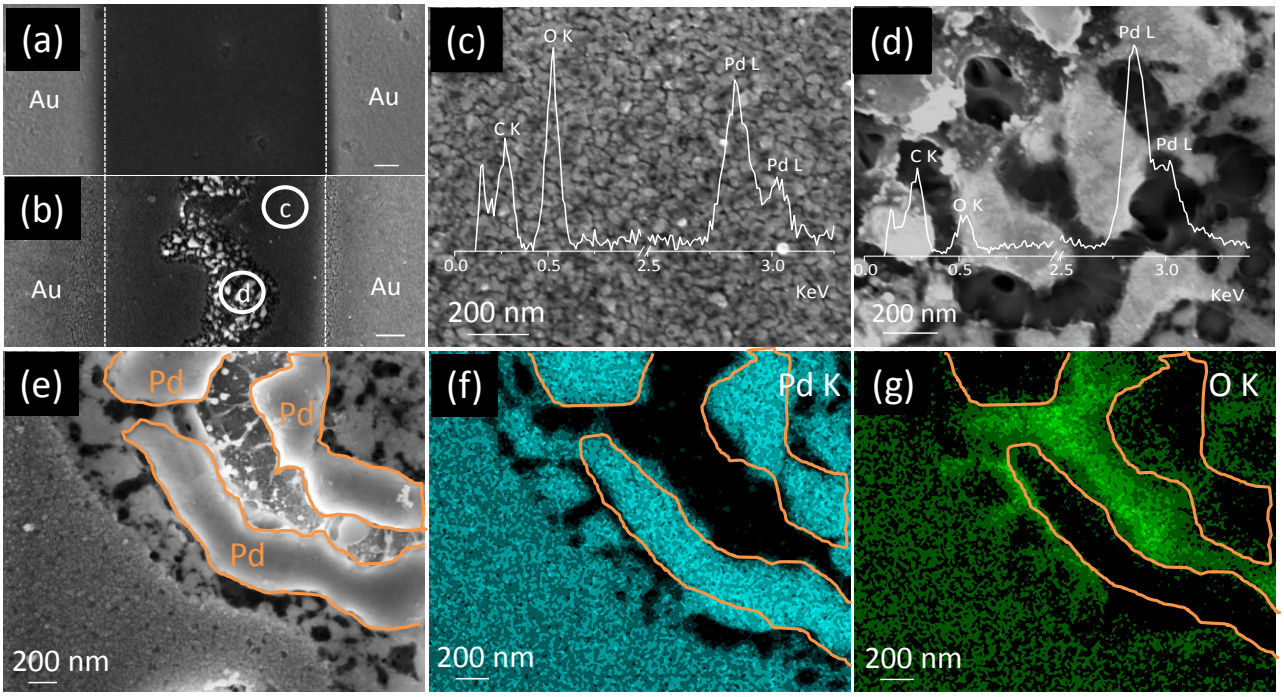

Figure IV.6 Microscopy analysis of the device active area, (a) before and (b) after forming. Outside (C) and in the cracked (d) regions. An interface region shown in (e) SEM image with corresponding Pd K (f) and O K (g) EDS maps.

This novel behaviour of PdO MMS device deserves careful microscopy analysis (Figure IV.6). Following the forming step, SEM imaging revealed a crack of width 1-3 µm in the PdO film (Figure IV.6a and 6b) near the centre of the gap electrodes along the entire length (~2 mm), while the region close to the electrodes remained unchanged (marked as 'c' in Figure IV.6b and Figure IV.6c). Similar observations have been reported in SiO_2 as a substrate with graphene electrodes.[35] The magnified view of the crack region 'd', shown in Figure IV.6b reveals a random distribution of particle agglomerates in the range 0.2 to 2.5 µm (Figure IV.6d). What is noteworthy is that the EDS analysis of these two regions showed significant differences with respect to oxygen signal as seen in Figure IV.6c and 6d. The agglomerates (coloured white) in

region ‘d’ show the predominant presence of Pd with very little oxygen. This is also confirmed by EDS measurements shown in Figure IV.6f and 6g corresponding to the magnified portion of PdO-crack in Figure IV.6e. In the forming process due to large current through the PdO thin film, Joule heating is expected which can locally convert PdO to Pd, provided favourable temperature (~ 500 K, ref) is achieved. As heat dissipation is relatively less in the gap region, this process begins in the centre of the gap due to thermal gradient.[56] The metallic Pd filaments lead to LRS after forming, which is crucial for the PdO MMS device.

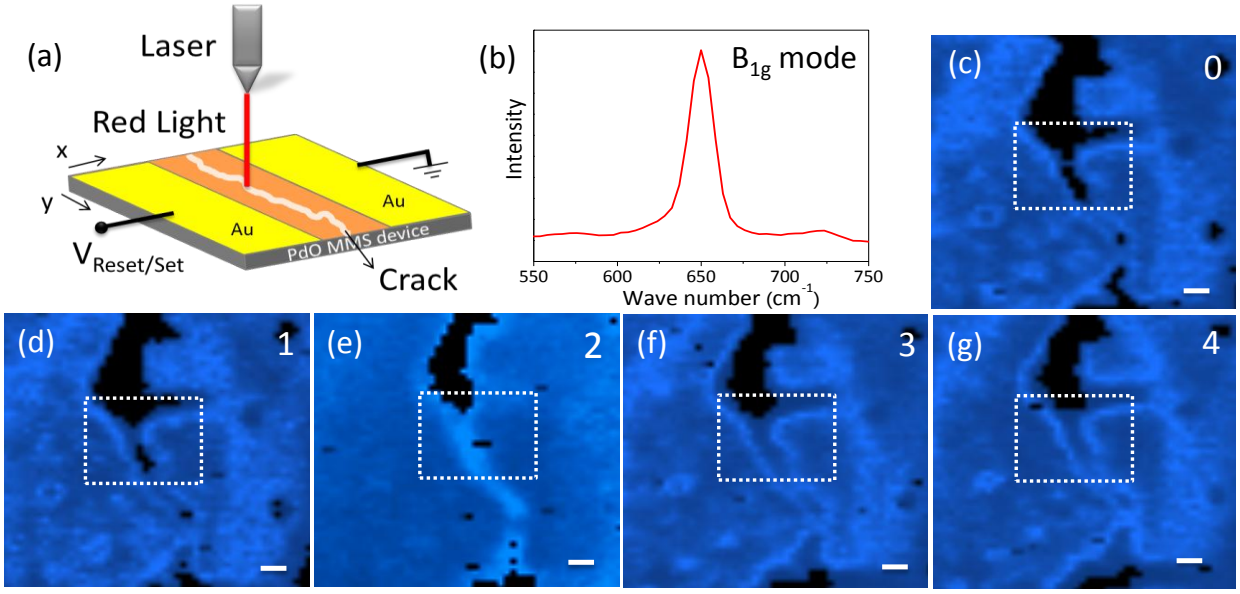

Figure IV.7 (a) Schematic illustration of the Raman spectroscopy measurements of an active MMS device. (b) Raman spectrum of the PdO thin film, showing B_{1g} mode. (c) to (g) Raman mapping of PdO signal near cracked region after applying 5, 8, 10, 12 and 15 V respectively to achieve the different resistance states (scale bar 200 nm). The number at the top right corner represents memory state. The rectangular box represents the active area of the device. Blue and black regions stand for the presence and absence of the PdO signal, respectively in device-12.

To elaborate and investigate the importance of observed spatial distribution of Pd and PdO species, Raman mapping was carried out across the crack region while the device was maintained at different memory states, as shown in the schematic in Figure IV.7a. The film outside of the gap region exhibited a Raman peak at 650 cm^{-1} corresponding to B_{1g} mode in PdO

(ref) (Figure IV.7b).[57] Raman maps with respect to this feature were collected over a 6 x 6 μm^2 area in the crack region after applying successively programming voltages of 5, 8, 10, 12 and 15 V (Figure IV.7c-7g). The black patches in the maps correspond to the existence of Raman inactive Pd regions while blue represents PdO. With increasing RESET voltage, the blue region increased and as a result the crack appears to be closing up (see Figure IV.7c-7g). This may be attributed to the surface oxidation of Pd to form PdO particles.[58] Some particle movement is also noticeable, arising from electromigration, which is quite common among RS.

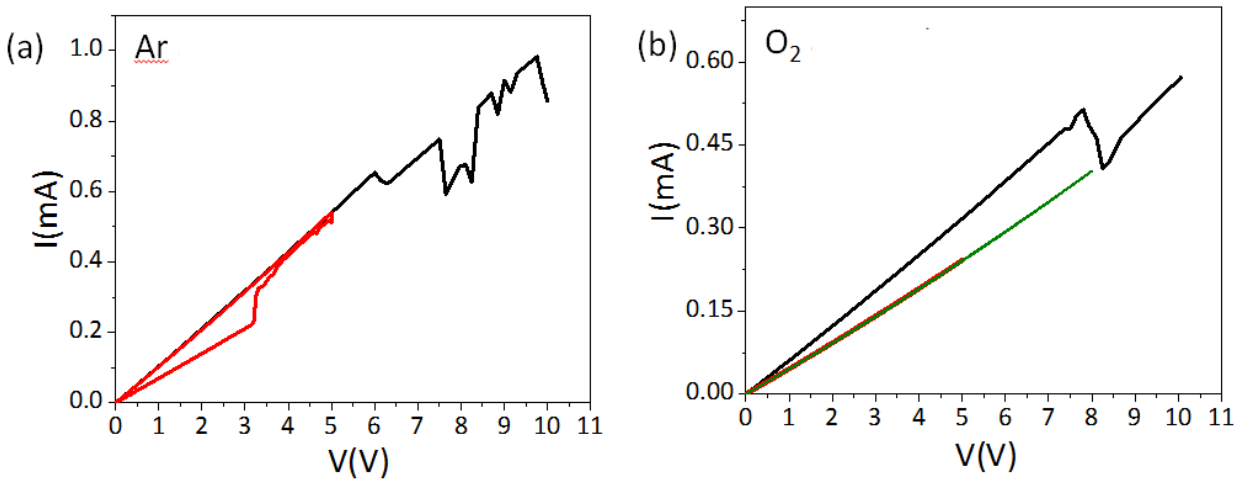

Figure IV.8 Resistive switching of a PdO MMS device in (a) Ar and, (b) O_2 atmospheres, respectively.

In order to understand the RS mechanism, the switching was tried in different atmospheres such as Ar and oxygen. The device exhibited RS in Ar atmosphere for first two cycles as shown in Figure IV.8a, however after two cycles, the device did not switch further. This indicates that oxidative atmosphere is essential for switching. Strikingly, the device showed lower RESET voltages (8V) in oxygen atmosphere as shown in Figure IV.8b and did not switch back to LRS from HRS state even at higher voltages. It is clear that the device requires oxygen for RESET process (LRS to HRS) whereas more oxygen is not favouring set process (HRS to LRS). Hence, the PdO MMS device exhibits switching only in the presence of dilute oxygen

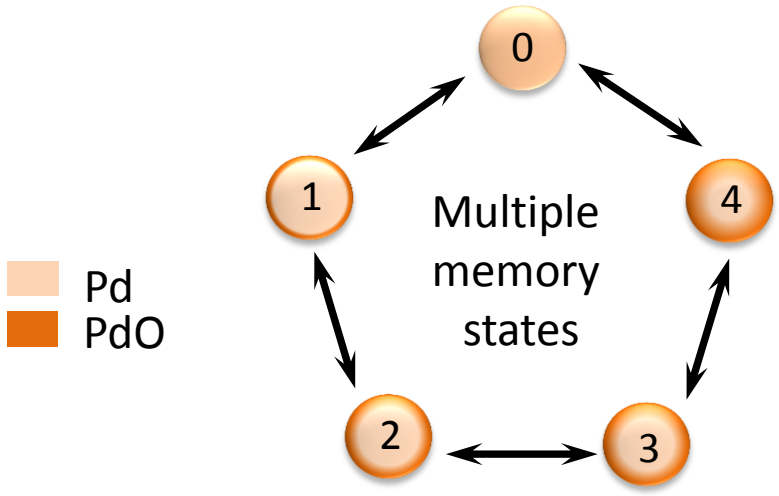

Figure IV.9 Schematic illustration of reversible surface oxidation and reduction of Pd nanoparticle.

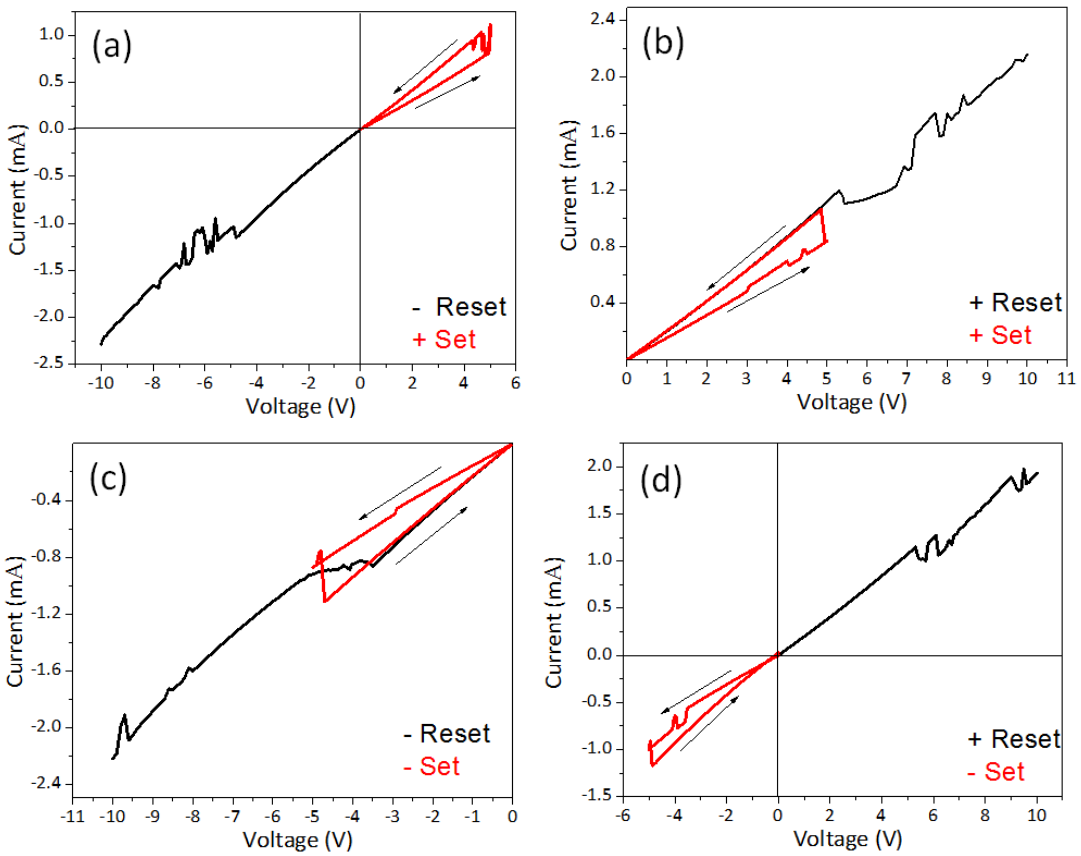

Figure IV.10 Non-polar resistive switching characteristics of PdO MMS device. The RESET and SET process performed at (a) negative-positive, (b) positive-positive, (c) negative-negative and (d) positive-negative bias polarities, respectively.

such as ambient condition, which is highly favourable for practical applications. This situation is different as compared with the devices made of SiO_2 and Al_2O_3, where RS takes place only in vacuum.[35, 59]

From the above experiments and observations, the following mechanism has been proposed for RS in PdO MMS device. In the forming process, PdO is reduced to Pd (see Figure IV.7). After forming, the device showed MMS because of the active Pd particles. In the RESET process, few monolayers of Pd was converted into PdO leading to surface oxidation.[58] Therefore, the increase in the resistance of the device is attributed to the surface oxidation. The content of the surface oxidation gradually increases with the applied V_{reset} voltage as shown in the schematic of Figure IV.9, leading to multiple resistance states. In the SET process, joule heating reduces surface oxidized PdO particles to Pd particles. The PdO is known to convert to Pd at elevated temperatures. Moreover, the switching is independent of the direction of the flow current (see Figure IV.10 for non-polar RS). Thus, the controlled reversible surface oxidation and reduction of active Pd particles present in the crack region is the cause for RS in PdO MMS devices.

In the literature, the reversibility of the multi-state memory devices in terms of intermediate state switching is rarely discussed. Most of them pertain to switching from and to the '0' state from a given state.[10-40] This aspect was given due attention in this study. In the present PdO MMS device, 5 memory states have been realized i.e. maximum possible switching combinations are 20, out of which only 14 switching events were fully possible, i.e. probability of 100% (Figure IV.11a). The cumulative probability of all switching combinations is shown in Figure IV.11b in the form of a histogram. The events shown in red are only partially possible with probability in the range of 15–60% while those in black represent events fully possible. An

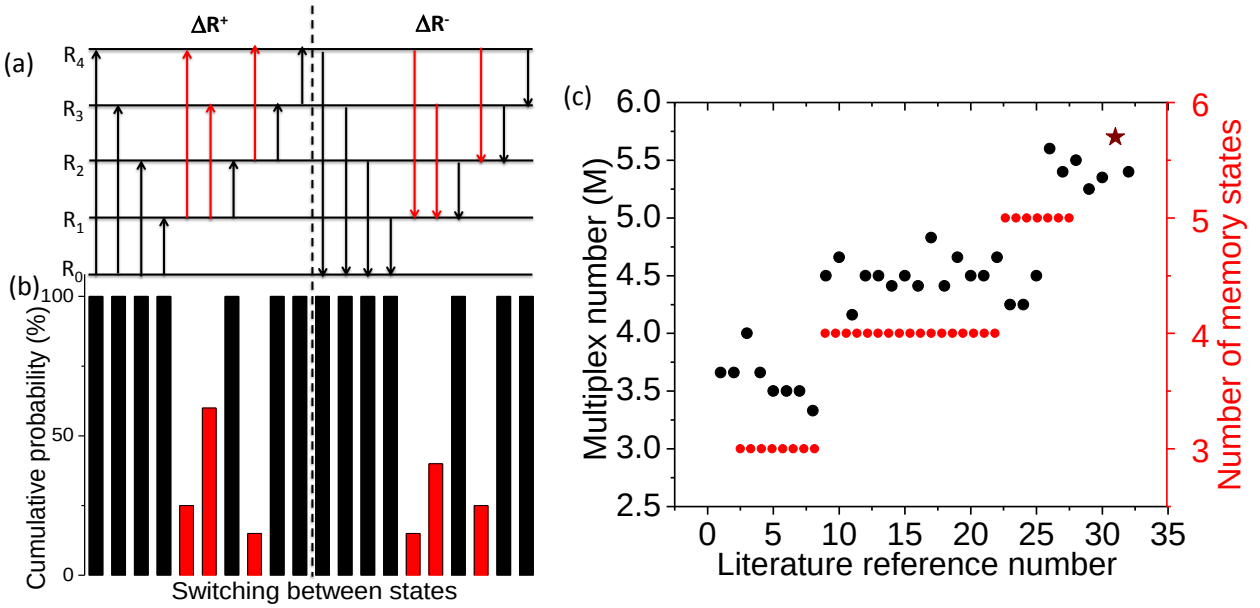

Figure IV.11 (a) Schematic illustration of switching between the memory states. Fully possible and partially possible switching combinations are represented with black and red arrows, respectively and (b) histograms of the corresponding cumulative probabilities for all switching combinations. (c) The multiplex number and number of memory states for various MMS devices fabricated in the literature.[10-40]

common analogy for the diagram in Figure IV.11a are the allowed and forbidden states in spectroscopy. The variation in the switching probability may be due to the lack of control over the oxidation or reduction in Pd nanoparticles, which require deeper understating of PdO resistive switching mechanism.

The existence of MMS and their importance in the next generation memory devices is self-explanatory. Unfortunately, there are no efforts in predicting or defining how many numbers of possible inter-state switching can takes place in MMS device. For the first time, a new parameter was defined and termed as 'Multiplex number (M)' which is a number that quantifies the quality of multi-level resistive switching devices. It is defined as,

$$M = n + \{\gamma/({}^{n}P_2)\} = n + \{\gamma/(n!/(n-2)!)\} \quad (3)$$

Here n is the number of states, and γ is the number of fully possible combinations of switching in between the memory states and ${}^{n}P_2$ the number of possible combinations of switching in between

the memory states. The first term enunciates the number of memory states in a device and the second term quantifies the fraction of switching events fully possible as against the total number; ideally, the second term should be unity. In other words, a MMS device with *n* states should have M of *n+1*, but in real situations, the M value stands between *n* and *n+1*. It should be noted by definition, M stands for a unique situation. In the present PdO MMS device, the multiplex number is 5.7, which may be interpreted as 5 memory states with 70% efficiency in switching. If it were to work with full efficiency M would be 6.0. Interestingly, M of 6.0 cannot represent a 6 state device as its efficiency would be reduced to zero! Similarly for all binary devices, M value will be 3 as switching efficiency (0 to 1 and 1 to 0) is always 100 %. M value of 5.7 for the present device is indeed appreciable compared to estimated values from other MMS devices reported in literature (Figure IV.11c and Table IV.2). For example, an estimate from ref yielded M of 3.5 which means the device has 3 memory states with 50% switching efficiency. Thus, the PdO MMS device has shown a high performance compared to MMS devices in the literature.

Table IV.2: Comparative study of multi-level resistive switching devices reported in the literature

S.No.	Device Structure	Device geometry	On/Off ratio	Retention time for all states (s) and reading voltage (V)	Conduction in		No. of states	Temperature dependent resistivity for all states	Multiplex number (M)	Ref.
					On state	Off state				
1.	Ti/ZrO_2 /n^+-Si	Out of plane	10^4	-	Ohmic	Non-ohmic	3	yes	3.66	10
2.	Al/CNT/Al	Out of plane	10^2	10^5 and -1	Ohmic	Non-ohmic	3	no	3.66	11
3.	Cu/TaO_x/ Pt	Out of plane	10^4	-	Ohmic	Non-ohmic	3	yes	4	12
4.	ITO /AlQ_3 /Al_2O_3 /AlQ_3 /Al	Out of plane	10^4	10^3 and 1	Non-ohmic	Non-ohmic	3	no	3.66	13

5.	Au/SiO_2/Au	Out of plane	10^4	-	Ohmic	Non-ohmic	3	no	3.5	14
6.	ITO/MEH-PPV/Al	Out of plane	10^5	-	-	-	3	no	3.5	15
7.	Ag/PI/graphene oxide:PI/PI /ITO	Out of plane	10^5	10^5 and 1			3	no	3.5	16
8.	Au /$Na_{0.5}Bi_{0.5}TiO_3$ /FTO	Out of plane	10		Non-ohmic	Non-ohmic	3	no	3.33	17
9.	Cu/HfO_2/Cu /Pt	Out of plane	10^7	10^5 and 0.1	Ohmic	Non-ohmic	4	yes	4.5	18
10.	$SrRuO_3$/$Ba_{0.7}Sr_{0.3}TiO_3$ /Pt	Out of plane	4	-	Non-ohmic	Non-ohmic	4	no	4.66	19
11.	ITO/PEDOT /organic/Al	Out of plane	10^3	10^6 and 1	Ohmic	Non-ohmic	4	yes	4.16	20
12.	Ag/organic/ITO	Out of plane	10^2	-	Non-ohmic	Non-ohmic	4	no	4.5	21
13.	Al/Alq_3/NiO /Al	Out of plane	10^3	10^5 and ~ 5	Non-ohmic	Non-ohmic	4	no	4.5	22
14.	Ag/Nb-doped $SrTiO_3$/Ti	Out of plane	10^4	-	Non-ohmic	Non-ohmic	4	no	4.41	23
15.	Ag/SiO_2/Pt	Out of plane	10^6	10^3 and 0.05	Non-ohmic	Non-ohmic	4	no	4.5	24
16.	Ti/ZrO_2/Pt	Out of plane	10^3		Ohmic	Non-ohmic	4	yes	4.41	25
17.	TiW/SiN/ Ge2Sb2Te5 /TiW	Out of plane	10^3	10^5 and 0.2	-	-	4	no	4.83	26
18.	Si/SiO_x/ITO	Out of plane	10^6		Non-ohmic	Non-ohmic	4	no	4.41	27
19.	Au /$La_{0.7}Sr_{0.3}MnO_3$ /Au	In plane	10^2	10^3 and ~15	Non-ohmic	Non-ohmic	4	no	4.66	28

20.	Pt/PA-TsOH /Pt	Out of plane	10^4	10^2 and -0.5	Ohmic	Non-ohmic	4	no	4.5	29
21.	$Pt/Cr_2O_3/TiN$	Out of plane	10^2	-	Ohmic	Non-ohmic	4	no	4.5	30
22.	Cu /GeTe/W	Out of plane	2		Ohmic	Non-ohmic	4	no	4.66	31
23.	TiN/HfO_x $/AlO_x/$ Pt	Out of plane	10^2		Ohmic	Non-ohmic	4	no	4.25	32
24.	$Au/C_{10}H_{12}O_2$ /STM tip	Out of plane	10	10^3 and 0.2	Non-ohmic	Non-ohmic	4	no	4.25	33
25.	$Pt/TiO_2/SiO_2/$ Si/ SGO/Pt	Out of plane	10^2	10^3 and 0.1	Ohmic	Ohmic	4	yes	4.5	34
26.	$Graphene/SiO_2$	In plane	10^4	10^4 and 1	Ohmic	Non-ohmic	5	no	5.6	35
27.	$Ti/Cu_xO/Pt$	Out of plane	10^4	10^2 and 0.2	Ohmic	Non-ohmic	5	no	5.4	36
28.	$Pt/TiO_2/TiN$	Out of plane	10^3	0.5 and 10	Non-ohmic	Non-ohmic	5	no	5.5	37
29.	Ti/AlOx/TiN	Out of plane	10	10^5 and 0.1	Non-ohmic	Non-ohmic	5	no	5.25	38
30.	$Al/Fe_2O_3/Al$	Out of plane	10^2	-	-	-	5		5.35	39
32.	Pt/NiO	Out of plane	10^5	--, 0.5	---	---	5	yes	5.4	40
31.	Au/PdO/Au	In plane	10	10^3 and 0.01	Ohmic	Ohmic	5	yes	5.7	Present work

IV.5 Conclusions

In this study, nanocrystalline PdO thin film has been successfully demonstrated as a MMS RS element in ambient conditions for the first time. The PdO MMS device has shown as many as five resistive memory states. The memory states are quite stable with high endurance and retention with variation less than 3%. The reading of the resistance states could be done with just 10 mV, due to the ohmic conduction. Based on low temperature resistance measurements, the conduction mechanism in the resistive memory states was found to be variable range hopping. SEM and Raman measurements provided a clear evidence for the conversion of initial PdO to Pd, which got surface oxidized during switching to high resistive states. The reversible oxidation/reduction of the active Pd/PdO particles is the basis of the MMS mechanism. For the first time, a 'multiplex number' has been defined to quantify the switching efficiency in-between the memory states. The multiplex number for the present PdO MMS device is 5.7, which is highest among the existing MMS devices in the literature. This may have high significance in futuristic 'human brain' like fabrication of memory devices.

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Chapter V

Lithography-free soldering of nanotubes

Summary

This study develops a simple lithography-free solution based method for soldering 1D nanomaterials with ohmic contacts, by taking specific examples of multi-walled carbon nanotubes (MWNTs), Si nanowires and ZnO nanorods. This is achieved by self-assembling a monolayer (SAM) soldering precursor, Pd^{2+} anchored to 1,10 decanedithiol, onto which MWNTs could be aligned across the gap electrodes via solvent evaporation. The nanosoldering was realized by thermal/electrical activation or by both in sequence. Electrical activation and the following step of washing ensure selective retention of MWNTs spanning across the gap electrodes. The soldered joints were robust enough to sustain strain caused during the bending of flexible substrates as well as during ultrasonication. The estimated temperature generated at the MWNT-Au interface using an electro-thermal model, is ~150 ºC, suggesting Joule heating as the primary mechanism of electrical activation. The XPS analysis and estimated interfacial gap between CNT and Au electrode from Simmons electron tunnelling model have given a clear evidence for desorption of SAM and soldering of MWNTs on Au electrodes with metallic Pd solder. The specific contact resistance is also derived from the transmission line model, which is less as compared to conventional lithography methods such as photolithography and electron beam lithography methods. This method also offers successful soldering of other 1D nanomaterials.

V.1 Introduction

One-dimensional nanomaterials (1D) are promising for many applications including biosensors, gas sensors, lasing, photonics, nanoelectronics and optoelectronics[1, 2]. The

electronic circuits made with 1D nanomaterials often lack robust contacts leading to high contact resistance that can dominate over their intrinsic resistance. High performance devices, such as field-effect transistors are achieved by different bonding processes that yield ohmic contacts with minimum contact resistance [3, 4]. For example, contact resistance can be reduced by depositing electrodes on top of 1D nanomaterials using approaches such as electron beam lithography (EBL) [5], but these patterning approaches can cause deleterious effects from contamination during processing. Further, fabrication of large-scale integrated circuits using EBL is rather slow and expensive.

Conversely, several different techniques have been attempted for soldering of 1D nanomaterials such as rapid thermal annealing [6], electron (or focused ion) beam induced metal deposition (EBID or FIBID) [7] and solder reflow [8]. Rapid thermal annealing is a harsh method and is not amenable to flexible substrates such as PET (polyethylene terephthalate). On the other hand, EBID and FIBID can cause diffusion of the solder into the 1D nanomaterial being soldered and thus can affect its electrical properties [7, 9]. However, such physical methods are expensive and not pliable to large areas. Although solder reflow [8, 10] is a reliable method for soldering positioned 1D nanomaterials between electrodes, it is tedious and not tractable to all nanoscale structures as the process involves integrating the solder segments to 1D nanomaterials during the synthesis. Hence, solution processed method with minimal contamination is of great importance to solder 1D nanomaterials.

Among 1D nanomaterials, carbon nanotubes (CNTs) have gained a great deal of importance, because of their unique electrical, mechanical and other outstanding properties [11]. The precise placement and alignment of CNTs across the electrodes has been done by two ways. First method is to grow the 1D nanomaterials directly on the electrodes. In second method, the

synthesized 1D nanomaterials were transferred by external means or self-assembled across the gap electrodes. But, the most effective method involves self-assembly of 1D nanomaterials without external stimuli. The soldering of 1D nanomaterials across gap electrodes was demonstrated by taking the example of multi-walled carbon nanotubes (MWNTs) which can sustain high current densities with potential applications in power transmission [12], IR detectors [13], transparent conducting electrodes [14] etc. Such applications require a simple lithography-free method to solder MWNTs with minimal contact resistance to realize high-performance devices. On the other hand, the present approaches have had limited success particularly with regard to flexible applications as the CNT junctions in circuits may not be robust enough to sustain bending [15]. In the literature, CNTs have been soldered across gaps by methods such as ultrasonic welding [16], electroless deposition on electrodes to reduce the contact resistance [17]. Also, local Joule heating along the interface of the CNT-electrode has been proposed for minimizing contact resistance [18], but during the process, oxidation of outer shells leads to rupture and damage of MWNTs [12, 19-21]. Hence, the conductance of CNT in air is limited by a threshold power above which oxidation occurs. Facile methods to solder CNTs across gaps with minimum contact resistance remain a crucial need if individual CNT properties have to translate into useful collective functions.

V.2 Scope of the present investigation

Previously, our group developed an EBL method to solder MWNTs across a gap with Pd hexadecanethiolate as a soldering precursor [22]. The present study is to formulate a simple lithography-free solution-based method by which CNTs as well as other 1D-nanomaterials. Here, a monolayer of Pd precursor self-assembled on the electrode surface was tried out as a solder material. Pd was chosen as a nanosoldering material for CNTs, as it is known to form ohmic

contacts.[23] The electrical soldering was attempted with external voltage/current sourcing. More effects have been put to generalize process, in order to solder other 1D nanoobjects.

V.3 Experimental Section

Au gap electrodes (50 nm thick) were deposited on glass substrates using a thin carbon fiber as shadow mask by physical vapor deposition with gaps typically 6 μm wide. As-deposited Au gap electrodes were cleaned with water, acetone and isopropyl alcohol just before the self-assembly. Subsequently, the substrates were immersed in a 50 mM solution of 1,10-decanedithiol in toluene for 2 hours; non-chemisorbed dithiol was washed away by excess toluene. Afterwards, the substrates were dipped in a 25 mM Pd^{2+} acetate in toluene for 1 hour and washed in toluene. Multi-walled carbon nanotubes (Sigma Aldrich) of diameters, 150–300 nm and lengths, 4–12 μm were used as active elements across the Au gap electrodes. The MWNTs were dispersed in *o*-dichlorobenzene by ultrasonication for 15 minutes. *o*-dichlorobenzene is considered as a good dispersing medium for the MWNTs and leaves minimal solvent traces after evaporation. ZnO nanorods were prepared by hydrothermal method [24]. Si nanowires were prepared by VLS growth method. The ZnO and Si nanowires were dispersed in ethanol. 10 μL of the nanotube/nanowire dispersion was drop-cast onto the gap electrode while heating the substrate at 80 °C.

The current–voltage measurements of the circuits were performed using a Keithley 236, which served as the source and measurement unit. SEM was carried out using a Nova NanoSEM 600 instrument (FEI Co., The Netherlands). The contact length of the MWNTs was estimated from the SEM images. AFM measurements were performed using a dimension 3100 SPM with NS-IV controller (Bruker, USA) in contact mode. Standard Si cantilevers were used for normal topography imaging. The sample for Fourier transform infrared (FTIR) spectroscopy was

prepared by drop casting (1 mM) Pd decanethiolate in toluene on a KBr pellet followed by evaporation of the solvent. The FTIR spectra of Au surface covered with Pd/SAM layers and thin film of Pd decanethiolate on the KBr pellet was taken in reflection mode. The FTIR measurements were recorded using a Bruker IFS66v/s spectrometer with a resolution of 2 cm^{-1}. X-ray photoelectron Spectroscopy (XPS) measurements have been carried out using a Omicron SPHERA spectrometer with non-monochromatic AlKα (E = 1486.6 eV).

V.4 Results and discussion:

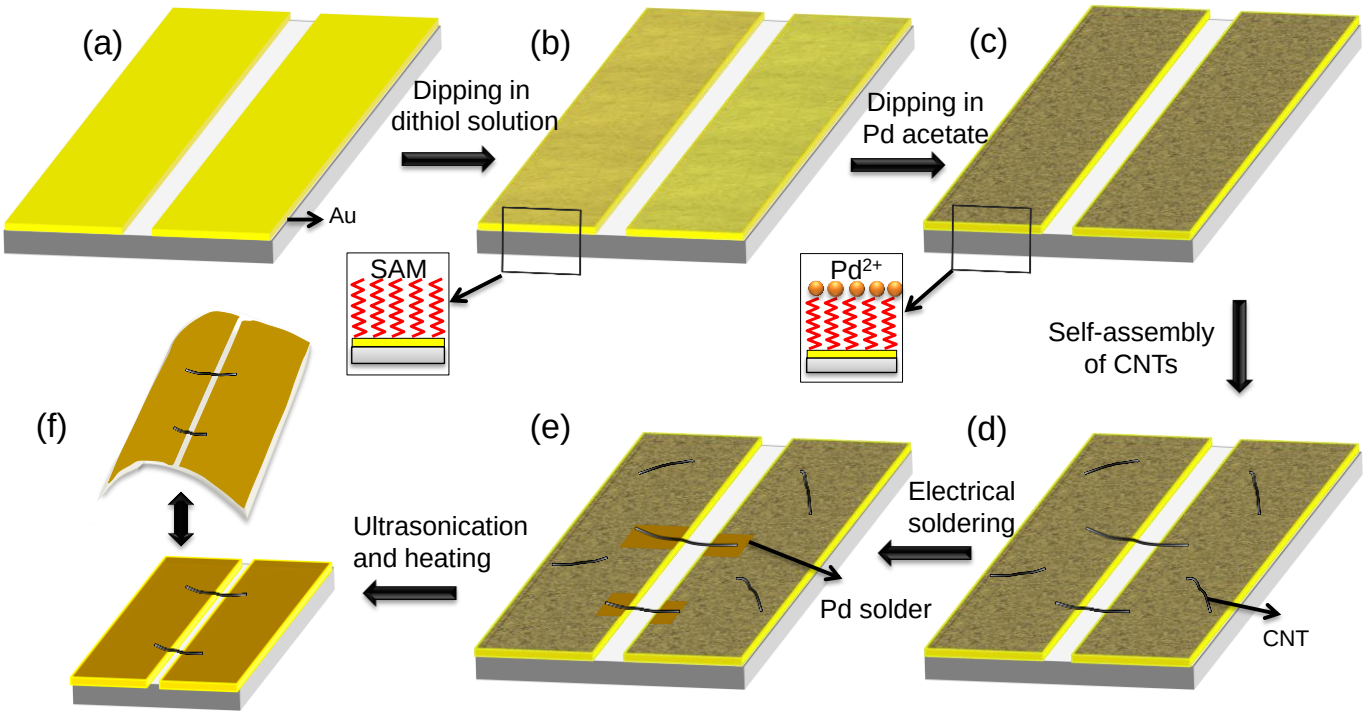

Figure V.1 Schematic illustration of the fabrication of a soldered CNT circuit: (a) 6 μm Au gap electrodes (~50 nm thick) (b) covered with SAM after immersion in 1,10 decanedithiol solution, followed by (c) decoration of Pd^{2+} onto SAM from Pd acetate solution. (d) CNTs assembled across the gap electrodes and (e) electrical activation for soldering; (f) ultrasonication and heating of CNT circuit for removal of unwanted CNTs. The method is extendable to flexible substrates as well.

The soldering ingredients are introduced via self-assembly across a pair of Au electrodes (separated by ~ 6 μm, see Figure V.1a). A self-assembled monolayer (SAM) of 1,10 decanedithiol is adsorbed firstly on Au electrodes (see Figure V.1b) and decorated subsequently with Pd^{2+} (Figure V.1c), which constitutes the soldering precursor, i.e., Pd/SAM. Further, CNTs

are aligned across the Au gap electrodes covered with Pd/SAM solder (Figure V.1d). The soldering of the as-prepared device was activated at first electrically (see Figure V.1e) following which the substrate is subjected to ultrasonication to remove un-activated CNTs (not spanning the gap electrodes). The soldering process was completed by thermolyzing the activated precursor at 250 ºC (see Figure V.1f). The method is extendable to flexible substrates as well and the solder joints are robust enough to take the strain caused during the bending (see Figure V.1f).

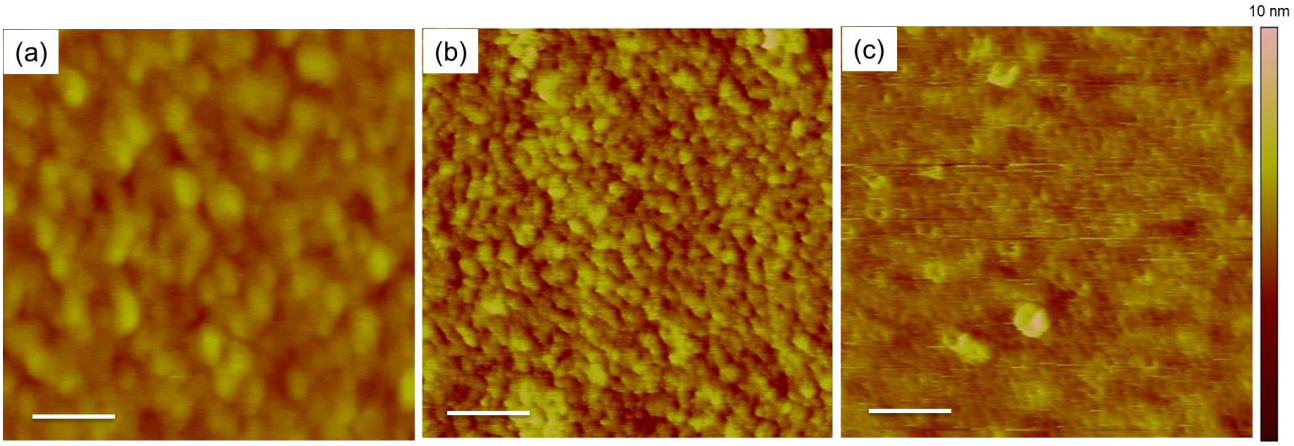

Figure V.2 AFM topography of (a) pristine Au surface (b) SAM/Au and (c) Pd/SAM/Au surface in 1 x 1 μm^2 area, scale bar 200 nm.

Initially, a detailed characterization of the self-assembled soldering precursor layer on Au electrodes was performed (Figure V.2). The AFM topography of pristine Au and SAM/Au surfaces in Figure V.2a, b has shown a roughness of 0.5 and 0.9 nm respectively. The Pd/SAM/Au electrode in Figure V.2c reveals the uniformity of the soldering precursor with the roughness being ~1.2 nm. The increase in roughness of the Au electrodes with sequential addition of SAM and Pd^{2+} layers is consistent with nanometric agglomeration of the soldering precursor seen in the AFM image (see Figure V.2). An increase in roughness with SAM thickness has been reported previously [25].

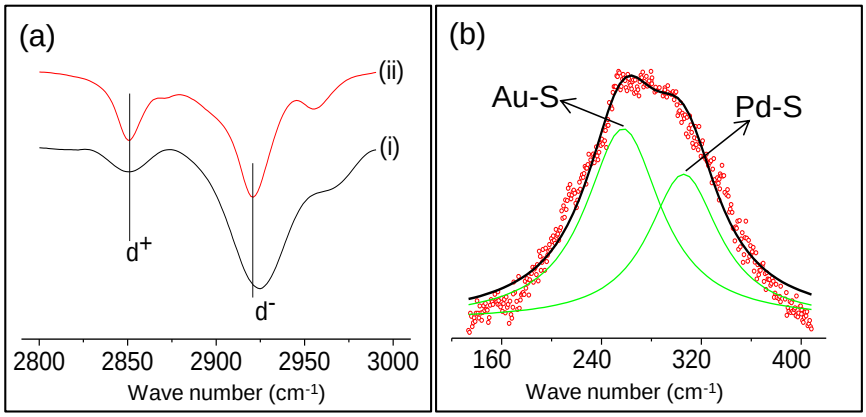

Figure V.3 Characterization of Pd/SAM covered Au electrodes. (a) FTIR spectra of Pd/SAM/Au (intensity has been multiplied by 3) (i) and pristine Pd decanethiolate (ii). (b) Raman spectrum (red circles) with the deconvoluted peaks (in green) corresponding to Au–S and Pd–S stretching modes.

The FTIR spectrum of the Pd/SAM/Au electrode in Figure V.3a exhibits peaks at 2850 and 2920 cm^{-1} corresponding to symmetric (d^+) and anti-symmetric (d^-) stretching vibrations of the methylene group respectively, typical of trans-conformation of the SAM [26]. This spectrum is compared to that of pristine Pd decanethiolate to assess order and crystallinity in the Pd/SAM layer. A blue shift of ~4 cm^{-1} is observed for the d^- peak in the case of Pd/SAM which signifies the presence of gauche conformers in chemisorbed SAM [27]. Figure V.3b elucidates the Raman spectrum of Pd/SAM, where the deconvoluted peaks at 257 and 306 cm^{-1} correspond to the stretching modes of Au-S and Pd-S bonds respectively [28, 29]. Thus, the Raman spectrum reaffirms the bonding of molecules with Au beneath and Pd on top (see Figure V.1c).

In order to determine the oxidation state of the Pd present on top of the SAM layer, X-ray photo emission spectroscopy (XPS) measurements were carried out on the self-assembled soldering precursor before and after thermolysis. The core level spectra of Pd 3d and Au 4d are observed close to each other due to their similar binding energies and therefore, the obtained spectra were deconvoluted from the observed broad peak as shown in Figure IV4a and 4b. The

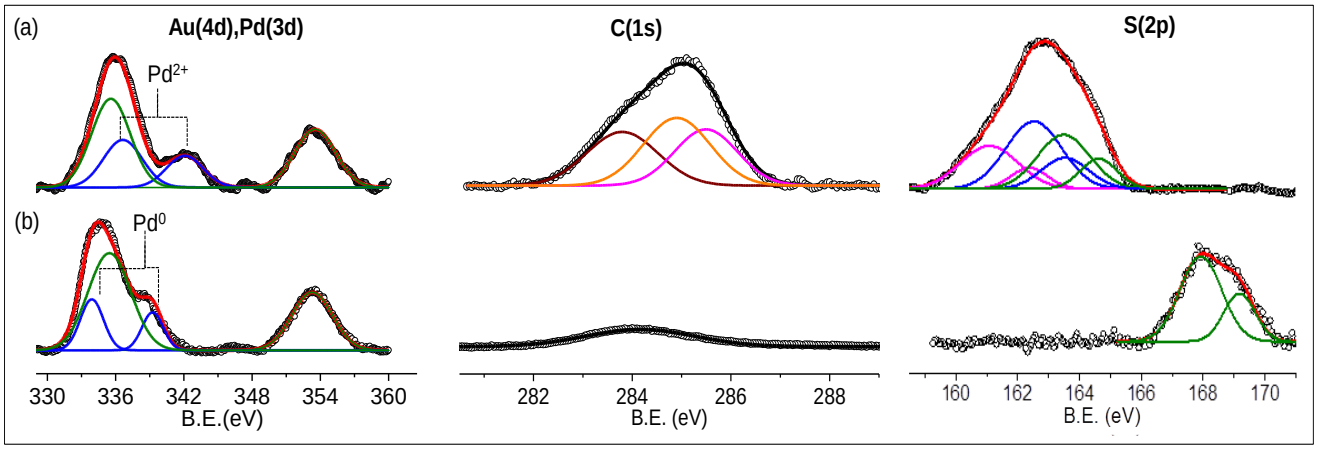

Figure V.4 Core level photoelectron spectra of Pd 3d, Au 4d, C 1s and S 2P before (a) and after heating (b) at 250 °C. (blue, green, orange, violet color peaks are deconvoluted peaks for the original data represented with black circles).

peaks at ~ 336.5 and ~ 342 eV (Figure IV4a) corresponding to Pd $3d_{5/2}$ and $3d_{3/2}$ respectively, are indicative of Pd^{2+} species residing on the SAM layer [30]. The soldering action (metallization) of Pd/SAM layer was also examined first with a control sample without CNTs. As expected, Pd^{2+} reduces to Pd metal after thermolysis [31] with the peaks shifting to lower binding energies ($3d_{3/2}$ ~ 339.25 and $3d_{5/2}$ ~ 334 eV, see Figure V.4). Of course, Au 4d core level features, $4d_{3/2}$ ~ 353.4 and $4d_{5/2}$ ~ 335.5 eV, respectively corresponding to the Au substrate [32] remain unchanged (see Figure V.4 left panel). The C1s core level spectrum before thermolysis is comprised of three peaks as shown in Figure V.4a (middle panel), which are positioned at 283.8, 284.9 and 285.4 eV corresponding to sp^2-hybridized carbon, C-C and C-S bonds, respectively [33, 34]. After heating to 250 °C, only one peak assignable to trace carbon was present at 284.1 eV while other peaks disappeared (see Figure IV4a middle panel). Notably, the C1s peak intensity decreased by 3 times, confirming desorption of the SAM. The deconvoluted peaks of S 2p signal indicate the presence of both Pd-S and Au-S bonds before thermolysis (see Figure IV4a, right panel) [35-37]. Detailed peak assignments are summarized in Table-IV1. Following thermolysis at 250 °C in air, broad sulfur signal was shifted towards higher B.E. (see Figure IV4b, right panel). This shift is

attributed to the presence of sulfonate species (SO_3^-, $2p_{3/2}$ at ~168 and $2p_{1/2}$ at ~169.15 eV respectively) [38]. Through these measurements, we confirm that thermolysis involves desorption of the SAM and concomitant conversion of Pd^{2+} to metallic Pd.

Table- IV1: Binding energies of Sulfur

S.No.	Heating	Bonding of S	Spin-orbit split peak	B.E. (eV)	Reference
1	before	Pd-S	$2p_{3/2}$	161.08	35
			$2p_{1/2}$	162.37	
2	before	Au-S	$2p_{3/2}$	162.4	36
			$2p_{1/2}$	163.5	
3	before	unbound S and S-S	$2p_{3/2}$	163.48	37
			$2p_{1/2}$	164.62	
4	after	SO_3^-	$2p_{3/2}$	167.9	38
			$2p_{1/2}$	169.15	

A dispersion of CNTs in *o*-dichlorobenzene was drop-casted on pre-characterized Au electrodes covered with Pd/SAM layer heated at 80 ºC for slow evaporation of solvent. The dispersed CNTs are dragged towards the gap as a result of the capillary force exerted by the solvent frontline during evaporation. The dragged CNTs span across the gap leading to self-alignment, which has been discussed in the literature [39]. We employed this method to align as many as twelve CNTs across a single Au gap electrode as shown in Figure V.5. We have examined several Pd/SAM/Au electrodes dosed with CNT dispersions which showed similar results. One such configuration is shown in Figure V.6a, where five CNTs bridge across the gap; the inset clearly

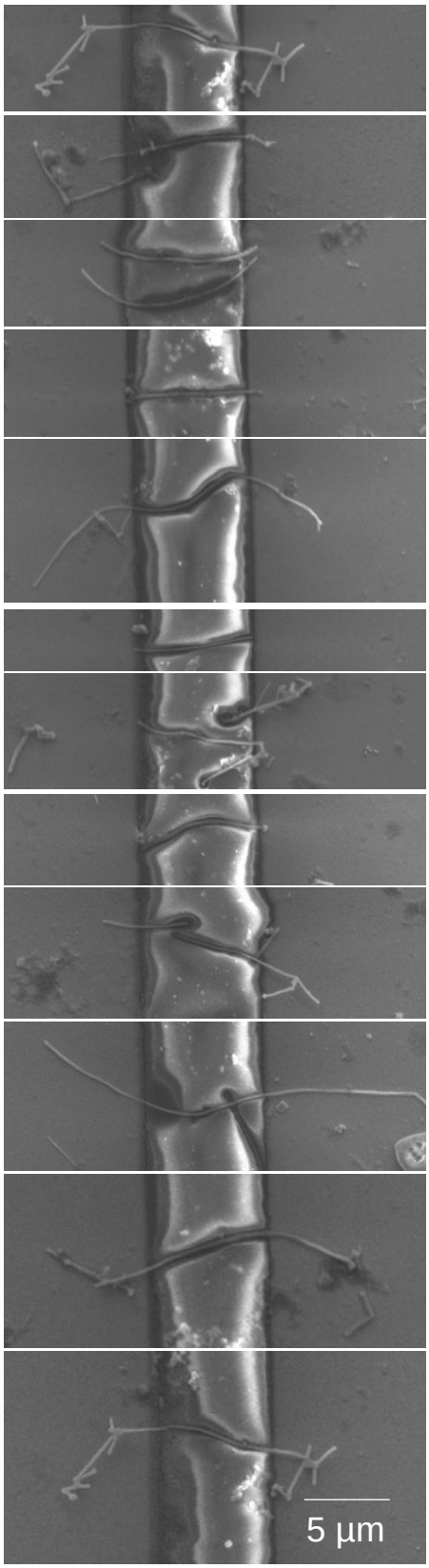

Figure V.5 SEM images of CNT circuit in 12 different areas stitched together with same scale bar.

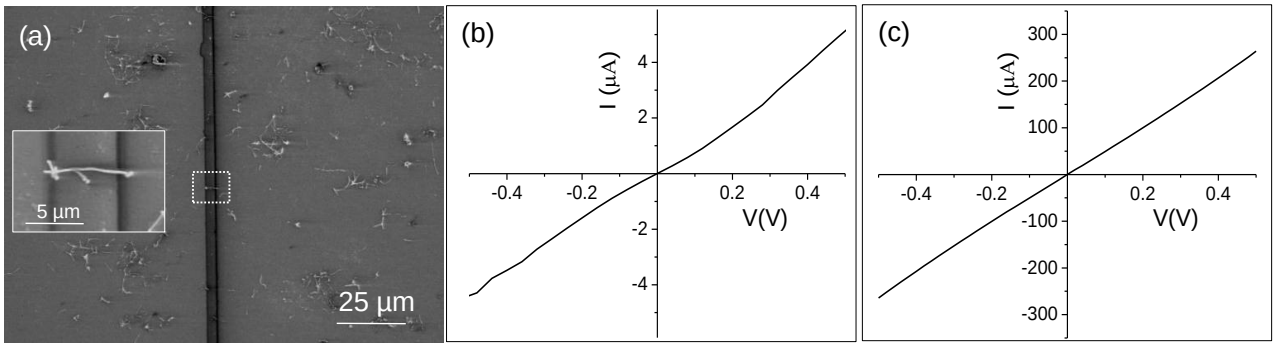

Figure V.6 (a) SEM image of the CNT circuit after self-assembly of CNTs with the inset showing a magnified view of single CNT across the gap. I-V characteristics of the self-assembled CNT circuit before (b) after heating (c) at 250 °C.

reveals that the CNT spans the gap between electrodes. The I-V characteristics of this circuit were slightly non-linear (Figure V.6b) with estimated resistance from the near zero bias region of 97 kΩ. This high value arises mainly due to the insulating nature of the SAM. The device was thermally activated by heating at 250 °C for 45 min to desorb the SAM. Thereafter, the current in the circuit increased implying that soldering by thermal activation decreased the contact resistance, and the I-V characteristics became linear, suggesting the ohmic nature of the contacts (Figure V.6c). The resistance reduced by nearly two orders to ~1.8 kΩ. This result clearly indicates thermal soldering mitigated the ultra-high contact resistance introduced by the SAM. In

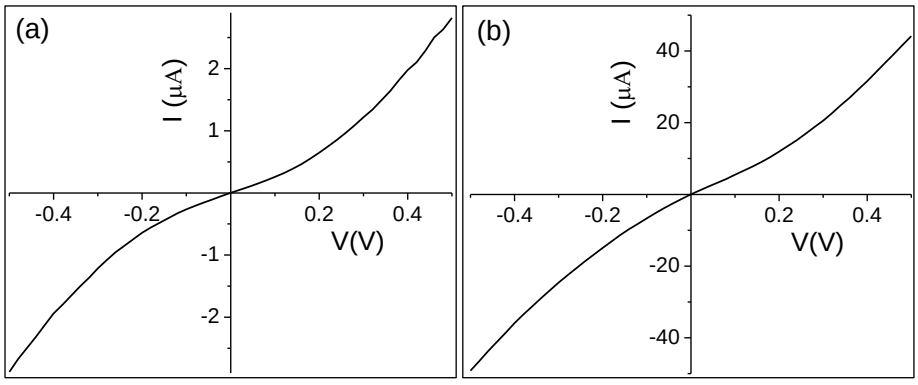

Figure V.7 I-V characteristics of CNT circuit (a) before and (b) after thermolysis without SAM/Pd (soldering precursor) layer.

order to test the soldering action of SAM/Pd (soldering precursor) layer. A controlled experiment was performed on a circuit with four CNTs self-aligned across the Au gap electrodes without any soldering precursor (Pd/SAM). As shown in Figure V.7, I-V characteristics of the CNT circuit is non-linear before and did not improve after thermolysis as well. This is a clear evidence that thermolysis alone cannot provide ohmic contacts with low contact resistance. Thus, the Pd/SAM soldering precursor is essential without which thermal treatment does not lead to ohmic contacts.

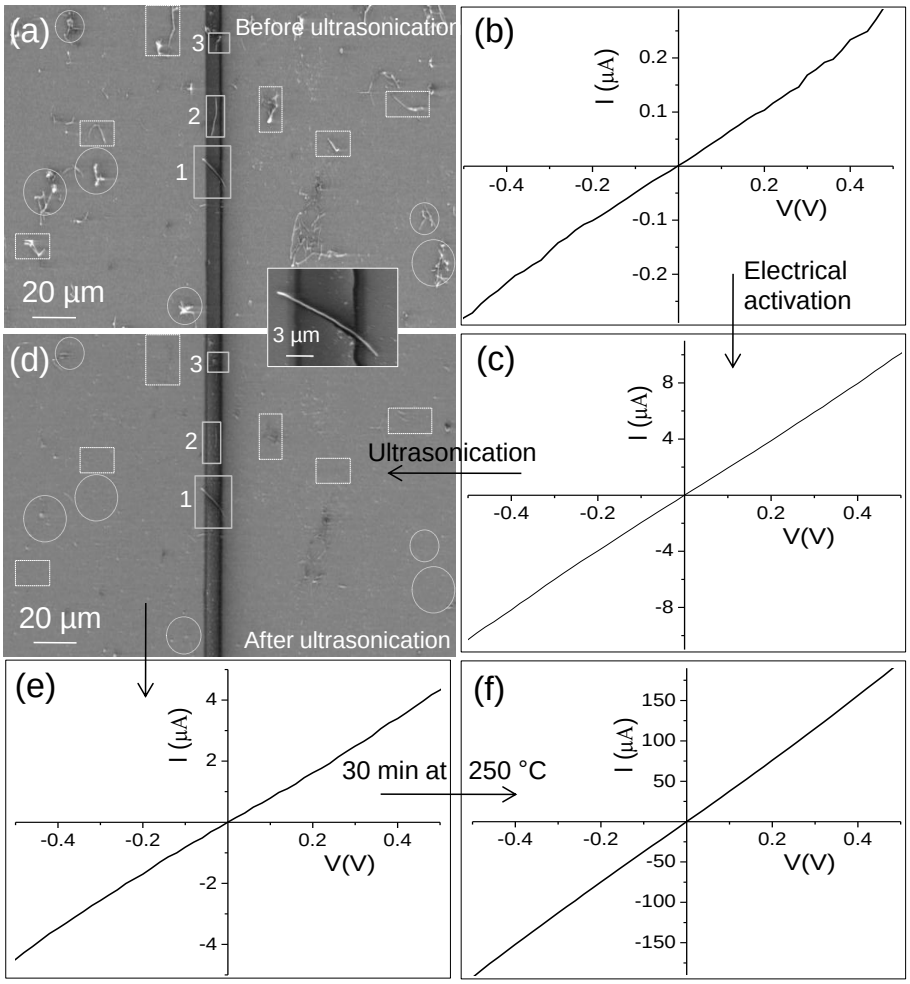

Figure V.8 SEM image of CNTs on Au gap electrodes (a) before ultrasonication, marked areas show randomly distributed CNTs and (d) after ultrasonication, marked areas do not contain CNTs. I-V characteristics of the pristine CNT circuit (b) before, (c) after electrical activation, (e) followed by ultrasonication for 30 s and (f) finally heating at 250 °C.

While the above process of using a SAM as a carrier for Pd soldering precursor leads to ohmic

contact between CNTs and the electrodes, the resultant structure lacks specificity. In other words, CNTs lying away from the electrical gap not participating in conduction are also glued to the electrode surface, which results in wastage of CNTs. A more desirable process could selectively solder CNTs spanning across the electrodes, enabling the retrieval of other CNTs. With this in mind, electrical activation of the soldering precursor was attempted (see Figure V.8). In the circuit shown in Figure V.8a, individual CNTs and bundles of CNTs are shown in rectangles and circles, respectively. Three CNTs lie near the gap of the electrodes, out of which the CNT labelled '1' neatly span across the gap electrode (see the inset for magnified view). The I-V characteristic of the pristine CNT circuit exhibited a resistance of 1.72 MΩ (Figure V.8b). Here, the electrical activation is achieved by applying a low voltage bias. To determine the optimal voltage bias, several bias values were tried out.

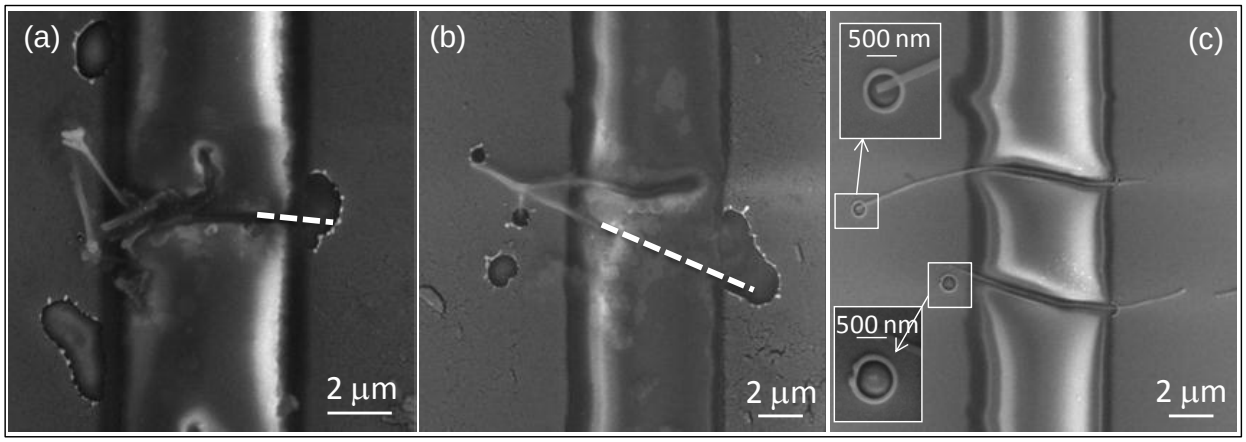

Figure V.9 SEM image of CNTs on Au gap electrodes after applying (a) 6 V for 30 s (b) 4 V for 50 s (dotted line shows the position of blown off CNT) and (c) 2 V for 60 s respectively. Insets show the magnified view of the ruptured area.

The electrical activation was performed on pristine circuits at different voltages 6, 4 and 2 V for 30, 50 and 60 s respectively. The SEM image of each circuit is shown in Figure V.9, which reveals that CNTs are damaged and electrodes got ruptured. As bias voltage is lowered from 6 V to 2 V, the damage of CNTs and rupturing of electrodes became less prominent (see Figure V.9). In circuits activated with high bias (~ 6 V and 4 V, see Figure V.9a, b), CNTs were blown off,

rupturing the electrodes due to the high power generated at the CNT-Au interface [18, 21]. Finally at 2 V bias, CNTs were undamaged though its footprint marks could be identified without any rupturing of the Au electrode (shown in inset of Figure V.9c). The CNT damage may be due to more Joule heating at higher bias. For this reason, the electrical activation was limited to lower bias. For this reason, the circuit was activated at a lower bias (2 V) for a short time (15 s). Interestingly, current in the circuit increased by two orders of magnitude after electrical activation (see Figure V.9c). Two possible effects may lead to this behaviour, Joule heating and electrical migration; here, an electro-thermal model is therefore considered (*vide infra*).

Following electrical activation, unsoldered CNTs and extraneous carbon material can be removed by mild ultrasonication of the substrate in *o*-dichlorobenzene for 30 s. The electrically activated CNTs were found to be intact with the Au electrodes even after ultrasonication, as shown in Figure V.8d. The CNTs that do not span the gap electrode were washed away during ultrasonication and can be reused for the fabrication of new CNT circuits. Notably, the decrease in current after ultrasonication (Figure V.8e) is due to the removal of one of the self-assembled

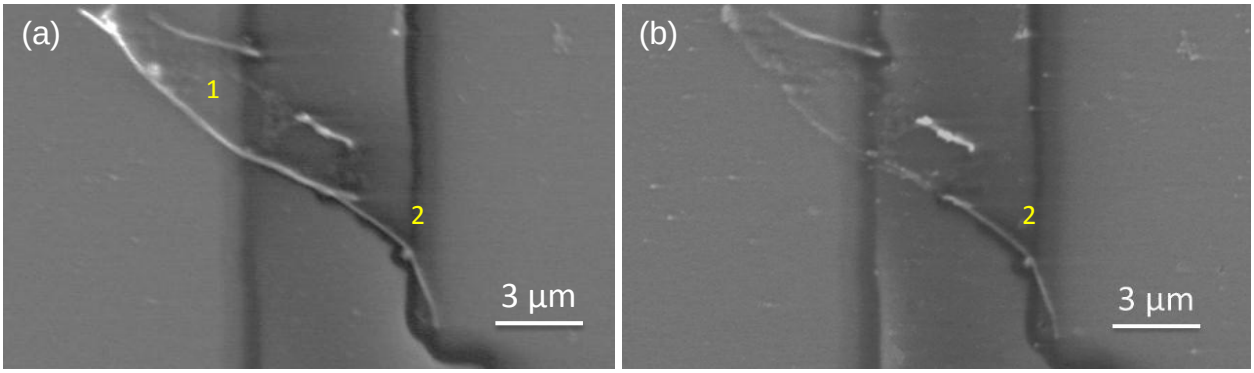

Figure V.10 SEM image of CNTs on Au gap electrode (a) before (b) after ultrasonication.

CNT spanning the gap electrode in addition to the presence of solvent traces. A careful examination of the CNTs span across the gap electrode was carried out to test the stability of soldering process, while undergoing ultrasonication test. The circuit in Figure V.10a shows two interconnected CNTs (labeled as 1&2) which were subjected to ultrasonication. The CNT-1 got removed while the CNT-2 remained intact (see Figure V.10b). This suggests complete soldering for CNT-2 while the CNT-1 was partially soldered. Its removal suggests that only weak electrical activation occurred for the CNT-1, may be due to its relatively high resistance (removal of the CNT is shown in Figure V.10). However, the current in the circuit was enhanced following heating the circuit at 250 °C for 30 min (Figure V.8f). The resistance of the CNT circuit was 2.5 kΩ after thermal activation, which decreases the resistance by nearly two orders. Thus, the electrical and thermal activation were combined to selectively solder the CNTs spanning across the gap. However, the former alone may not be practical for circuits containing many CNTs, as the current required to cause complete soldering will be proportionally very high and can lead to damage of CNTs.

In order to investigate the electrical activation process in detail, a circuit with only one CNT spanning across the gap was fabricated. The SEM image of the CNT shown in the inset of Figure V.11 clearly shows the CNT spanning across the gap with a contact length of 2.72 ± 0.1 μm on the electrodes. The initial resistance of the single CNT circuit was ~ 100 kΩ due to the presence of insulating species prior to soldering. Current-controlled experiments were performed in order to prevent thermal runaway during the transient drop in contact resistance that occurs during electrical activation. For this purpose, a variable current source was ramped at a constant, controlled rate of 5 mA s^{-1}, and the transient resistance change was measured. Initial tests were

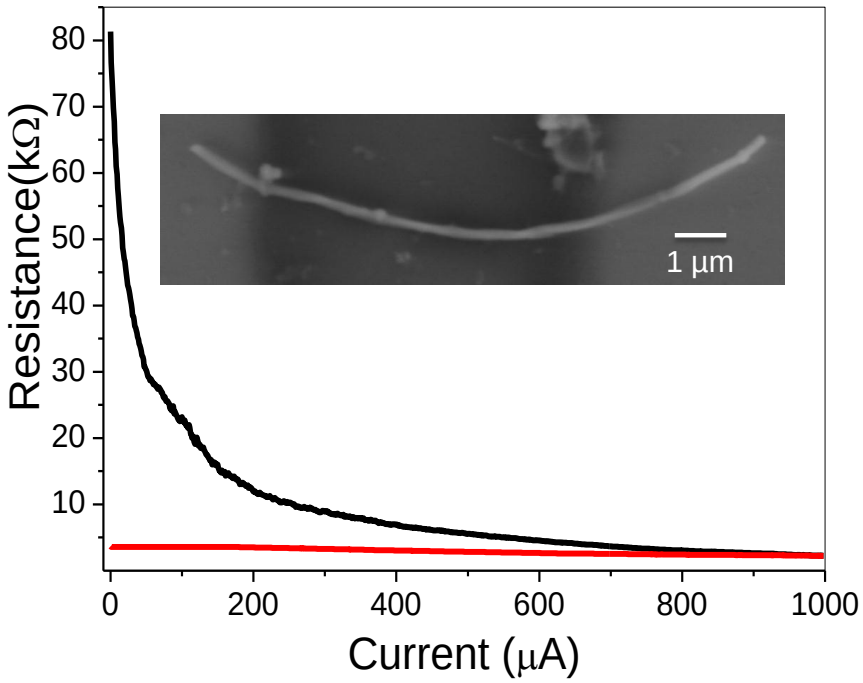

Figure V.11 Resistance of a single CNT circuit as a function of current during (black) and after (red) the electrical activation. Inset shows the SEM image of CNT spanning across Au gap electrodes self-assembled with Pd/SAM layer.

performed by sweeping the current from 1 to 10, 1 to 20 and 1 to 100 μA respectively as shown in Figure V.12. A small and temporary decrease in resistance was observed in consecutive current sweeps, which interestingly reversed to the initial value upon withdrawal of the current (see Figure V.12). This indicates that the electrical soldering could not occur within the current range of 1 to 100 μA; higher current value is inevitable.

However, the application of 1 to 1000 μA decreased the resistance permanently by ~20 times as shown in Figure V.11, suggesting that electrical activation occurred in the current range of 100 to 1000 μA. The resistance of this circuit decreased permanently from 100 to 3.6 kΩ after the electrical soldering; the reduction in resistance here compares well with that obtained via thermal soldering. It demonstrates that the above method of current controlled activation would suffice for simple circuits with a single CNT such as the one shown in Figure V.11, while circuits containing multiple CNTs may additionally require the following step of thermal

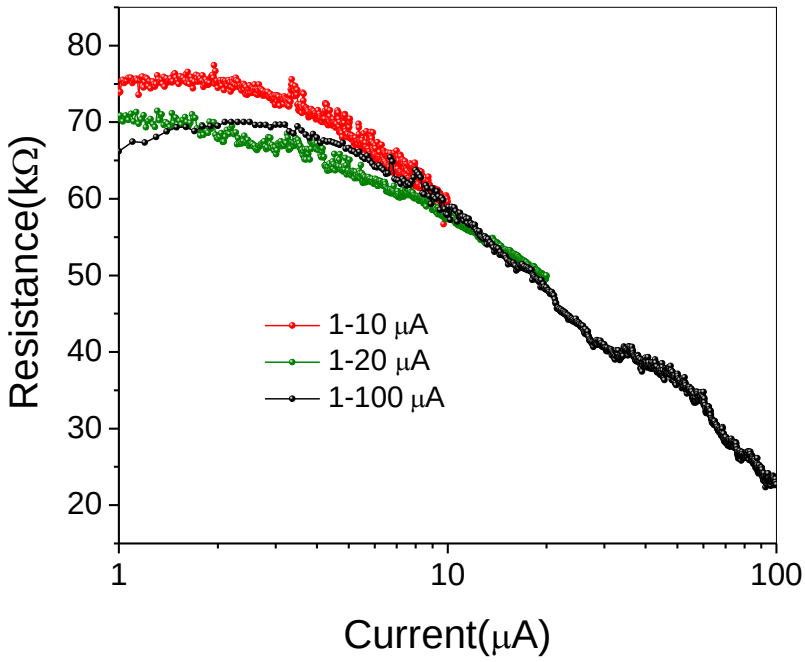

Figure V.12 Resistance versus current characteristics of a single CNT circuit.

treatment to achieve lower contact resistances. This is not surprising because parallel-channel devices would not be expected necessarily to exhibit equal resistances in each channel. Therefore, the Joule heating would be non-uniform, resulting in high variations in activation. Between the two types of electrical activations, current controlled activation is considered superior as there is less chance of overloading and rupturing of the electrodes (compare Figures. V.9 and V.12); but this is applicable effectively only for single CNT circuit. A summary of the CNT circuits fabricated in this study is given in, Table-IV2.

To assess the dominant mechanism of electrical activation, a simplified electro-thermal model is considered as depicted in Figure V.13. In this model, only the electrically and thermally active region of the SAM is considered and thermal boundary resistance between the CNT and Au substrate is neglected [40]. In other words, the highly insulating SAM layer prohibits current flow laterally across the SAM, forcing current to flow vertically across the SAM through the CNT contact. The Joule heat generated in the SAM is expected to induce its desorption in the activation region (Figure V.13a, dashed area), enabling Pd to aggregate at the CNT-Au

Table-IV2: CNT soldering data with circuits attempted in this study

No.	Number of CNTs spanning the gap	Total contact length (μm)	Type of soldering	Resistance of the circuit		Resistance per one CNT (kΩ)
				Before soldering (MΩ)	After soldering (kΩ)	
1	1	2.72	Electrical	0.1	3.6	3.6
2	1	6.25	Electrical	0.620	1.9	1.9
3	1	0.3	Electrical	316	8	8
4	1	2.36	Electrical	460	2.08	2.08
5	1	3.2	Thermal	625	4.3	2.8
6	1	3.4	Thermal	200	1.2	2.2
7	5	8.1	Thermal	0.097	1.8	9
8	6	16	Thermal	0.25	0.2	1.2
9	2	7.4	Electrical +Thermal	1.72	2.5	5

interface, as shown in Figure V.13b. Under conditions of steady electrical current and heat flow, the temperature of the SAM-CNT interface (T_{SAM}) results from Joule heat generation per unit area *P"*:

$$T_{SAM} = T_{Au} + P"/G" \quad (1)$$

where *G"* is thermal conductance per unit area of the SAM-CNT interface and T_{Au} is the

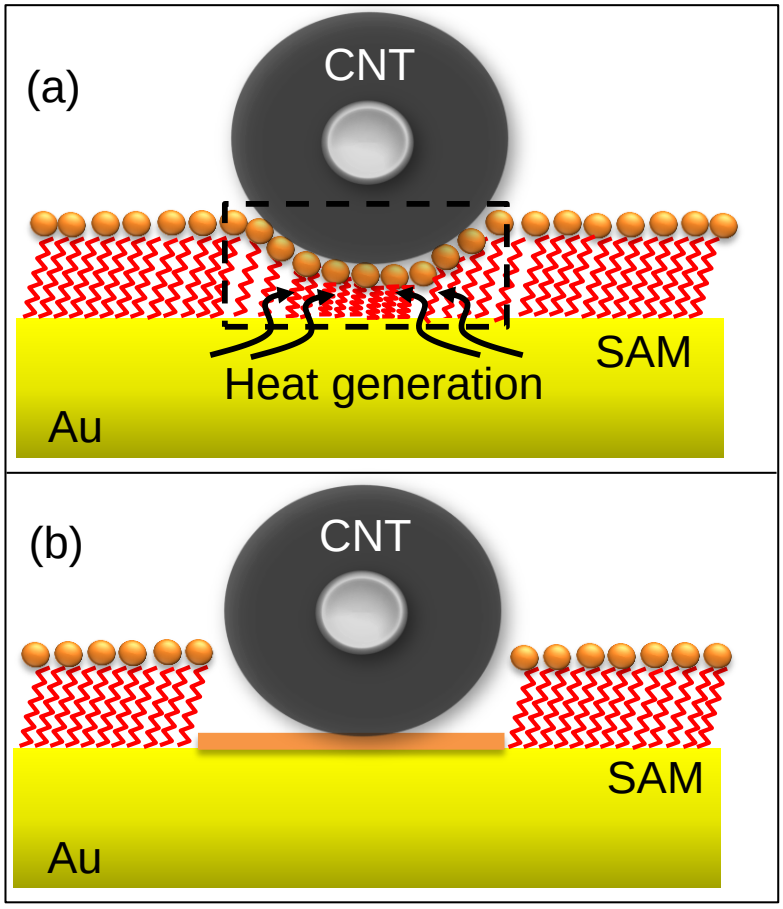

Figure V.13 Schematic illustration of the CNT circuit (b) before (the dashed rectangle encloses the activation region) and (c) after electrical activation.

electrode temperature. The thermal conductance (*G''*) of the Au-SAM was considered to be 220±100 μW μm^{-2} K^{-1} based on the literature value of experimentally measured conductance of an alkanethiol functionalized Au surface [41]. The contacting perimeter between the SAM and CNT was estimated as 32±1 nm for the ~160 nm diameter (see SEM image Figure V.11), assuming perfect conformation of the SAM on the CNT surface (see Figure V.14). The SAM-CNT interface area is calculated by assuming that SAM completely conforms to the CNT. Since, the CNT just touches Au substrate active region, the width of the electrically active region can be determined geometrically (see Figure V.14). We approximate the width, *w* in terms of the CNT diameter, *D* and SAM thickness, *t*:

$$w = 2\sqrt{0.25D^2 - \left(0.5D - t\right)^2}$$

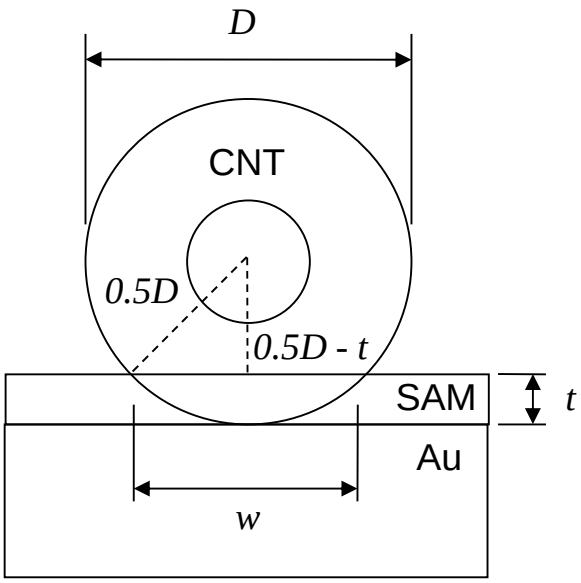

Figure V.14 Schematic utilized to determine width of the active region at CNT-Au interface.

The CNT in the circuit under consideration has a diameter of ~ 160 nm and contact length of 2.72 μm as determined from SEM. Employing Eq. (1), the width of the active region of the SAM is w = 32±1 nm, resulting in an active area of 0.087±0.003 μm^2. The CNT-SAM contact area is therefore estimated as 0.087±0.003 μm^2, based on the length and perimeter of the contact. The average heat energy generation rate and temperature rise of the SAM were calculated as a function of source current from the experimental electrical activation data (Figure V.11) based on the above described theory, and the result is shown in Figure V.15. As shown in the plot, the temperature bounds (red dashed curves) suggest that the temperature of the SAM increases with increase in current. In contrast to the thermal treatment (250 $^{\circ}$C, 45 minutes), the duration of the entire electrical activation experiment was short (0.2 s). Thus, only a small portion of the SAM at the SAM-CNT interface could be desorbed from the local Joule heating (see Figure V.13b and Figure V.1e), and this resulted in electrical connection between the Au electrode and the CNT

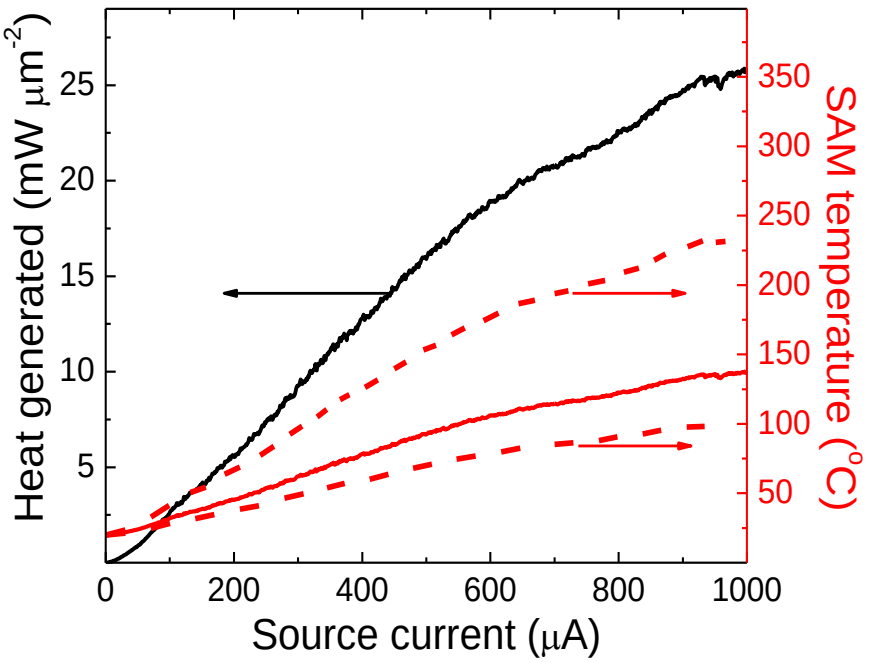

Figure V.15 (a) Heat generation and SAM temperature at the CNT-Au interface as a function of source current during electrical activation of a CNT circuit. Theoretically predicted SAM temperature (solid red line) has bounds due to uncertainty of Au-SAM thermal conductance indicated by dashed red lines.

through Pd. This finding supports the conjecture that electrical activation occurs via a localized Joule heating mechanism. For a deeper insight in the details of the electrical activation mechanism, the Simmons electron tunnelling model [42] was applied for this circuit to assess the electronic transport regimes before and after electrical activation. To measure the interfacial gap between the CNT and Au electrodes, the I-V characteristics are fitted with the following Simmons equation: [42]

$$I = \left(\frac{eA}{4\pi^2\hbar d^2}\right)\left\{\left(\phi_B - \frac{eV}{2}\right) \times exp\left[-\frac{2(2m)^{1/2}}{\hbar}\alpha\left(\phi_B - \frac{eV}{2}\right)^{1/2} d\right] - \left(\phi_B + \frac{eV}{2}\right) \times exp\left[-\frac{2(2m)^{1/2}}{\hbar}\alpha\left(\phi_B + \frac{eV}{2}\right)^{1/2} d\right]\right\}$$

where I is the current through junction, m is the electron mass, d is the interfacial distance, $\phi_B$is the barrier height, V is the applied bias, h is plank's constant and a is a unitless adjustable parameter. The interfacial distance (d) between CNT and Au was calculated by fitting the I-V

characteristics of the device before and after soldering with the above equation as shown in Figure V.16.

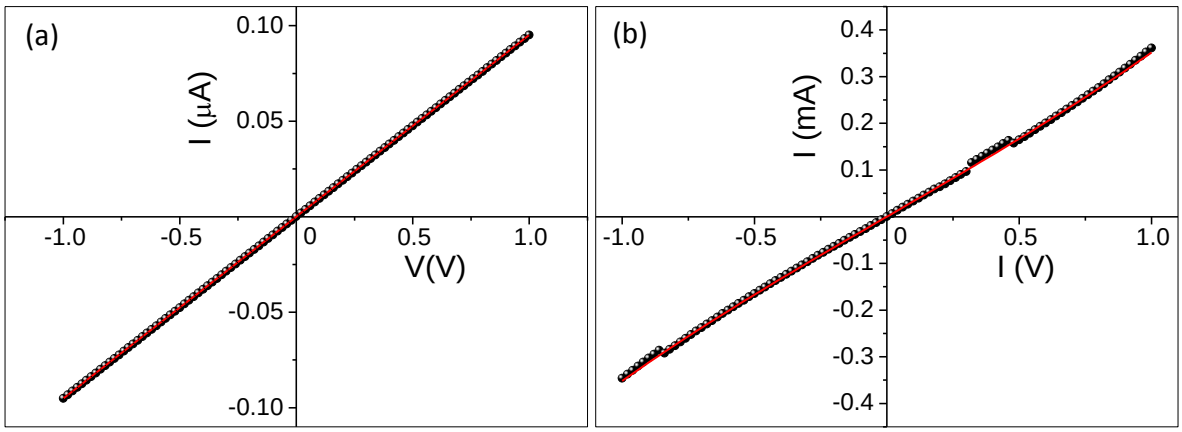

Figure V.16 I-V characteristics of single CNT circuit (a) before and (b) after electrical soldering. Black dots are experimental data and red lines are the best fit of the tunneling model.

The interfacial gap was estimated to be ~ 2.1 nm from the I-V characteristics of the circuit as shown in Figure V.16a, which indicates that the interfacial gap is roughly comparable to the length of the 1,10-decanedithiol molecule (~1.4 nm) [43]. As shown in the schematic of Figure V.16b, the CNT is supported on top of the SAM distributed with Pd^{2+}. After electrical soldering the fitted interfacial gap is 0.13 nm (see Figure V.16b) suggesting a good (metallic) bond between CNT and Au electrodes (See Figure V.13b). Sufficient electrical heating desorbs SAM molecules in the electrically active region; thereby Pd solder forming at the CNT/Au interface. Thus, the electrical activation decreased the interfacial gap to form good electrical contact.

The electrical resistance of the soldered circuit, i.e, total resistance, comprises the actual resistance of the CNT (R_{CNT}) and specific contact resistance (r_c). To estimate the actual resistance of the CNT, a transmission line model was applied as described by Lan *et al* [44]. The contact resistance and resistance of the CNT were estimated by using the following equation derived from the transmission line model [44]

$$R(x) = \left(\sqrt{r_{CNT} r_c}\right) \coth\left(\sqrt{\frac{r_{CNT}}{r_c}}\, x\right) + \left(r_{CNT} L'\right) + \left(\sqrt{r_{CNT} r_c}\right)$$

where $R(x)$ is the total resistance of the circuit, r_{CNT} is the resistance per unit length, r_c is the specific contact resistance for a unit length, x is the contact length and L' is the length of the CNT between the electrodes.

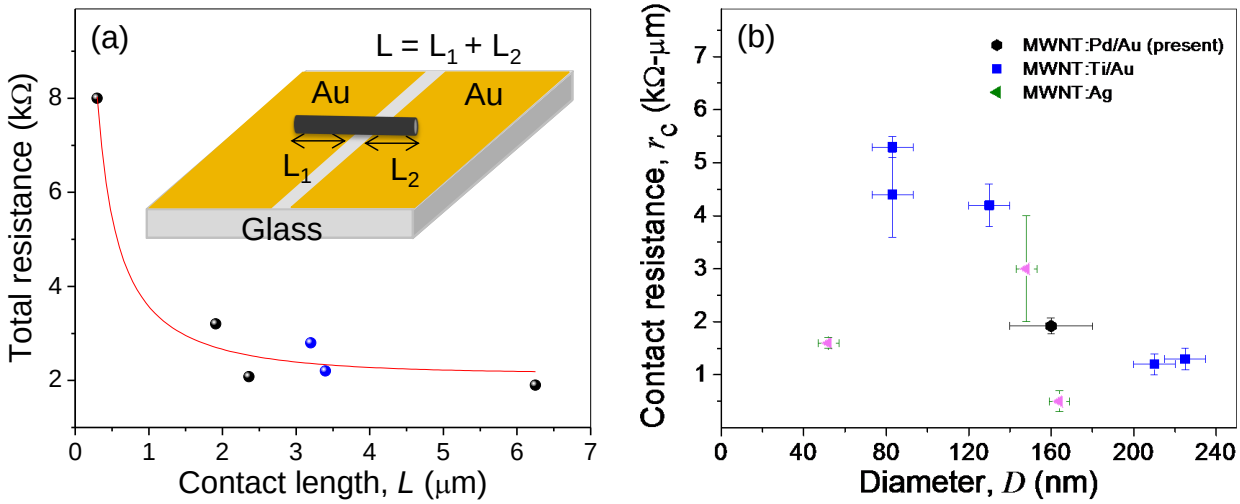

Figure V.17 (a) Total resistance versus contact length of single CNT circuits. The solid circles experimental data, solid line is best fit for resistance from a transmission line model.[40] (b) Linear contact resistivity as a function of CNT diameter soldered via different processes. The legend indicates the type of CNT-metal bond. Data for CNT: Ti/Au and CNT: Ag is depicted from Refs.[44, 45]

The contact length of the single CNT circuit was calculated from the SEM image as shown in Figure V.11. The plot between the total resistance and contact length of six single CNT circuits is shown in Figure V.17a (black circles, blue circles represent thermally and electrically soldered circuits respectively). The red curve is the best fit for the data, and the estimated parameters are the CNT resistance (R_{CNT}), 0.16 ± 0.02 kΩ μm^{-1} and specific contact resistance (r_c), 1.92 ± 0.15 kΩ-μm. As shown in Figure V.17a, the decrease in total resistance with contact length was significant and suggests that the transport in the circuit was not dominated by contact resistance, thereby establishing the efficacy of our soldering recipe. A length-independent measure of

contact resistance, specific contact resistance r_c, is also considered to quantify the CNT binding quality obtained by the present electrical activation process. The specific contact resistance is defined as $r_c = R_c L$, where R_c is the total contact resistance in kΩ and L is CNT contact length in μm. Because this parameter is a length-independent measure of contact resistance, it provides an intrinsic metric to compare the soldering quality of CNTs of differing sizes and for varying bonding electrode materials. In Figure V.17b, the specific contact resistance obtained with the present electrical soldering process is compared to those obtained via conventional metal deposition. CNTs of various sizes have been bonded and their linear contact resistivity values have been presented previously [44, 45]. As depicted in Figure V.17b, the present bottom-up process yields specific contact resistance near the low end of the distribution of contact resistances from the literature. With such low linear contact resistivity, integration of the present facile fabrication process may be rapidly achieved for CNT circuit fabrication.

The present soldering process was extended to flexible substrates (kepton, 6 μm gap electrodes) as well. Figure V.18a shows the I-V characteristics of a CNT circuit, containing two CNTs soldered to the electrodes. There is minimal change in the I-V characteristics after five bending cycles, demonstrating the robustness of the soldered circuit. A careful examination of the circuit using SEM (Figure V.19) showed that the CNT was intact across the Au electrodes at bending diameter of 1 cm. The traces shown in the top inset in Figure V.18a expose relatively small change in the position of the CNT while soldered regions being unaffected. Many such circuits have been tried out in bending experiments (Table-IV3). The small changes in the CNT geometry across the gap do reflect in the circuit resistance (Figure V.18b). The resistance is observed to increase with bending diameter of the substrate, in both compression and tension,

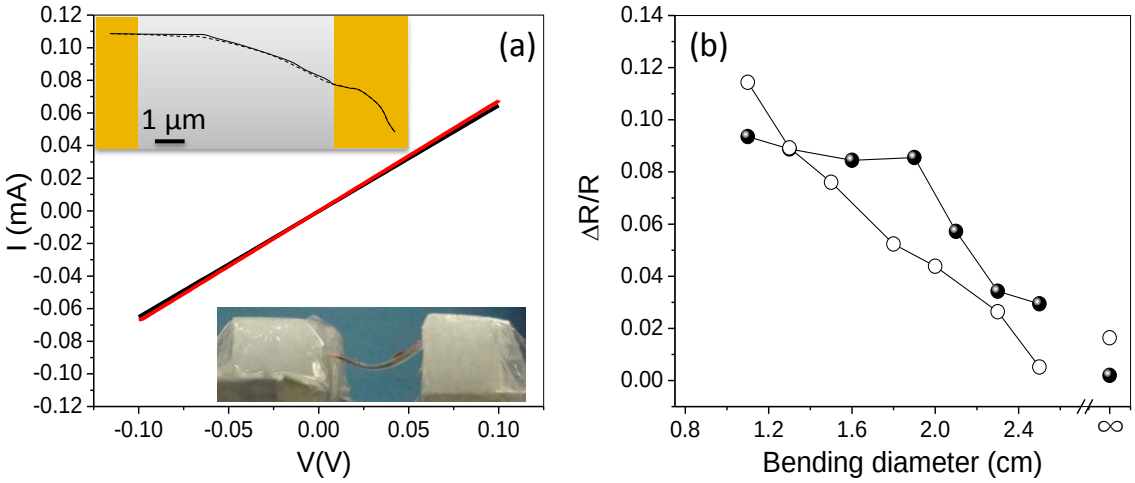

Figure V.18 (a) I-V characteristics of the soldered CNT circuit before (red curve) and after five bending cycles (black curve), top inset shows the trace of SEM images, flat (solid line) and bended (dotted line), and bottom inset shows the photograph of flexible CNT circuit. (b) Change in resistance of CNT circuit with respect to bending diameter, compression and tension data are represented by solid circles and open circles respectively.

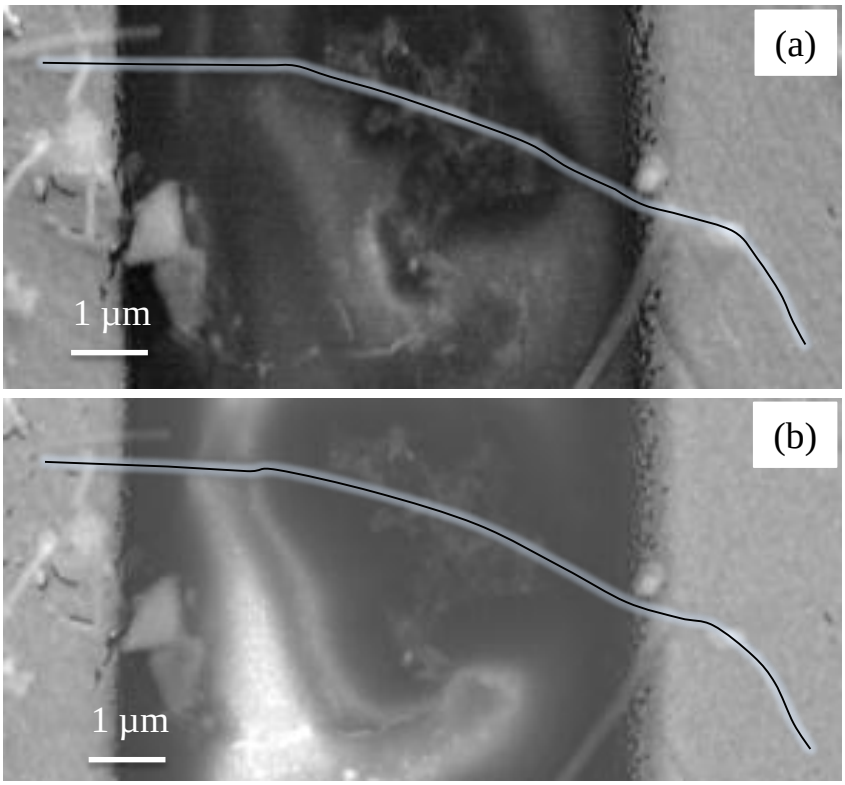

Figure V.19 SEM image of soldered CNT on Au gap electrodes in (a) flat position and (b) bent at a diameter of 1cm.

which is attributed to the incremental strain in the CNT (unlikely at the soldered interface), which is consistent with literature [46]. The gauge factor for the various circuits was in the range of 0.57 to 6.28, which is comparable to the values observed in the case of MWNT/epoxy nanocomposite (GF~10) [47]. Metallic CNTs are known to exhibit weak sensitivity to strain [48]. The change in resistance is minimal after making the circuit flat (at infinity diameter) following a bending cycle (see Figure V.18b). This indicates that the soldered contact between CNT and the Au electrodes is robust, which is an essential requirement for high performance flexible electronics.

Table-IV3: CNT soldering data with circuits attempted on flexible substrate

Sample number	**Number of CNT's**	**Resistance (kΩ)**		**Resistance per CNT (kΩ)**	**change in Resistance (ΔR/R)**	**Gauge factor**
		Before soldering	**After soldering**			
1	1	1220	4.3	4.3	0.011	0.85
2	1	225	5	5	0.006	0.57
3	1	185	2.7	2.7	0.009	1.57
4	2	57	2.4	4.8	0.015	2.12
5	2	230	1.5	3	0.013	4.21
6	4	35.2	0.97	3.8	0.024	6.28

This method of soldering can be generalized for many 1D nanomaterials. In the following example, ZnO nanorods prepared by a hydrothermal method [24] were placed across Au gap electrodes covered with Pd/SAM layer. The I-V characteristics of as-made circuit are shown in the Figure V.20a (see black curve). The current in the circuit is in the nA range due to high

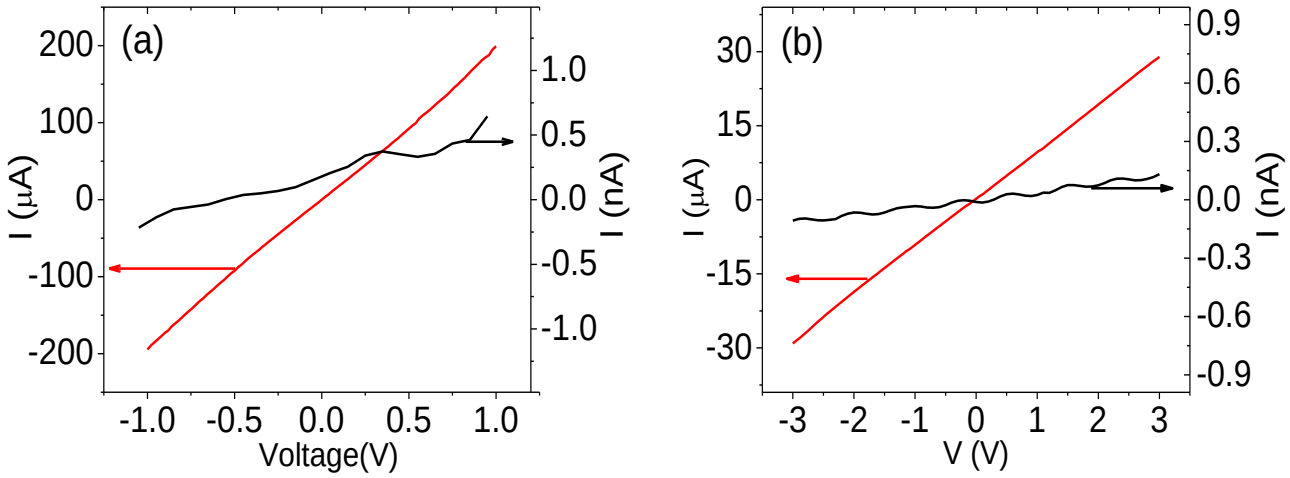

Figure V.20 I-V characteristics of (a) ZnO nanorods and (b) Si nanowires (NWs) before and after thermolysis (before and after thermolysis represented by black and red lines, respectively).

contact resistance. The substrate was then heated to 250 ºC for 1 hr to thermally solder the ZnO nanorods across the gap. The current in the circuit increased by four orders of magnitude after heating as shown by the I-V characteristics after heating (Figure V.20a, see red curve). Also, the I-V characteristics became linear due to the ohmic contacts between the ZnO rods and Au electrodes. A similar case involving Si nanowires is shown in Figure V.20b, where the current in the circuit increased by three orders following soldering. Thus, the presented method can be employed for soldering 1D nanomaterials in general, without any disparity between semiconducting (e.g., ZnO, Si nanowires) and metallic nanomaterials (e.g., CNTs).

V.5 Conclusions

A simple lithography-free solution-based method to assemble and solder 1D nanomaterials (nanotubes and nanowires) across a gap was investigated. The soldering precursor, Pd^{2+} anchored to 1,10 decanedithiol was introduced onto the electrodes by a self-assembly process. The nanosoldering has been carried out by thermolysis as well as by electrical activation. In thermal activation, the substrate is heated to desorb the molecules leading to form

ohmic contacts between CNT and electrodes with minimal contact resistance. In electrical activation, selective soldering of nanotubes was ensured by means of self-heating at the contacts, by Joule heating, i.e., local thermolysis, leaving behind a conductive metal contact. The temperature generated at interface between CNT and electrodes is estimated to be ~150 °C. The unwanted carbon material and unsoldered CNTs not spanning across the gap were removed by ultrasonication. This method proposed here is highly selective in soldering only the active CNTs across the gap implying that the neatness of the circuit is maintained and parasitic conductance paths via randomly laid CNTs can be avoided. The current controlled activation is better than the voltage controlled activation to avoid thermal runaway of the circuits. The specific contact resistance estimated from the transmission line model is compared to the lower values found in the literature. The flexibility of the soldered circuit is shown at various bending diameters, while the soldered joint unaffected. The method is generic and has been successfully applied to soldering MWNTs, and 1D nanomaterials including ZnO nanorods and Si NWs.

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Chapter VI

Summary and Outlook

Chapter-I of the thesis has dealt with an overview of old and new materials and tools, device made using those including modern devices. This introduction is a platform for literature results bringing out issues related to the experimental work carried out in the thesis. **Chapter-II** deals with characterization tools and techniques used in the thesis. In **Chapter-III**, a newly developed crackle lithography technique has been reported, useful in producing 'invisible' material patterning. While this technique can be adapted to pattern a material of choice onto any arbitrary substrate, here it was employed to fabricate metal wire networks on transparent substrates to realize transparent conducting electrodes. Thus fabricated TCEs have been used effectively to fabricate devices, in lieu of conventional TCEs. In the recipe used in this thesis, the crackle template was fabricated using drop or spin coating of the colloidal dispersion and metal deposition was carried out in vacuum. It is worth noting that the method *per se* has no such limitation and indeed it can be potentially extended to roll-to-roll fabrication relying on solution based processing. Another prospective of this method is to fabricate wire networks with novel materials other than metals, or in the form of heterostructures involving various functional materials/substrates. The metal network derived TCEs are highly suitable for the fabrication of electrochromic, thermochromic, light emitting diodes and transparent FETs devices. The crackle lithography can be used for patterning of rough surfaces as well. Such patterning may be important for highly textured Si solar cells to serve as transparent metal electrode.

Chapter-IV has dealt with fabrication of a multi-bit memory device based on resistive switching in PdO thin films. The devices are fabricated in an extremely simple way with in-plane geometry, unlike the capacitive geometry of conventional resistive switching devices reported in

the literature. These devices not only showed multi-level resistive switching with high endurance, retention and reliability but also switching between intermediate resistance states with good multiplex number. This fabrication method has a great promise and is easily adaptable to large area and high density in-plane memory device fabrication. These MMS devices can be used in futuristic neuromorphic devices and 'human brain' like memory devices. In **Chapter-V** selective soldering of CNTs in circuits has been realized. The fabrication method allows reusing the redundant CNTs not participating in electrical conduction. The soldered joints are ohmic in conduction with low contact resistance and are mechanically robust. This method can be extended to other 1D objects, as well as 1D devices ranging from field effect transistors to transparent conducting electrodes. The selective soldering of CNTs can be used in large area and highly dense array of CNT devices fabrication.

In short, the thesis work has successfully demonstrated that the fabrication recipes and methodologies, with a clear focus on low infrastructural material requirements ensuring low cost fabrication while being environmentally acceptable. In many instances, large area flexible devices have also been demonstrated. It is envisaged that many of these processes should be easily taken forward to industries and be part of next generation devices.

List of publications

From this thesis:

1. **K. D. M. Rao**, R. Gupta and G.U. Kulkarni, Fabrication of Large Area, High-Performance, Transparent Conducting Electrodes Using a Spontaneously Formed Crackle Network as Template, ***Adv. Mater. Interfaces***, 1, 6, (2014)
2. **K. D. M. Rao**, Christoph Hunger, R. Gupta, Giridhar U. Kulkarni and Mukundan Thelakkat, ITO-free organic solar cells using metal network based transparent conducting electrode derived from cracked polymer template, ***Physical Chemistry Chemical Physics***, 16, 15107 (2014).
3. **K. D. M. Rao**, R. Gupta and G. U. Kulkarni, Transparent and flexible capacitor fabricated using metal wire network as transparent conducting electrode, ***RSC Advances***, 4, 31108 (2014).
4. **K. D. M. Rao** and G. U. Kulkarni, Highly crystalline single Au wire network as high temperature transparent heater, ***Nanoscale,*** *6*, 5645 (2014).
5. **K. D. M. Rao**, Ritu Gupta**,** Kartikeya Srivastava, Ankush Kumar, S. Kiruthika, and Giridhar U. Kulkarni, Spray coating of crack templates for the fabrication of transparent conductors and heaters on flat and curved surfaces, ***ACS Applied Materials & Interfaces***, 6, 13688, (2014).
6. **K. D. M. Rao**, Christoph Hunger, R. Gupta, Mukundan Thelakkat and G. U. Kulkarni, Semitransparent inverted organic solar cells with random Au mesh/PEDOT:PSS hybrid top electrode, 2014, submitted.
7. **K. D. M. Rao,** Kartikeya Srivastava and G. U. Kulkarni, Transparent strain sensor with Au wire network, 2014, submitted.
8. **K. D. M. Rao**, Abhay, T. Pradeep and G. U. Kulkarni, In plane multilevel resistive switching PdO thin films, 2014, submitted.
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